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Reconfigurable Filter Design for Implantable Auditory Prosthesis

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Introduction

Cochlear Implants (CI) are implantable electronic devices that can partially restore hearing to profoundly deaf patients by directly stimulating the patient's auditory nerve via surgically implanted electrode arrays [1]. Rather than introducing a processed acoustic signal, implants receive, process, and transmit acoustic information via electrical stimulation. A block diagram of a transcutaneous CI is shown in Fig. 1.

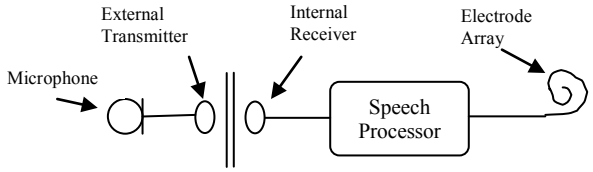

Fig. 1. Implantable system of a transcutaneous CI

In the last few decades, CIs have known huge developments. These developments regard electrode design, type of stimulation, signal processing, etc. Recent trends in CI developments try to have the sound processor fully implanted along with the receiver and the electrode system [2].

The Continuous Interleaved Sampling (CIS) algorithm is a multi-channel sound processing approach developed by the Research Triangle Institute (RTI) [1, 3]. It uses non-overlapping interleaved pulses for stimulation of the cochlea/auditory nerve. The block diagram of the CIS processing approach is shown in Fig. 2.

The signal processing is done as follows: the speech signal is first compressed/pre-emphasised (PGA) to match the patient's hearing dynamic range. It is then split into a number of sub-bands by a bank of bandpass filters (BPF). Each sub-band is responsible for the stimulation of a specific area inside the cochlea. The envelopes of the filtered signals are extracted and used to control the amplitude of the stimulation pulses. Finally, trains of non-simultaneous biphasic pulses are generated.

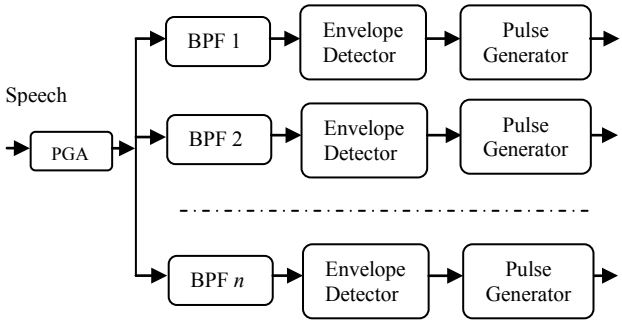

Fig. 2. Block diagram of the CIS processing

As such, there are a number of parameters associated with the CIS approach that can be programmed to optimize speech recognition performance for each patient: pulse rate and pulse duration, stimulation order, compression function and filter spacing [1,4]. Reprogramming of the cochlear implant, refers to setting the electrical stimulation limits necessary for the cochlear implant user to perceive soft and comfortably loud sound.

With fully implanted speech processors reprogramming becomes an issue, as there is no direct access to manipulate the processor parameters. Mapping information can only be transmitted over the same wireless link [5] as the speech information (see figure 1). Thus, programmable processing blocks become of great interest for such fully implanted speech processors.

This paper proposes a fully reconfigurable Gm-C filter for use in CIS implants. A current-mode analog signal processing technique has been implemented due to the advantages over its digital equivalent: low power consumption, speed, etc. The targeted application however gives a series of constraints to the analog circuitry: low supply voltages, low power consumption, a minimum of 60 dB dynamic range, tunability over a wide frequency range and high linearity.

The work is organized as follows. First of all, the design and the configurability of the main analog blocks is discussed. Further on, the simulation results of the analog

blocks are presented. Finally a conclusion is drawn by summarizing the main contributions of this paper.

Circuit Design

The need for low power consumption and low power supply voltages is satisfied by operating the MOS transistors in the subthreshold region. With vBS=0, the drain current is expressed as:

$$i_D = \frac{W}{L} I_{D0} \exp\left(\frac{v_{GS}}{nU_T}\right), \quad (1)$$

where W and L are the width and length of the transistor, respectively, Id0 is the subthreshold pre-exponential current factor, n is the subthreshold slope factor, and $U_T = KT/q$ is the thermal voltage.

The transconductor is implemented with the fully differential symmetrical OTA topology with inherent common mode feedback [6]. The exponential relationship between the output current and the gate-to-source voltage, expressed in (1), shows that a linear voltage-to-current transformation is only produced for small input signals, the linear range being limited. Thus, resistive source degeneration is implemented for linearization.

The schematic of the proposed Wide Linear Range OTA (WLR OTA) is given in Fig. 3. The transistor aspect ratios are then listed in Table 1.

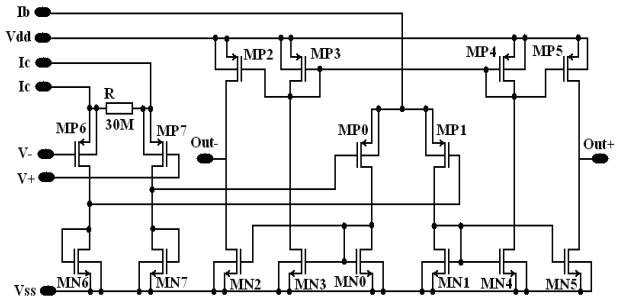

Fig. 3. Circuit schematic of the fully differential Wide Linear Range OTA

As can be seen in Fig. 3, a second input stage was added to achieve an increased flexibility for controlling the OTA parameters [7], [8]. Two bias currents control the OTA transconductance: the main bias current I_b and the input stage bias current I_c. The effects of the two bias currents on the transconductance value are listed in table 2.

Table 1. Aspect ratios of the WLR OTA transistors

Transistor	Aspect Ratio
MN0, MN1, MN6, MN7	12.2µ/10µ
MN2, MN3, MN4, MN5	3.05µ/10µ
MP0, MP1, MP6, MP7	31.2µ/5µ
MP2, MP3, MP4, MP5	7.8µ/5µ

Table 2. Gm variance of the OTA in respect to its bias currents

Bias Current	Transconductance
I_b ↑	G_m ↑
I_c ↑	G_m ↓↓

As it is shown in Table 2, I_b is used for fine tuning and I_c is used for hard tuning the OTA.

Using the OTA from Fig. 3, several active circuit element equivalents can be implemented [9]: active resistors, inductances, i.e. gyrator + capacitor, etc. Their equivalent values depend on the OTA gain, and are consequently controlled by the OTA bias currents. Thus, the passive equivalent component values can be tuned accordingly to achieve desired specifications.

The Gm-C biquad is based on a passive RLC prototype [9]. It is built by replacing the passive components with their active equivalent. The resulting schematic is shown in Fig. 4.

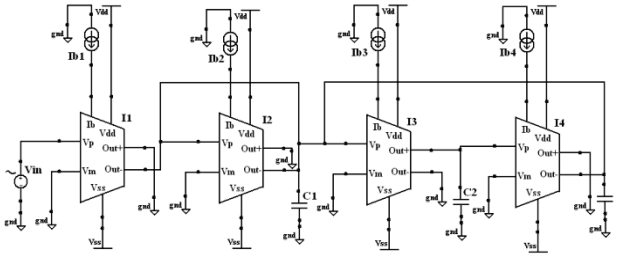

Fig. 4. Circuit schematic of the Gm-C biquad

It is made up by: voltage-to-current (V-I) converter, active resistor, capacitor, equivalent inductance: gyrator + capacitor. The V-I converter gain and the equivalent resistance and inductance values are all dependent on the OTA transconductance, and consequently, on the OTA bias currents: I_{b1} controls the gain of the input V-I converter; I_{b2} controls the equivalent resistance value; I_{b3} and I_{b4} control the equivalent inductance value. Thus, a control of the biquad behaviour is achieved by means of the bias currents, as shown in Table 3.

Table 3. Biquad parameter variance in respect to the OTA bias currents

Bias Current	Central Frequency	Bandwidth	Amplification
I_{b1} ↑	f_c _	BW ↑	A ↑
I_{b2} ↑	f_c _	BW ↑	A ↓↓
I_{b3} ↑	f_c ↑ slightly	BW _	A _
I_{b4} ↑	f_c ↑ slightly	BW _	A _

Rather than modifying all filter characteristics at once, as is the case of first order section cascade [10], the biquad permits independent tuning of parameters by means of the corresponding bias current. A higher precision and robustness for filter tuning is then achieved [11].

The division of a frequency band $[f_0, f_n]$ into n sub-bands is done by determining the boundary frequencies of each individual sub-band $[f_{l,i}, f_{h,i}]$, where f_l and f_h are the low and high boundary frequencies and subscript i shows the sub-band numbering. For a logarithmic spacing, the boundary frequencies are determined as [12]:

$$f_{l,i} = f_{m,i} \cdot \sqrt{q}\,, \quad (2)$$

$$f_{h,i} = \frac{f_{m,i}}{\sqrt{q}}\,, \quad (3)$$

where f_m is the mean frequency of the sub-band and q is determined as

$$q = \frac{f_{m,i+1}}{f_{m,i}}. \quad (4)$$

For a filter bank made up of 6 BPFs with logarithmic frequency spacing, the design specifications are determined with equations (2) and (3) and are listed in Table 4. To be noted that the central frequencies are taken from psycho-acoustic medical studies [13].

Table 4. Specifications of the 6 bandpass filters which build the filterbank for a logarithmic spacing

f_c [Hz]	Frequency range f_l–f_h [Hz]	BW [Hz]	Q
393	308 – 499	191	2
639	499 – 815	316	2
1037	815 – 1317	502	2
1685	1317 – 2140	823	2
2736	2140 – 3474	1334	2
4443	3474 – 5642	2168	2

For multi-channel CI signal processing applications, e.g. the CIS approach, medical studies show that 6th order Butterworth approximation filters are needed [13]. The 6th order filters are realized by cascading 3 biquad structures like the one from Fig. 4. The resulting filter schematic is shown in Fig. 5.

The central frequency of the Gm-C BPF is proportional to the g_m/C, i.e. I_{bias}/C ratio. Since the OTAs are biased in the subthreshold region, that is nA bias current levels, small capacitor values can be used. This makes a single-chip solution feasible.

To implement the filter specifications from Table 4, the needed bias currents and capacitor values are listed in Tables 5 and 6.

In Tables 5 and 6, the first numeric subscript shows the OTA numbering within the biquad, and, the second numeric subscript shows the biquad numbering within the 6th order BPF. If the second subscript is missing, then all corresponding bias currents are the same.

Table 5. The OTA bias currents needed to implement the BPFs from Table 4

Central Frequency [Hz]	393	639	1037	1685	2736	4443
I_{b1_1} [nA]	72	74	76	78	80	82
I_{b1_2} [nA]	45	47	49	51	53	55
I_{b1_3} [nA]	108	110	112	114	116	118
I_{c1} [nA]	10	9	8	7	6	5
I_{b2} [nA]	60	60	60	60	60	60
I_{c2} [nA]	10	10	10	10	10	10
I_{b3} [nA]	62	63	64	65	66	67
I_{b4} [nA]	62	63	64	65	66	67
I_{c3} [nA]	9	8.5	8	7.5	7	6.5
I_{c4} [nA]	9	8.5	8	7.5	7	6.5

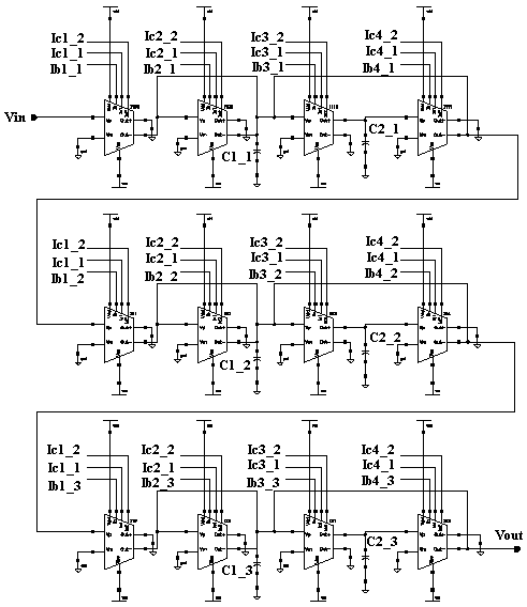

Fig. 5. The 6th order Butterworth approximation BPF schematic

Table 6. Capacitor values needed to implement the BPFs from Table 4.

Central Frequency [Hz]	393	639	1037	1685	2736	4443
C_{1_1} [pF]	9.18	5.56	3.48	2.14	1.31	0.812
C_{1_2} [pF]	5.57	3.42	2.11	1.3	0.8	0.492
C_{1_3} [pF]	14.1	8.7	5.36	3.3	2	1.25
C_{2_1} [pF]	5.48	3.37	2	1.27	0.787	0.484
C_{2_2} [pF]	13.9	8.56	5.27	3.24	2	1.23
C_{2_3} [pF]	8.45	5.2	3.2	1.97	1.21	0.747

Filter Programability

Programmability of the reconfigurable analog circuits refers to parameter tuning by means of digital control. This becomes a key feature in many useful applications.

The programmability principle is presented in figure 6 The digital control word $a_1...a_n$ is computed in the digital control block based on the current state of the analog signals and a number of other constraints. Both the input and output signals of the analog block can be used for parameter control. When the parameter control is done based on the input signal, we talk about Feedforward control. When the output signal is used for that purpose, we talk about Feedback control. The computation algorithm depends on the targeted overall application.

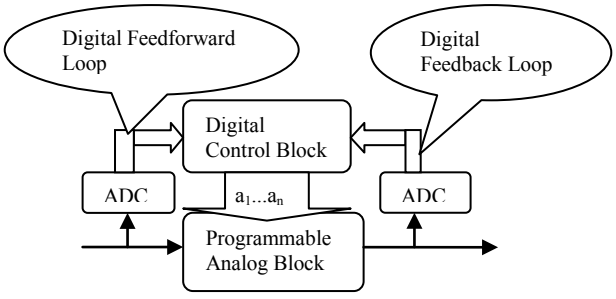

Fig. 6. The principle of programmability

As shown in tables 5 and 6, the analog filter structure parameters are controlled by corresponding bias currents and capacitor values. If the bias current is varied accordingly, any desired performance can be achieved within a certain range.

For the digital control of the bias currents, a Current Division Network (CDN) is used. The output current of the CDN is given by [14]:

$$I_{out} = \sum_{i=1}^{n} \overline{a_i} \cdot \frac{I_{in}}{2^i} \qquad (5)$$

and is a weighted sum of input current fractions. Whether or not a current fraction is added to the output current is decided by the control bit a_i. Thus, the CDN output current is controlled by a digital word $a=[a_n,\ldots,a_2,a_1]$.

The CDN consists of a cascade of Current Division Cells (CDC). Each CDC divides its input current and adds it to the output branch, considering the state of a pMOS switch. Another copy of the same divided current is fed to the next CDC for further division. The CDC schematic is shown in Fig. 7.

In the schematic from Fig. 7, the differential stage was used as a division element instead of a MOS divider to overcome limitations such as transistor matching and CDN length limitation [14]. Cascoding was used to increase the output resistance.

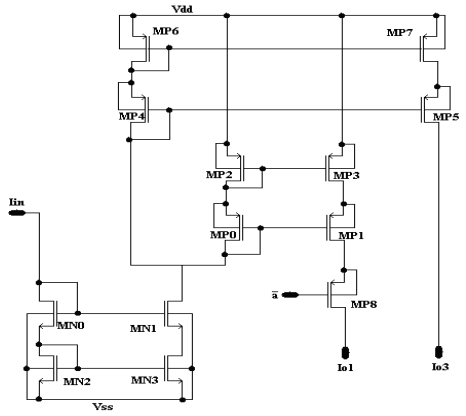

Fig. 7. Circuit schematic of a Current Division Cell

To source the bias currents from Table 4, a CDN with an 8-bit control word, that is, a cascade of 8 CDCs (CDN8) was implemented. The input current was set to 128 nA which gives a 0.5 nA resolution for the bias current adjustment. Thus, a digital tuning of the analog filter is achieved.

For programming the capacitor values, a capacitive array (CA) was implemented. An implementation of the CA is shown in Fig. 8.

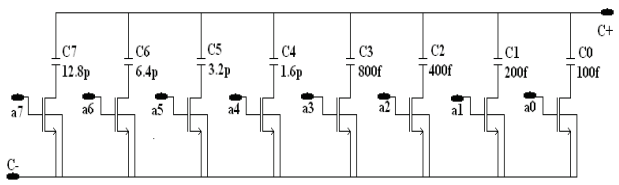

Fig. 8. Schematic of a possible implementation of the capacitive array (CA)

It can implement capacitor values up to 25.5 pF with a 100 fF resolution. The equivalent capacitor value is controlled by a digital word that is fed to nMOS switches. In order to reduce the switch on-resistance, wide nMOS transistors were used: $(W/L)_{nMOS}=100\mu/5\mu$.

To be noted is that the bias currents can only be used for tuning of the BPF, e.g. tuning of the central frequency, filter gain, etc. This is especially useful when fine adjustments need to be made. Changing the equivalent capacitor value however changes the whole filter characteristic, i.e. the central frequency. Considering the non-simultaneous fashion of the CIS stimulation, the whole filterbank can be implemented on a single filtering structure by using CAs.

Simulation Results

The proposed circuits have been implemented and simulated in CADENCE, using the AMS 0.35µm technology. The simulations were performed for differential V_{dd}=-V_{ss}=1.5V supply voltages.

Fig. 9 illustrates the V-I conversion characteristic of the subthreshold OTA for different bias currents. I_b was varied between 10 nA and 50 nA, while I_c was kept constant at 10nA. It can be noticed that for small bias currents, i.e. small OTA gain, the OTA linear range becomes limited again.

The biquad control, as stated in Table 2, is demonstrated in Fig. 10 and 11. The different bias currents were varied between 50nA and 70nA, with a 5nA step size. Fig. 10 illustrates the control of the filter gain by means of I_{b2}. Fig. 11 illustrates the control of the central frequency by means of I_{b3} and I_{b4}. Thus, the filter gain was varied around the 0dB level, and the central frequency was varied between 2kHz and 2.5kHz, achieving a digital filter tuning.

As shown in Fig. 10 and 11, and as stated above, the bias currents only permit a tuning of the filter parameters within a certain range. For considerable changes in the filter characteristic, e.g. to change the central frequency, the equivalent capacitance value of the CA needs to be varied. By doing so, the specifications of each BPF from Table 2 are achieved. The resulting amplitude characteristics are shown in Fig. 12.

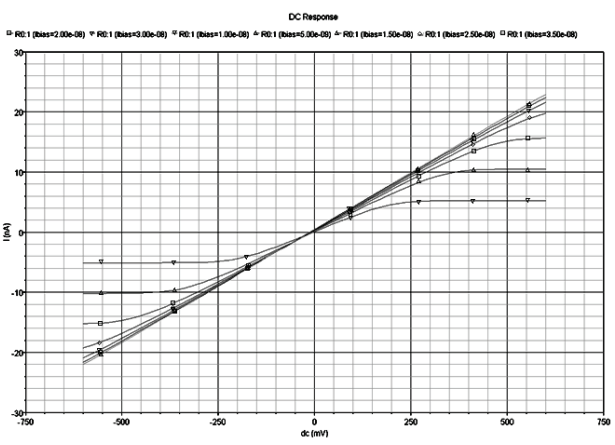

Fig. 9. Variation of the OTA gain in respect with the OTA bias current I_b

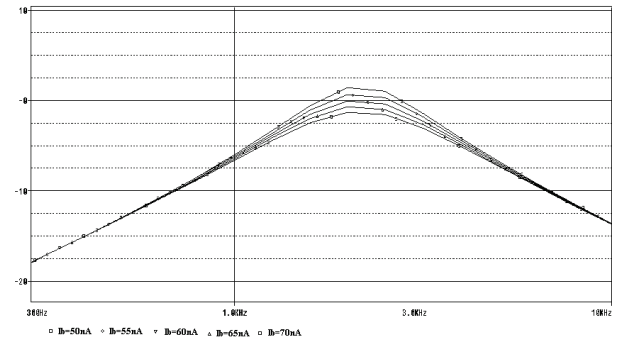

Fig. 10. Variation of the BPF gain in respect with the bias current I_{b2}

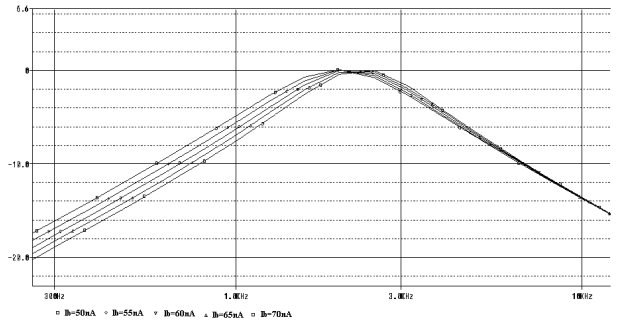

Fig. 11. Variation of the BPF central frequency in respect with the bias current I_{b3}

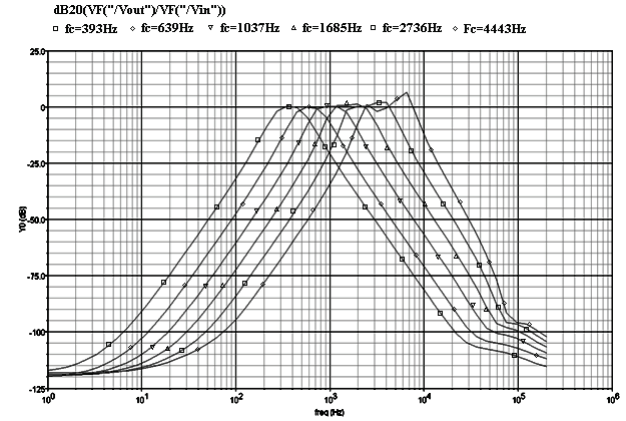

Fig. 12. The amplitude characteristics of the BPFs building the filterbank

Besides tuning of the filter parameters, bias currents I_{b1}, I_{b2}, I_{b3} and I_{b4} can also be used to achieve error compensation. As all bias currents are digitally controlled, the digital control loop can implement amplitude and frequency compensation schemes. This is particularly important in CI applications where good filter performance is crucial for quality sound perception. Testing and proving the efficiency of the digital tuning loop is subject to further simulations.

Conclusions

This paper presents the CMOS implementation of a fully reconfigurable BPF to be used in Cochlear Implant applications, suitable for the CIS processing strategy. The OTAs building the filter are biased in the subthreshold region, thus, reduced power consumption estimated in the μW domain is achieved.

The small capacitance values allow for a single-chip solution. A digital tuning of the BPF was proposed. Variation of the digital control word permits a fine tuning of the filter characteristic on one hand, and, the implementation of completely different filter characteristics on the other. The simulation results show the efficiency and effectiveness of the proposed digital control of the analog filter.

Acknowledgements

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Multichannel sound processing approaches are used in Cochlear Implant (CI) applications for increased performance. Filterbanks are required for this purpose. The implementation of a fully reconfigurable bandpass filter (BPF) with digital control is presented. Subthreshold transconductors (OTA) are used for lower power consumption and smaller capacitor values. The digital control of the OTA bias currents allows for a fine tuning of the BPF frequency characteristic. The full reconfigurability proves itself useful for non-simultaneous stimulation strategies. The BPF is implemented at transistor level. It covers the 300Hz-5.5kHz audio range and splits it into 6 logarithmically spaced channels. Simulations of the resulting circuit prove the efficiency of the digitally controlled reconfigurable analog blocks. Ill. 12, bibl. 14 (in English; summaries in English, Russian and Lithuanian).

С. Гхинтеа, П. Фараго, Л. Фэстила, П. Сиосер. Перестраиваемый фильтр для имплантируемого слухового протеза // Электроника и электротехника. – Каунас: Технология, 2010. – № 3(99). – С. 7–12.

Для повышения эффективности кохлеарных имплантатов (CI) используется многоканальная обработка звука. Для этой цели необходимы системы фильтров. Представлено осуществление полностью перестраиваемого полосового фильтра (BPF) с цифровым управлением. Подпороговые транскондукторы (OTA) используются для уменьшения энергопотребления и емкости конденсаторов. Цифровое управление токов OTA позволяет точно настроить частоты характеристики BPF. Полная реконфигурация полезная для не одновременного стимулирования. BPF реализован на транзисторном уровне. Он охватывает 300 Hz – 5,5 kHz звуковой диапазон и разбивает его на 6 логарифмически расположенных каналов. Моделирование созданой схемы доказало эффективность реконфигурируемых аналоговых блоков с цифровым управлением. Ил. 12, библ. 14 (на английском языке; рефераты на английском, русском и литовском яз.).

S. Hintea, P. Faragó, L. Festila, P. Söser. Klausos implantams skirto perderinamojo filtro projektavimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 3(99). – P. 7–12.

Klausos implantų efektyvumą galima padidinti daugiakanaliu garso apdorojimu. Šiam tikslui reikalingos filtrų sistemos. Aprašomas visiškai perderinamo skaitmeninio juostinio filtro (BPF) projektavimas. Energijos suvartojimui ir naudojamų kondensatorių talpai sumažinti naudojami OTA. Skaitmeninis OTA maitinimo srovių valdymas užtikrina tikslų dažninės BPF charakteristikos valdymą. Visiško perderinimo galimybė naudinga esant nevienalaikiam stimuliavimui. BPF sukurtas tranzistoriniu lygmeniu. Jis aprėpia 300 Hz–5,5 kHz garso diapazoną ir suskaido jį į 6 logaritmiškai išdėstytus kanalus. Sukurtosios schemos modeliavimas parodė, kad gaminys efektyviai naudojamas perderinamuosiuose analoginiuose skaitmeniniuose blokuose. Il. 12, bibl. 14 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).