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Orders Priorities Settings Criteria for Multifunctional Registers

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Introduction

Already are known methods for synthesis of FSM [1], complex digital automata with wired sequencers systems [2], [3], [4], using the multifunctional registers (MFR). In this paper, the authors propose an original method for designing and implementing a MFR register.
Let's consider a such digital register structure like in Fig. 1:

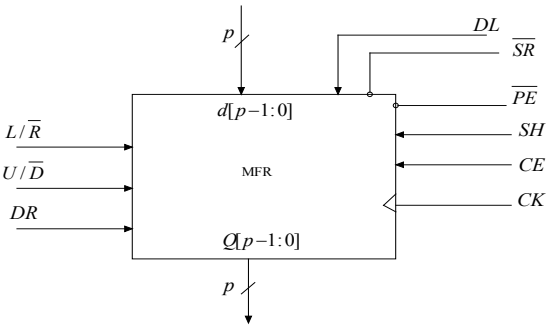

Fig. 1. MFR register

Input command signals:
- $\overline{SR}$, asynchronous reset (High Priority Level)
- $\overline{PE}$, Parallel Enable
- SH, logical shift
- CE, count enable (low priority level)

Data:
- $d[p-1:0]$, input data in parallel load mode
- DR, DL, serial input data, right shift, left shift

Conditional input data signals:
- $L/\overline{R}$ - fixed shifted direction ($L/\overline{R}=0$ – right shift, $L/\overline{R}=1$ – left shift)
- $U/\overline{D}$ – fixed binary count direction ($U/\overline{D}=0$ – decrement, $U/\overline{D}=1$ – increment)
- CK – clock input, active on positive edge signal

The thruth table of MFR is illustrated in Table 1:

Table 1. The MFR thruth table

Mode	$\overline{SR}$	$\overline{PE}$	SH	CE	$L/\overline{R}$	$U/\overline{D}$	CK	$Q[p-1:0]_{n+1}$
Hold	1	1	0	0	x	x	x	$Q[p-1:0]_n$
Reset	0	x	x	x	x	x	x	00…0
Parall –el Load	1	0	x	x	x	x	↑	$d[p-1:0]_n$
Shift Right	1	1	1	x	0	x	↑	$DRQ_{p-1}...Q_2Q_1$
Shift Left	1	1	1	x	1	x	↑	$Q_{p-2}Q_{p-3}...Q_0DL$
Count Down	1	1	0	1	x	0	↑	$[Q_n-1] \bmod 2^p$
Count Up	1	1	0	1	x	1	↑	$[Q_n+1] \bmod 2^p$

Taking account the signals inputs priority levels, the equations of D_i are, (1), (2):

$$D_i = \overline{SR}(PE \cdot d_i + \overline{PE}(SH(\overline{L/\overline{R}} \cdot Q_{i+1} + L/\overline{R} \cdot Q_{i-1}) + \overline{SH}(CE(\overline{U/\overline{D}} \cdot (\overline{Q_i} \oplus \varphi_i) + U/\overline{D} \cdot (Q_i \oplus \psi_i)) + + \overline{CE} \cdot Q_i))), \quad when \quad 1 \le i \le p-2, \tag{1}$$

here φ_i – represents the function of the "i" bit from the binary down counter; ψ_i – represents the function of the "i" bit from the binary up counter:

$$\begin{cases} \varphi_i = \prod_{k=0}^{i-1} \overline{Q_k}, \\ \psi_i = \prod_{k=0}^{i-1} Q_k, \\ \\ \varphi_i = \varphi_{i-1} \cdot \overline{Q_{i-1}}, \\ \psi_i = \psi_{i-1} \cdot Q_{i-1}, \\ \varphi_0 = \psi_0 = 1. \end{cases} \tag{2}$$

The reader can consider the (1) relation for D_0 and D_{p-1}, for the shift operations with DL and DR data signals.

A possible implementation is considered in Fig. 2.

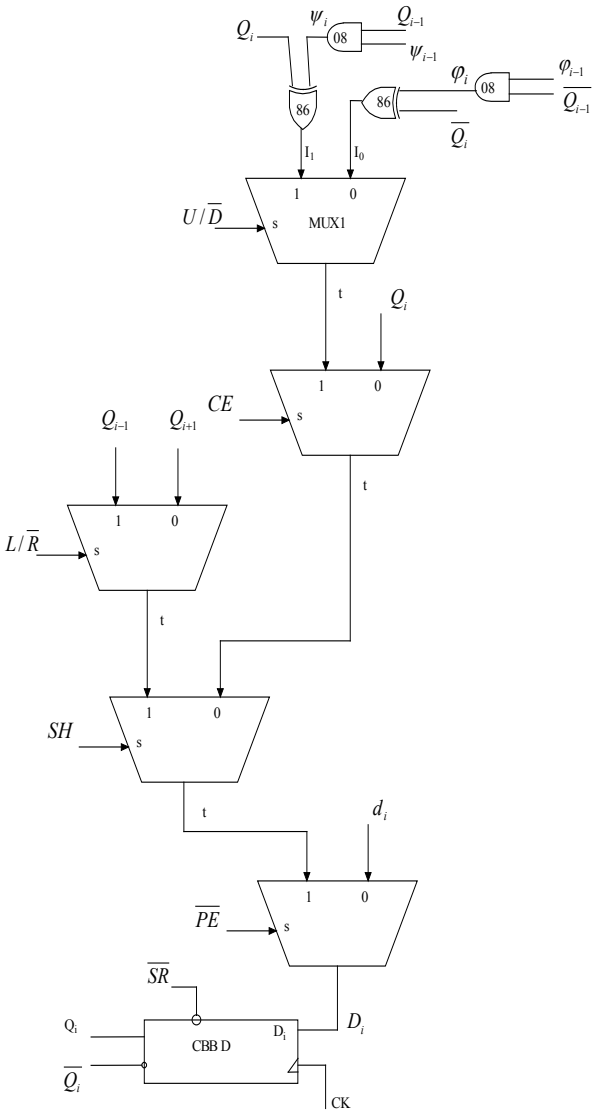

Fig. 2. Implementation of CLS from Table 1

The calculation of the minimum period (maximum frequency) **of the clock** (alternative 1 – according to the implementation of Fig. 2). Consider the multiplexer implemented with "buffers with three states" (SN74LS126A), [6], as in Fig. 3.

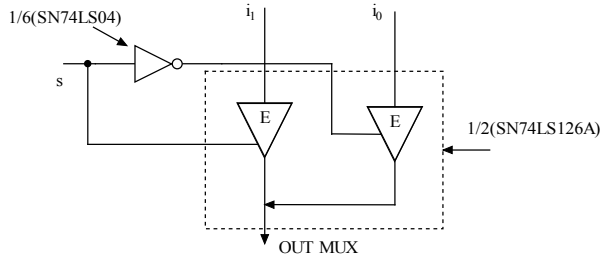

Fig. 3. Implementation with MUX 2x1

The equation of this multiplexer is

$$OUTMUX = i_1 s + i_0 \bar{s}. \quad (3)$$

We extract from the same component data book, [6], the following time parameters:

$$\overline{t_{pLH}}(MUX) = \overline{t_{pHL}}(MUX) = \overline{t_p}(MUX) = 15ns\,, \quad (4)$$

the propagation times from DATA INPUT to OUTMUX

$$\overline{t_p}(\varphi_i) = \overline{t_p}(\psi_i) = i \cdot \overline{t_p}(08) = 20i[ns]\,,\ \overline{t_p}(86) = 30ns\,. \quad (5)$$

It is used D flip–flop circuits, of type SN74LS74A, with the following parameters:

$$t_b = MAX[\overline{t_{pLH}}(Q), \overline{t_{pHL}}(Q)] = 40ns\,, \quad (6)$$

here t_b – the switching time.

$$\underline{t_{s-u}}(D) = 20ns\,, \quad (7)$$

here t_{s-u} – the set–up time.

We denote by $\underline{x}$, $\overline{x}$ – the minimum value, respectively the maximum value of the (x) magnitude. In Fig. 4 is illustrated a time diagram for the implementation from Fig. 2 (it was proposed the most unfavorable mode, "COUNT").

From condition of ensuring a minimum (t_{s-u}) is obtained

$$\begin{aligned}\underline{T_1} &= \underline{t_{s-u}}(D) + \overline{t_b} + \overline{t_p}(\varphi_i, \psi_i) + \overline{t_p}(86) + 4\overline{t_p}(MUX) = \\ &= \underline{t_{s-u}}(D) + \overline{t_b} + i\overline{t_p}(08) + \overline{t_p}(86) + 4\overline{t_p}(MUX).\end{aligned} \quad (8)$$

In the case of system implemented with 4 binary ranks (i = 4) and replacing in equation (5) values from equation (4) is obtained

$$\underline{T_1} = 230ns\,, \quad (\overline{f_1} \cong 4{,}35MHz)\,. \quad (9)$$

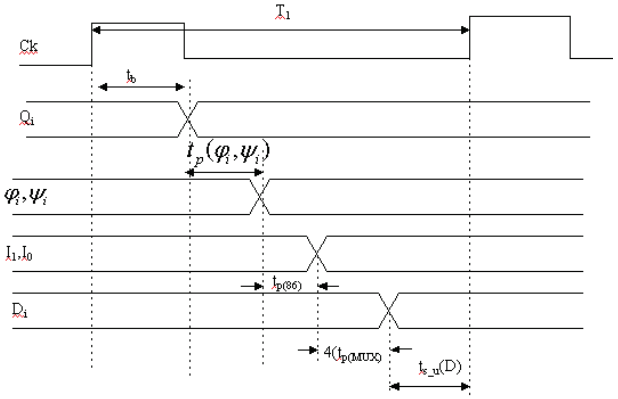

Fig. 4. The signal diagram for the most unfavorable case of the implementation from Fig. 3

The calculation of the minimum period (maximum frequency) **of the clock** (alternative 2). The alternative 2 of the synthesis / implementation will correspond to another order of priorities, for example: $\overline{SR}$ (High

Level), CE , SH , $\overline{PE}$ (Low Level). The table in Table. 2 represents the truth table for this case.

Table 2. The truth table (alternative 2)

Mode	$\overline{SR}$	CE	SH	$\overline{PE}$	$L/\overline{R}$	$U/\overline{D}$	CK	$Q[p-1:0]_{n+1}$
Hold	1	0	0	1	x	x	x	$Q[p-1:0]_n$
Reset	0	x	x	x	x	x	x	00…0
Cound Down	1	1	x	x	x	0	↑	$[Q_n-1] \bmod 2^p$
Count Up	1	1	x	x	x	1	↑	$[Q_n+1] \bmod 2^p$
Shift Right	1	0	1	x	0	x	↑	$DRQ_{p-1}...Q_2Q_1$
Shift Left	1	0	1	x	1	x	↑	$Q_{p-2}Q_{p-3}...Q_0DL$
Par. Load	1	0	0	0	x	x	↑	$d[p-1:0]_n$

The logical relation for the D_i data input of the D type circuits, according to the new order of priorities from equation (7), is implemented as in Fig. 7.

$$\begin{cases} D_i = \overline{SR}(CE(\overline{U/\overline{D}\cdot(\overline{Q_i}\oplus\varphi_i)}+U/\overline{D}, \\ (Q_i\oplus\psi_i))+\overline{CE}(SH(\overline{L/\overline{R}}\cdot Q_{i+1}+L/\overline{R}\cdot Q_{i-1})+ \\ +\overline{SH}(PE\cdot d_i+\overline{PE}\cdot Q_i))). \end{cases} \quad (10)$$

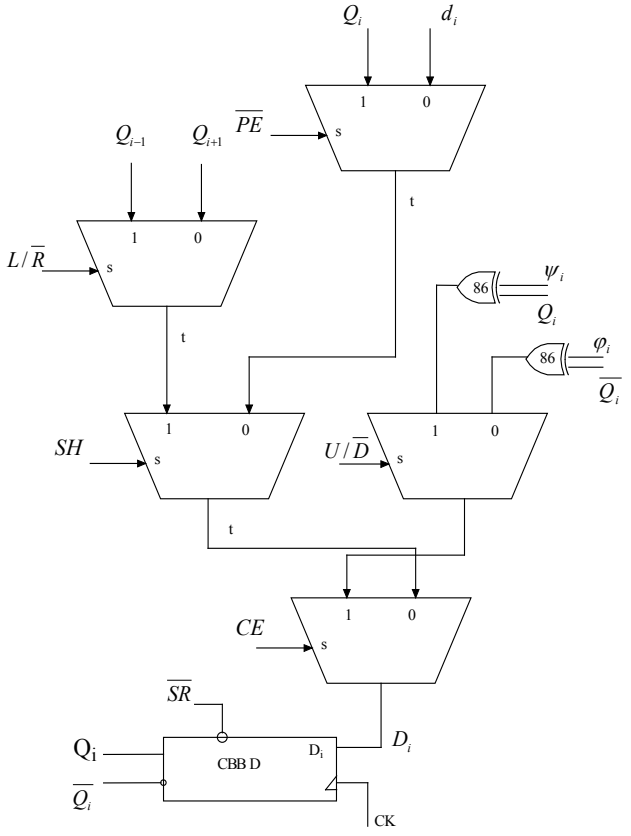

Fig. 5. The implementation according with table from Table 2

Using the same idea as in previous paragraph (2), it is obtained the minimal value of the clock (11)

$$\underline{T_2} = \underline{t_{s\_u}(D)} + \overline{t_b} + \overline{t_p}(\psi_i,\varphi_i) + \overline{t_p}(86) + \\ + 2\overline{t_p}(MUX) = 200n\sec(\overline{f_2} = 5MHz). \quad (11)$$

Considering a 4 bit binary number (i=4), the implementation was done with the same circuit types, [6]. It is obtained with the same hardware cost, with only modification of priorities orders for command signals, the minimal clock period was reduced from 230nsec to 200nsec or, the relative speed of the system was increased by 13 %

$$\Delta T\% = \frac{\Delta T\cdot 100}{\underline{T_1}} \cong 13\%. \quad (12)$$

Conclusions

From the minimal delay propagation of MFR synchronised clock signal, we have the conclusion that it depends by the command choosed priorities.

From the previous example, the most advantageous situation (maximal frequency) is when the maximal priority (after reset) is assigned to input command signal with minimal propagation time $(Q_i => D_i)$.

From the (8) and (11) relations, can be observed that when the MFR, (i), range number is increased, the relative values for speed $\Delta T\%$ decreases. As a conclusion, on a greater number of binary positions, the commands priorities order is no semnificative.

References

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This paper presents the further on researches which were done in [1], that is synthesis of digital systems using MFR (Multifunctional Register) with commands inputs signals synchronised with clock and scheduled priority setting signals. The authors proposed a new

method for setting the priority orders of the input command signals, thus the synchronization clock have the maximum frequency upper limit settings. Ill. 5, bibl. 5, tabl. 2 (in English; abstracts in English, Russian and Lithuanian).

Ал. Валачи, М. Тимис, Б. Эйгнэтоаи, С. Тарцау. Критерии параметров настройки приоритетов распоряжений для многофункциональных регистров // Электроника и электротехника. – Каунас: Технология, 2010. – № 4(100). – С. 87–90.

Описываются дальнейшая исследования синтеза цифровых систем на основе многофункциональных регистр с учетом команд входных сигналов, синхронизированными с часами и намеченными сигналами урегулирования приоритета. Предложили новый метод для урегулирования первоочередных заказов команды входных сигналов. Ил. 5, библ. 5, табл. 2 (на английском языке; рефераты на английском, русском и литовском яз.).

Al. Valachi, M. Timis, S. Tarcau, B. Aignatoaie. Parametrų kriterijų prioritetų nustatymas daugiafunkciame registre // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 4(100). – P. 87–90.

Pateikti atlikto tyrimo duomenys [1]. Skaitmeninėse sistemose naudojami daugiafunkciai registrai, kai įėjimo signalai sinchronizuojami su taktinių impulsų generatoriumi ir nustatytų prioritetų signalais. Pasiūlytas naujas metodas įvesties signalų prioritetų tvarkai nustatyti, sinchronizuojant didesniu taktinių impulsų dažniu už nustatytą ribinį. Il. 5, bibl. 5, lent. 2 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).