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Project-Oriented Approach to Low-Power Topics in Advanced Digital Design Course

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Introduction

Project-oriented approach to learning of digital design refers to any learning environment in which the problem drives the learning, because it is posed in such a way that students realize they need to acquire new knowledge before the problem can be solved [1]. We consider a problem of low-power synthesis of digital systems, which are described as a Finite State Machine (FSM). FSM is a widely recognized model used in digital system design. Our approach to digital design is based on an FSM decomposition that is one of the most important problems in discrete device synthesis. FSM decomposition is an essential topic for digital design education at Tallinn University of Technology (TUT). Decomposition problem is a task of substituting prototype FSM with a network of interconnected sub-FSMs, which has the same terminal behavior. A FSM can be decomposed into smaller interacting machines in order to archive different optimizations. In this paper, we apply decomposition technique (as a case study) to organize the network as a collection of alternatively working components, thus greatly reducing the switching activity of the circuit (dynamic power management).

To make a decision of decomposition task more tractable, corresponding CAD tools (called D&S system) were developed at TUT. The D&S software automatizes routine calculations and provides intuitive interface for experimenting with various methods of decomposition. Another tool, FSMNet (stands for Finite State Machine Network) Stochastic Explorer is a software, which can be used for investigation of FSM and FSM networks on behavioural level using different stochastic estimations. These stochastic estimations can then be successfully applied to making a choice and evaluating the most appropriate decomposition of the prototype FSM or state encoding problem. Both software environments are implemented using Java technology making them compatible with a wide range of operating systems and allowing a possibility for the remote access. Actually, D&S system presents interconnection of CAD tools with e-learning methodology.

The primary output of this work is the development of laboratory materials for students in digital system design. The primary goal in developing these materials is to provide the students with extensive hands-on opportunities to enhance their knowledge and understanding of advanced concepts and principles in designing low-power digital systems using FPGA technology. FPGA design has a much short design cycle, lower cost, and a smoother learning curve. In addition, FPGA devices are programmable and reprogrammable, which makes them reusable throughout the lab practices and excellent devices to test and investigate different design alternatives. The reprogrammable nature of FPGA makes them ideal for educational purposes as it allows students to iterate in their design tasks [2].

The tools, which are chosen to support the learning process, are easy to use and have a self-explaining interface. Therefore, they do not require an extensive learning curve and students can focus on their task right away. These tools also help to avoid routine actions and boring calculations, which are normally necessary for solving complex task-related problems.

Low-power design approaches

Power consumption has always be one of the primary concerns in the digital design. Low power consumption is essential to achieve longer autonomy for portable devices, e.g. mobile battery-powered systems where the lifetime of the battery decreases as the power consumption of integrated circuits and peripherals grows. Increasingly high circuit density and higher clock frequencies are creating heat dissipation problems. Huge effort are being invested to come up with design solutions that satisfy technical feasibility from a thermal profile standpoint and reduce the cost of the package and cooling means.

In CMOS circuits, power is consumed during charging and discharging of the load capacitances. Average power dissipation is proportional to the average

switching activity. A good approximation of the average switching activity is the switching probability. Probabilistic approaches have been recently receiving more attention as capable techniques for analysis of complex digital systems.

As a rule, the control part in the high-level representation of a digital system is characterized with a finite state machine (FSM). The transition structure of an FSM can be modeled with a Markov chain in order to study its probabilistic behavior, assuming the FSM description and the input probabilities are provided as well. The input probability distribution can be obtained by simulating the FSM at a higher level of abstraction in the context of its environment or by direct knowledge from the designer [3]. By labeling each outgoing edge of each state with the probability for the FSM to make that particular transition, a finite state model, that matches the definition of a discrete parameter Markov chain, can be obtained. The behavior of such Markov chain can be studied in order to obtain steady state probability distribution. This, in turn, would allow to build different kinds of quantitative estimations of FSM's stochastic behavior, which can be used for solving various problems in the area of low-power digital design.

In a high-level specification states of the FSM are represented with symbolic variables. As current digital circuits employ bistable storage elements, which can hold one of only two possible values, transformation of these abstract variables to physical implementation requires binary encoding. In other words, each symbolic variable should be replaced with a binary vector. The resultant circuit would greatly depend on the selected encoding, as it may affect area, performance, testability and power consumption among others.

The hardware implementation of the FSM generally consists of two main parts. One is a register, where state codes are stored. The other is combinational logic, which calculates the next state and outputs. Both parts serve as power dissipation sources. However, the dynamic power dissipation in the combinational part of the circuit is very difficult to estimate, even after the state encoding is determined [4]. Therefore, reduction of switching activity in the state register is often chosen as the primary optimization goal. Based on stochastic model of the FSM, the state assignment is obtained by minimizing the Hamming distance (number of bits by which two codes differ) between adjacent states with higher transition probability [5].

Minimizing the switching activity by modifying the state encoding of an FSM by itself does not always guarantee reduced total power dissipation, because the power consumed in the combinational part is not accounted for. Dynamic power management is a concept that includes various design methods and techniques, which are based on the principle of shutting down parts of the circuit that are not currently active. Sequential circuits have an extremely large number of reachable states, but probabilistic analysis may show that only a relatively small subset is actually being visited during normal operation (computational kernel). If such computational kernel does exist, it can be identified (by means of stochastic analysis) and separated from the rest of the circuit using the notion of additive decomposition.

Decomposition is essentially a problem of substituting prototype FSM with a network of interconnected sub-FSMs, which exhibit exactly the same behavior. The main idea of additive decomposition is the addition of a special "idle" state to each component sub-machine. When the sub-FSM is not in use, it transitions to idle state. Therefore, only one sub-machine in the decomposed network can be active at the same time, while others remain suspended (stay in "idle" state). Thus, there is no redundant switching activity present for non-working blocks (dynamic power management). As the computational kernel is very likely to remain active during majority of the operation time, the reduction of the overall switching activity may be expected.

CAD tools

Decomposition and Synthesis (D&S) software package [6] has been specifically designed for research and experiment with various decomposition methods. D&S environment provides the following features:

- An easy-to-use graphical user interface (GUI);
- Duplication of GUI modules by their command-line versions (currently, command-line tools are available for the following features: decomposition, partition search, random partition generation and checking the FSM specification.)
- Built-in libraries of FSM benchmarks;
- Ability to import the prototype FSM and to export either the whole decomposed sub-machine network or individual sub-FSMs in various formats (such as VHDL, BLIF, KISS2);
- Can be accessed over Internet or run locally;
- Help documentation that describes theoretical background and contains manuals;
- Lots of examples.

In order to analyze the stochastic behavior of the FSM, it can be modeled with a Markov chain. Then any stochastic property of an FSM can be considered as such of the underlying Markov chain model. FSMNet Stochastic Explorer tool can be used for computation of different stochastic estimations of FSM and FSM networks with specified precision and rounding schemes. FSM description is specified using Berkley KISS2 format. FSMNet Stochastic Explorer allows automatic generation of input pattern probabilities on basis of known input signal probabilities for a given FSM. FSMNet Stochastic Explorer serves as a supplementary tool for the decomposition and synthesis system.

Since both tools have been developed using Sun Java platform, the range of operating systems where the programs can be executed is limited only by availability of Java Runtime Environment. Furthermore, Java provides capabilities to run programs (applets) inside standard browsers, which offers possibility for the remote access over the Internet. The only drawback is that the web-based part is subjected to some use limitations (for example, some applets are not allowed to save the results of user's work on the local computer).

FPGAs in digital design education

Digital design courses are offered at technical universities throughout the world. However, there is still an extensive search over the best way to organize them. In recent years, the practical part of digital design courses was taught mostly with simulation-based approach. Building of a custom VLSI prototype involves high costs and lengthy fabrication delays, which make this method unsuitable for hardware verification. The FPGA technology provides an attractive alternative. Low-cost FPGA-based development boards reduce costs due to hardware reusability and offer fast design cycles.

Digital circuit design is about making trade-offs like area vs power consumption. Students become aware of these trade-offs during actual hardware implementation of the project. Although, FPGA design flow may not be directly related to custom silicon prototyping, students would still have to evaluate and partition design, manage trade-offs, locate bottlenecks, etc.

Until recently the FPGA-based development boards have not been a commonly used practice at TUT. Now such devices are extensively employed to support the practical part of the various digital design courses taught to undergraduate and postgraduate students.

Digital design laboratory is equipped with different models of the development boards, featuring FPGA devices from Xilinx and Altera, two of the leading programmable logic devices manufacturers. Boards also carry a wide range of industry standard interconnections, memory subsystems and expansion headers. All the necessary software is provided by the FPGA manufacturer: Integrated Software Environment (ISE) for Xilinx devices and Quartus-II for Altera devices. These design suites allow to perform all steps of the FPGA design flow (design entry, simulation, synthesis, translation and device configuration). Students may continue working on projects outside university, as both manufacturers provide free versions of their design suites, which can be downloaded from the Internet.

Case study

Consider an example FSM (“opus” from LGSynth’93 benchmark set) with steady state probability distribution as summarized in Table 1, which has been calculated using FSMNet Stochastic Explorer tool. It is easily seen that FSM spends 83% of its operation time in states “init0” and “init1”. Therefore, these states should form the computational kernel. The resultant computational kernel is a rather simple sub-FSM with three states (including “idle” state). Undoubtedly, it should consume considerably less power than original FSM does, as for the most part computational kernel is going to remain an active component.

Decomposed network for example FSM consists of two component FSMs. The first component represents the computational kernel and works alternatively with component the second component. In order to ensure a proper transfer of control, components have to exchange information using so-called internal variables. Whenever one sub-FSM is about to make a transition to “idle” state, it should pass information about its current state to other components in the network via additional output. This information is necessary to determine which sub-FSM gains the control and to which state it should move to.

Table 1. Steady state probability distribution of the example FSM

State	Steady State Probability	State	Steady State Probability
init0	0.5000001408	read0	0.0006720432
init1	0.3346775136	write0	0.0006720432
init2	0.0877016376	RMACK	0.0006720432
init4	0.0584677584	WMACK	0.0006720432
IOwait	0.0161290368	read1	0.0003360216

VHDL description for prototype FSM and decomposed network can be generated by decomposition applet. This description can be used to implement and verify both designs using FPGA-based development board using Xilinx Integrated Software Environment 11 (ISE). Implementation of the design completes with the generation of a report, which presents resource usage, timing and power estimations. This data can be used to evaluate the quality of the practiced technique or method.

The optimization can be measured in terms of a cost function. The employed power-oriented cost function considers the Hamming distance between adjacent state codes, as well as the probability of making that particular transition. It is assumed, that there is no difference between transitions from logic '1' to logic '0' or vice versa. Therefore, state transitions may be considered undirected. Then, the encoding defect can be measured as a ratio of cost function values for the received encoding to the perfect encoding. The desired encoding can be added to VHDL description after it is obtained.

In order to estimate the impact of the proposed techniques on power consumption, Xilinx Integrated Software Environment (ISE) 11 was used for carrying out FPGA design flow with Spartan-3 family FPGA being set as the target device. Xilinx Integrated Software Environment allows to employ different state assignment algorithms (along with user-defined encoding). Power consumption estimation was received using XPower Analyzer tool. The default settings for the switching rate of inputs were used. The frequency of clock signal was set to 50MHz. Only the dynamic power component was considered, as it has been the target of minimization.

As it is seen from Table 2, the dynamic power consumption (in mW) has been reduced by 60% for decomposed design with area overhead of 44%. Application of low-power state encoding yielded 57% power reduction with area overhead of 31%.

Table 2. Implementation results

Design	Power Consumption	Power Reduction	Area Overhead
Original (Auto)	4,68	–	–
Decomposition	1,85	-60%	44%
Encoding	2,01	-57%	31%

Conclusions

Our concept for teaching digital design includes problem-based approach as well as possibilities for "learning by doing". The tools, which are chosen to support the learning process, are easy to use and have a self-explaining interface. Therefore, they do not require an extensive learning curve and students can focus on their task right away. These tools also help to avoid routine actions and boring calculations, which are normally necessary for solving complex task-related problems.

FPGA-based development boards are low-cost and powerful educational tools for prototyping and development of digital systems. The use of FPGA technology in digital design education can add a certain level of realism to the learning experience. Apart from extensive simulation and synthesis, it would be possible to perform a final verification on a hardware prototype. And it may simply help to boost students' motivation, as they see their ideas get actually implemented and working. Also, FPGA design suites can be freely downloaded from the Internet, which permits to continue working on projects outside university.

The D&S system and FSMNet Stochastic Explorer, which have been developed at TUT, provide the essential software environment for education and research in the area of FSM decomposition and stochastic analysis of FSMs. Both tools can be easily used for educational purposes because of their interactive nature and user-friendly interface. Another advantage is that both can be accessed from all over the world using the Internet. Due to built-in support of widespread data formats, the experiments can be carried out on the range of well-known benchmarks of FSMs as well as on user-defined FSMs. The results of experiments can be exported to other CAD-related software for hardware verification.

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We consider a problem of low-power synthesis of digital systems, which are described as a Finite State Machine (FSM). In this paper, we apply FSM decomposition technique to organize the network as a collection of alternatively working components, thus greatly reducing the switching activity of the circuit (dynamic power management). To make a decision of decomposition task more tractable, corresponding CAD tools were developed at Tallinn University of Technology. Software tools are implemented using Java technology making them compatible with a wide range of operating systems and allowing a possibility for the remote access. Actually, developed system presents interconnection of CAD tools with e-learning methodology. The primary output of this work is the development of laboratory environment that provides students with extensive hands-on opportunities to enhance their knowledge and understanding of advanced concepts and principles in low-power digital design using FPGA technology and FPGA design suits. This can add a certain level of realism to the learning experience and helps to boost student's motivation. Bibl. 6, tabl. 1 (in English; abstracts in English, Russian and Lithuanian).

Д. Михайлов, Ф. Суднисон, М. Круюс. Исследование дискретного проектирования при изучении сетей малой мощности // Электроника и электротехника. – Каунас: Технология, 2010. – № 6(102). – С. 151–154.

Рассматривается проблема декомпозиционного проектирования сетей конечных автоматов с оптимизацией потребляемой мощности. Метод синтеза ориентирован на реализацию на базе программируемых пользователем вентильных матриц. Разработана программная среда с привлечением технологий позволяющих удалённый доступ через Интернет с использованием различных операционных систем. Разработка внедренна в учебный процесс в Таллиннском технологическом университете и успешно освоена студентами. Библ. 6, табл. 1 (на английском языке; рефераты на английском, русском и литовском яз.).

D. Mihhailov, A. Sudnitson, M. Kruus. Skaitmeninio projektavimo kurso, taikomo mažos galios tinklų tematikoje, tyrimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 6(102). – P. 151–154.

Apžvelgtas skaitmeninio projektavimo kursas ir jo svarba mažos galios tinklų tematikoje. Mažos galios tinkluose skaitmeninės sistemos traktuojamos kaip baigtinės būsenos mechanizmai (BBM). Dekompozicijos užduoties sprendimui palengvinti Talino technologijos universitete buvo sukurta atitinkama programinė įranga (CAD). Programinei įrangai diegti buvo pritaikyta „Java" technologija. Dėl to pavyko išvengti nesuderinamumo su įvairiomis operacinėmis sistemomis, atsirado galimybė dirbti naudojantis nutolusiais kompiuteriais. Sukurta laboratorinė aplinka, leidžianti studentams gilinti savo žinias ir skaitmeninio projektavimo supratimą. Ši sistema rodo, kaip CAD įrankiai diegiami į e.mokymąsi. Visa tai didina studentų motyvaciją.. Bibl. 6, lent. 1 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).