ELECTRONICS AND ELECTRICAL ENGINEERING

ISSN 1392 – 1215 *2010. Nr. 8(104)*

ELEKTRONIKA IR ELEKTROTECHNIKA

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The Adequate Selection Algorithm by Estimating Local Oxide Influence

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Introduction

The characteristics of the element during the formation of integrated elements of integrated structure intended to not impair. In this case the manufacture of integrated circuits focuses on the area where the integrated element is being formed. It is essential that the area dimensions at the beginning of the technological processes must be kept the same during the whole technological process. The main aim is to maintain unchanged characteristics of the three-dimensional structure using local oxidation technology for isolation of integrated elements and to verify if the three-dimensional integrated element fits into the integrated circuits. In essence the designers of technological processes, manufacturers and researchers do not mention this stage of technological process and the methods (or algorithms) used to their rationalization [1]. Minimizing the cost of production processes is useful to create the adequate selection algorithm of the three-dimensional field-effect transistor in the three-dimensional integrated circuits by estimating local oxide influence, the realization of which is based on created mathematical models and their adaptation for the simulation.

During oxidation impurities in a integrated circuit can change its electrical, chemical, and even mechanical properties [2]. Oxidation as thermodynamic processes could be described using finite element method [1, 3–5]. The method is widely applicable, because simulated structure can be presented both in two and three-dimensional space. In this method seeks to maintain the minimum transitional zone (usually the transition zone is limited by one element).

The main objective of this paper is to examine and evaluate the adequate selection of the three-dimensional integrated element in the three-dimensional integrated circuits, modeling of the thermal oxidation using mathematical models. Rational parameters of local oxidation process in the three-dimensional structures are defined in [1].

Algorithm of the three-dimensional field-effect transistor of the adequate selection in the integral three-dimensional structure by estimating local oxide influence

ATHENA program of mathematical simulation software package TCAD is used for mathematical structures simulation [6]. It is adapted to the specific case of simulation using subprograms.

Mathematical structures are created using the finite element method for local thermal oxidation process simulation [3]. As mentioned in [3] mathematical structures consist of a silicon substrate (thickness – 0,8 μm), crystallographic plane orientation <100>, a silicon oxide (thickness – 0,02 μm) and silicon nitride (thickness – 0,1 μm). The area (1,2 μm) committed for the three-dimensional integrated element and areas for thermal oxide are formed [1]. Another mathematical structure is created for the fully recessed local thermal oxidation process with etched 0,3 μm deep cavity (length – 0,9 mm). The area (1,2 μm) committed for the three-dimensional integrated element is formed [4].

Local oxide profile is influenced by time and temperature of the process, the thickness of nitride mask and SiO_2 leading to the specific parameters of the integrated elements. Each of these parameters affects the type of LOCOS formation, stress distribution, lift-up nitride mask, lateral oxide under the silicon nitride mask, thin oxide form in the three-dimensional structures. Simulation was carried out in accordance with the model structure [3]. It was found during the modeling using program ATHENA that rational parameters of the thermal process creating the LOCOS in the three-dimensional integrated structures are t=90 min, T=1100 ºC, SiO_2=0,02 μm, Si_3N_4=0,1 μm. They allow to increase the integration degree, quick-action, reduce parasitic capacitances, the stresses, create maximum useful length in the three-dimensional integrated structures [1, 7, 8].

It is important to avoid distortion of integrated elements in the three dimensional integrated circuits. In

this case mathematical models are created implementing three-dimensional field effect transistors (MOS and V-MOS) [3, 7, 9] and assessing the adequate selection of the three-dimensional integrated element in the three-dimensional integrated circuits (Fig. 1). It evaluates the variation of characteristics during local thermal oxidation process. The source and drain areas occupy 0.35 µm each, the channel length – 0,5 µm [4, 7].

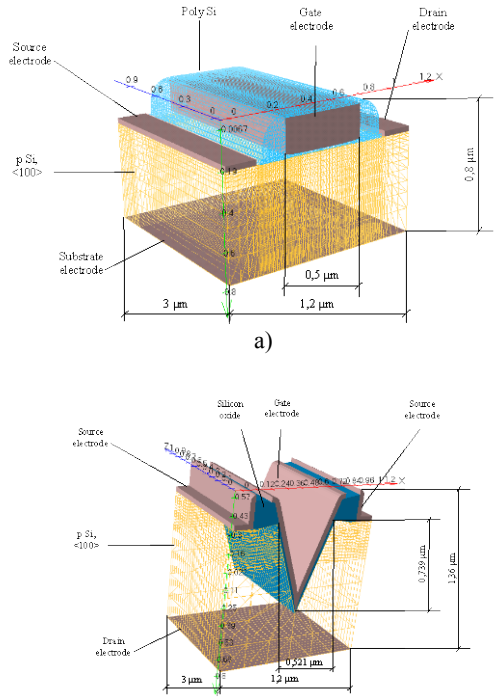

Fig. 1. Transistor mathematical models: a – MOS; b – V-MOS

The channel is formed in accordance with entire “V” perimeter in the V-MOSFET mathematical model. In the same area the three-dimensional structure of V-MOS mathematical model is formed, the channel length is up to 0,2 µm. The three-dimensional "V" groove depth is 0,739 µm and length – 0,521 µm.

The parameters of three-dimensional integrated element and three-dimensional integrated structure changes due the thermal technology, whose are difficult to identify and evaluate during the production. In this case the major human and material resources required, that’s why a mathematical simulation of technological processes adapting methods is used.

The results of simulation have been carried out in the three-dimensional integrated structure modeling (Fig. 2), when transistor (Fig. 1., a) is simulated between local oxides [3].

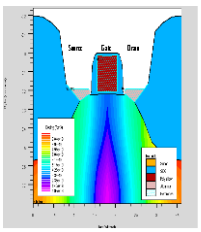

Fig. 2. Field-effect two-dimensional transistor in the integrated structure

Three-dimensional V-MOS transistor (Fig. 1) is used in order to avoid regions redistribution and increase the escarpment of transistor characteristics. The drain current of the transistor determines the channel area, a three-dimensional V-MOS structures can be used to power integrated structures, light emitting busy diodes, indicators and even low-power engines. Another advantage of the three-dimensional V-MOS technology is the savings of about 40% of the area compare to three-dimensional NMOS technology.

Using V-MOS less opportunities to redistribute impurities in source and drain regions appear during the thermal oxidation process, since the transistor drain current determine the length of the channel in the "V" shaped groove. According to the areas of redistribution in NMOS, the formation of a three-dimensional V-MOS in the three-dimensional structure is simulated (Fig. 3).

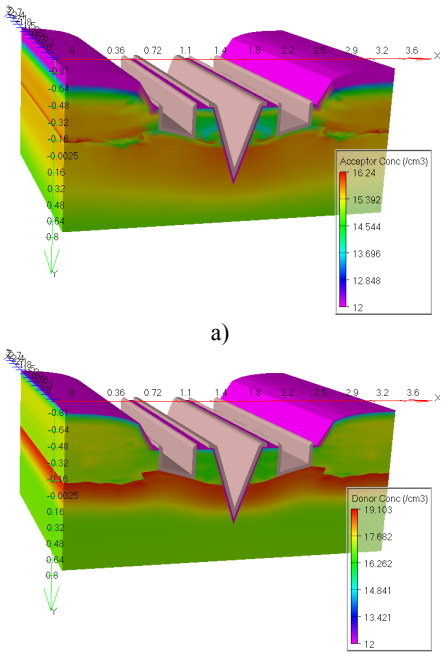

Fig. 3. Acceptor (a) and donor (b) concentration in three-dimensional integrated structures with V-MOS transistor structure

In the case of impurity distribution and movement of pn areas it was received that the most impurities were redistributed after three-dimensional thermal oxide formation processes. It was found out that during the thermal oxidation process impurities move into the lower doped layers in the three-dimensional integrated structures.

The redistribution of acceptors and donors in much larger volume during the formation of three-dimensional integrated structure using the local oxidation process formation was received. This is the result of thermal oxidation. Here acceptors were redistributed below the "V" shaped groove. Possible solution – a deeper "V" groove, but in this way largest groove increases not only the depth, but also the width which reduce the degree of integration

Redistribution of impurities in the thermal process is very important for the production of three dimensional integrated structures of increasingly higher integration degree, impurities move to other areas or redistribute

because of the thermal process, error occurs in the formed areas. So the three-dimensional field-effect transistor adequate selection algorithm in the integral three-dimensional structure which estimates local oxide influence is created.

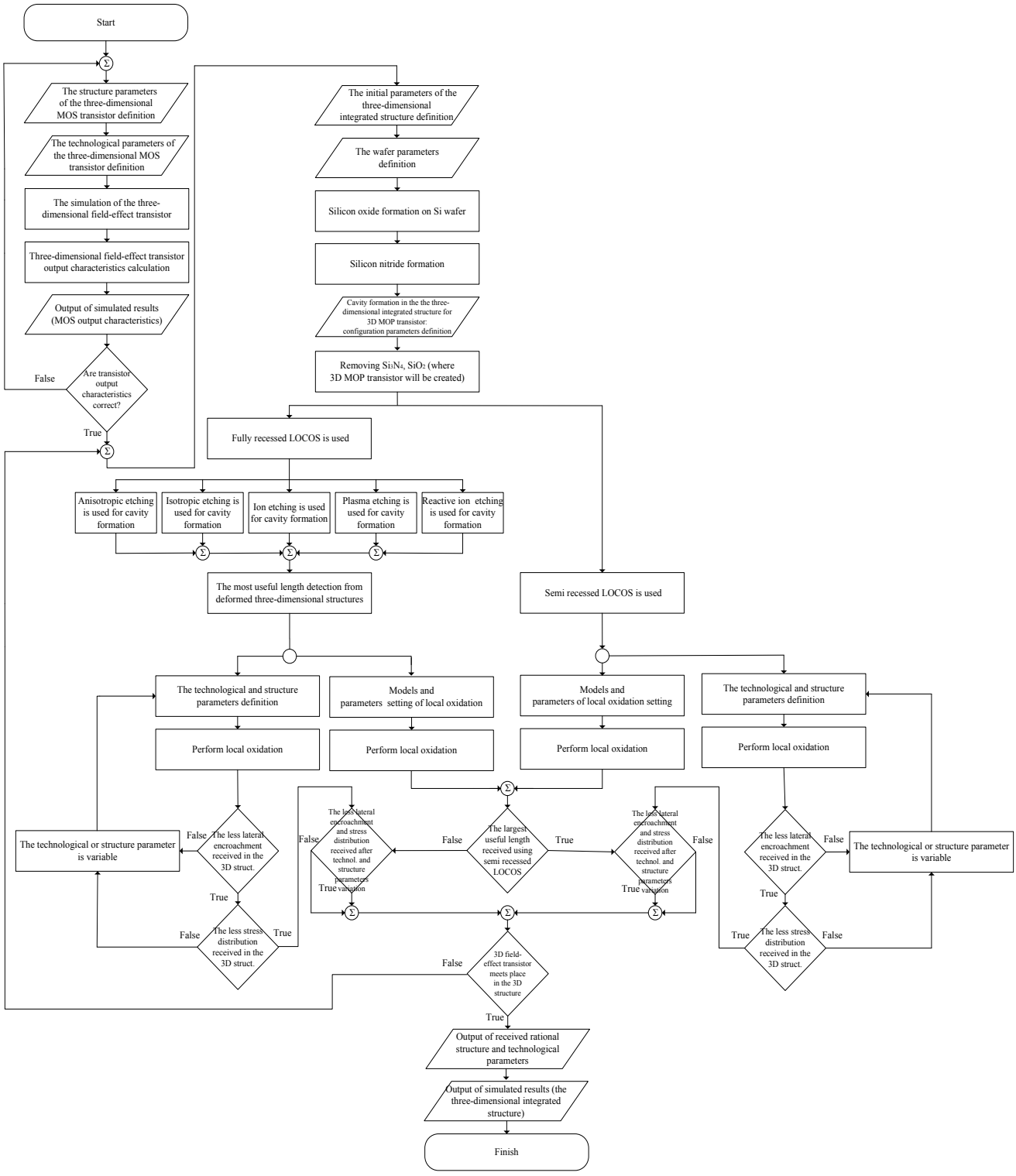

Fig. 4. The three-dimensional field-effect transistor adequate selection algorithm in the integral three-dimensional structure

Conclusions

- It was found out that during the thermal oxidation process impurities move into the lower doped layers in the three-dimensional integrated structures.
- The three-dimensional field-effect transistor adequate selection algorithm in the integral three-dimensional structure which estimates local oxide influence is created.
- The algorithm estimates etching technologies, local oxidation process, and rational parameters

and has feedback to other technological processes stages.

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Received 2010 06 28

D. Andriukaitis. The Adequate Selection Algorithm by Estimating Local Oxide Influence // Electronics and Electrical Engineering. – Kaunas: Technologija, 2010. – No. 8(104). – P. 39–42.

During oxidation impurities in a integrated circuit can change its electrical, chemical, and even mechanical properties. Redistribution of impurities in the thermal process is very important for the production of three dimensional integrated structures of increasingly higher integration degree, impurities move to other areas or redistribute because of the thermal process, error occurs in the formed areas. The three-dimensional field-effect transistor adequate selection algorithm in the integral three-dimensional structure which estimates local oxide influence is created. The algorithm estimates etching technologies, local oxidation process, and rational parameters and has feedback to other technological processes stages. Ill. 4, bibl. 9 (in English; summaries in English, Russian and Lithuanian).

Д. Андрюкайтис. Алгоритм уступчивости интегрального элемента в интегральной структуре, оценивающий локальный процесс окисления // Электроника и электротехника. – Каунас: Технология, 2010. – № 8(104). – С. 39–42.

Примеси в процессе окисления могут изменят электрические, химические и даже механические свойства. Перераспределения примесей после термических процессов наиболее важны при больших уровнях интеграции микросхем. Из-за этого возникают геометрические погрешности формируемых структур. Создан интегральный элемент оценки уступчивости алгоритма интегральной структуры, который позволяет оценить локальный процесс окисления на МОП транзистора в интегральной структуре, и установлены рациональные параметры при моделировании процесса оксидирования. Ил. 4, библ. 9 (на английском языке; рефераты на английском, русском и литовском яз.).

D. Andriukaitis. Integrinio elemento atitikties integrinei struktūrai algoritmo, įvertinčio lokalinės oksidacijos proceso įtaką, sudarymas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 8(104). – P. 39–42.

Oksidacijos metu priemaišos gali pakeisti integrinės struktūros elektrines, chemines ar net mechanines savybes. Priemaišų persiskirstymas po terminio proceso turi labai didelę reikšmę gaminant vis didesnio integracijos laipsnio trimačius integrinius grandynus, nes dėl terminių procesų priemaišos difunduoja, persiskirsto, atsiranda formuojamų sričių paklaidų. Sukurtas integrinio elemento įvertinimo atitikties integrinei struktūrai algoritmas, kuris leidžia įvertinti trimatės lokalinės oksidacijos proceso įtaką formuojant lauko tranzistorių trimatėje integrinėje struktūroje ir modeliuojant nustatyti terminės oksidacijos proceso racionaliausius parametrus. Il. 4, bibl. 9 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).

DOI: 10.5755/j02.eie.9223