ELECTRONICS AND ELECTRICAL ENGINEERING
ISSN 1392 – 1215 *2010. No. 9(105)*
ELEKTRONIKA IR ELEKTROTECHNIKA

ELECTRONICS
T 170
ELEKTRONIKA

Efficiency Increase of Switched Mode Power Supply through Optimization of Transistor's Commutation Mode

P. Špánik, M. Frivaldský, P. Drgoňa, J. Kandráč
Department of Mechatronics and Electronics, Faculty of Electrotechnical Engineering, University of Žilina, Univerzitná 1, 010 21 Žilina, Slovak Republic, e–mail: frivaldsky@fel.uniza.sk

Introduction

Nowadays, the main stream in the field of power semiconductor devices is concentrated on continual improvements of static, dynamic, thermal properties. This fact is reflected in research and application of new materials (SiC, GaN), which should be suited for semiconductors manufacture. Also new IEC standards are being constantly tightened, what is in the final result reflected in the designing of "EcoSmart" and "green" solutions. One of the merits is efficiency of power supplies, which has to be always as higher as possible. There are several ways how to eliminate almost all of the losses of power semiconductor devices, whereby one way is to utilize soft–switching technique, second way is to utilize the progressive semiconductor structures. Nevertheless to reach a compromise between switching frequency, efficiency and output power, the optimization of parameters, which influence transistor's commutation mode, is necessary. The first step in optimization consists in commutation mode selection. The second step is checking out general parameters of the selected mode e.g. dead–time, slope grows of current/voltage, gate resistor, auxiliary capacitance to find influence on switching losses at various switching frequencies. A perfect way of investigation could be the experimental analysis; nevertheless simulation analysis should demonstrate an overview of acceptable semiconductor switching losses for the selected transistor and target application.

Energy balance of commutation process of power transistor

Due to existence of feedback between rise/fall of transistor's voltage U_{DS} and fall/rise of transistor's current I_D the generation of power loss come into being. The analytical expression for total amount of power loss which is generated during one switching cycle is

$$P_{TOT} = \frac{1}{T}W_{ON} + \frac{1}{T}W_{COND} + \frac{1}{T}W_{OF} + \frac{1}{T}W_{OFF}, \quad (1)$$

where W_{ON} – energy absorbed during turn – on process; W_{COND} – energy absorbed during conduction time; W_{OF} – energy absorbed during turn – of process; W_{OFF} – energy absorbed during off – state; T – time period.

During computation of each part of losses next equations have been used.

$$P_{OFF(ON)} = \frac{1}{T}\cdot W_{OFF(ON)} = \frac{1}{T}.\int i_P(t)\,u_P(t)\,dt = \sum_{i=T_{Z1}}^{T_{Z2}} I_P[i]U_P[i]\Delta T, \quad (2)$$

where $i_P(t)$ – time function of transistor's current; $u_P(t)$ – time function of transistor's voltage; T_{Z1} – sequence of sample at the begin of transistor's turn–on/turn–off process; T_{Z2} – sequence of sample at the end of transistor's turn–on/turn–off process; $I_P[i]$ – i^{th} sample of transistor's current; $U_P[i]$ – i^{th} sample of transistor's voltage; ΔT – sampling time.

To find best commutation mode for selected transistor, the investigation is first executed by simulation analysis of most well known switching technique, which are hard switching, ZVS and ZCS.

Simulation analysis of selected commutation techniques

The aim of this chapter is to compare and evaluate processes during switching action of power transistor at various settings of switching mode parameters. Because of that each commutation mode requires specific behavior of circuit, the circuit simulation models were adapted to fulfill this requirement and meet the reality and authenticity of target application. Next figures show principal schematics of testing circuits which have been used in simulation environment.

The simulation analysis of hard switching technique is realized by circuit that is shown on Fig. 1, which represents replacement scheme for the investigation of dynamic characteristics of power transistors or diodes. Thus in this way it is possible to make parametrical analysis with the change of components which are influencing dynamic characteristics [2, 3, 5, 11].

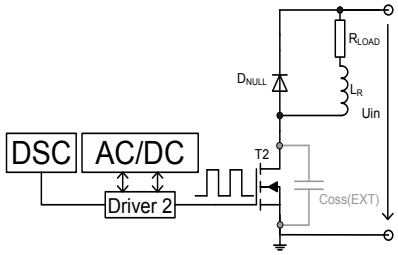

Fig. 1. Principal scheme for HS technique analysis

Parameters of simulation: U_{IN} = 325 V, I_{LOAD} = 10 A, R_{GATE} = 33 Ω, slope of current rise di/dt = 250 A/us, f_{SW} = 100 kHz.

Table 1. Power losses (hard switching technique)

	P_{ON} [W]	P_{OF} [W]	$P_{ON} + P_{OF}$ [W]
IPW60R165CP	19,5	14	33,5

The results of hard switching mode are listed in Table 1. The amount of turn – on losses is highly dependent on type of D_{NULL}. Turn – of losses are mostly dependent on dynamic behavior of transistor or/and on gate drive circuit.

The simulation analysis of zero voltage switching technique is realized by circuit that is shown on Fig. 2. The main leg consists of transistors which were subjected to analysis. The load is presented by series resonant circuit (C_R, L_R, and R_{LOAD}). The only part of power losses in ZVS commutation mode are turn – of losses as turn – on losses are null due to switching of transistor at zero voltage.

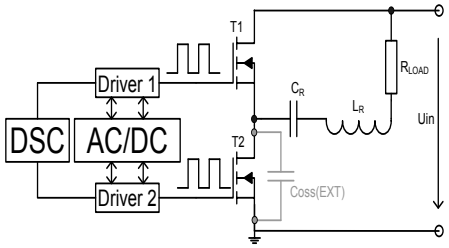

Fig. 2. Principal scheme for ZVS technique analysis

During simulation experiment of ZVS turn – of process the auxiliary capacitance has been connected in parallel to analyzed transistor for securing the ZVS conditions. For parametric evaluation of ZVS turn – of process variable parameter were dead time (t_D) and auxiliary capacitance (C_{OSSAUX}).

Parameters of simulation: Constant parameters: U_{IN} = 325 V, I_{LOAD} = 10 A, R_{GATE} = 20 Ω, f_{SW} = 100 kHz. Variable parameters: t_D = 300ns, 500ns, C_{OSSAUX} = 0nF, 1nF

Table 2. Power losses (ZVS technique)

	P_{OF} [W]	P_{OF} [W]	P_{OF} [W]	P_{OF} [W]
t_D	**300 ns**	**300 ns**	**500 ns**	**500 ns**
$C_{OSS(AUX)}$	0 nF	1 nF	0 nF	1 nF
IPW60R165CP	7	3,8	6,7	2,7

The results of ZVS mode are listed in Table 2. It can be seen that the value of turn – of losses is highly dependent on both variable parameters. Higher value of auxiliary capacitance is limiting the rise of transistor's voltage slope and longer dead time secures more time to charge/discharge the internal/auxiliary capacitances.

Simulation analysis of ZCS switching technique has been performed through the use of circuit which is show on Fig. 3. The resonant components (L_R, C_R) form the necessary conditions for generating waveforms in ZCS commutation mode. The load is presented by fast voltage rectifier (D1, D2, D3, and D4) and by the load resistance (R_{LOAD}). If rectifier is replaced by resistance, the circuit would work as an series resonant inverter.

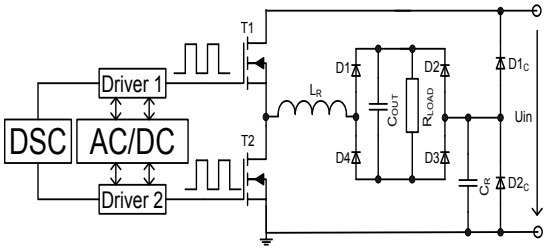

Fig. 3. Principal scheme for ZCS technique analysis

Parameters of simulation: Constant parameters: U_{IN} = 325 V, I_{LOAD} = 10 A; R_{GATE} = 22 Ω, f_{SW} = 100 kHz. Variable parameter: t_D = 300ns, 500ns, 1µs

Table 3. Power losses during turn on process (ZCS technique)

		P_{ON} [W]	
t_D	**300 ns**	**500 ns**	**1 us**
IPW60R165CP	3,8	3,42	3,4

Table 3 is showing results from parametric simulation experiment of ZCS turn – on process. In any case of dead time setting the turn – on losses are almost the same. Therefore it could be said, that dead time is not influencing the amount of turn on losses, and existing difference should be caused by simulation error. Opposite situation is visible at investigation of turn – of power losses. Value of this loss is not in linear relationship to dead time, whereby the lowest value of losses occurs at the highest value of dead time. It is also generally well known that ZCS is not good option for unipolar transistor structure, due to existence of high value of internal capacitances [1, 4, 6].

Fig. 4. is showing comparison of absorbed energy during one switching period of transistor at various commutation modes.

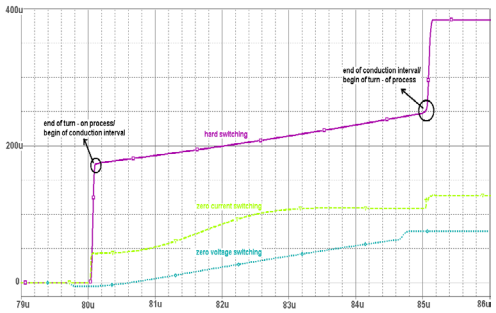

Fig. 4. Comparison of absorbed energy of transistor IPW60R165CP during one switching period at various mode (HS – solid line, ZCS – dashed line, ZVS – dot line)

These waveforms were prepared by OrCAD_PSpice simulation tool, and are valid for best conditions of each commutation mode (ZVS: t_D = 500 ns, C_{OSSAUX} = 1 nF, ZCS: t_D = 1 us). It has to be noted that, waveform is showing also absorbed energy during conduction interval. The amount of switching losses is from begin to the end of turn – on, or turn – of process.

Utilization of optimized commutation mode at selected SMPS topology

The well–known PWM hard switching converters are characterized by low efficiency due to high value of power losses that are caused by high switching frequency operation. The candidate topology for the current fast–switching applications achieving high efficiency is represented by resonant converters. The resonant converters are well–known due to their high efficiency and low EMI noise. The perspective resonant topology is nowadays the LLC resonant converter (Fig. 5). The benefit of the LLC resonant converter is a narrow switching frequency range with a light load and ZVS capability with even no load [7–10]. It is well–known that a LLC converter is a multiresonant type of converter. It could be working at three different types of operation (Fig. 5). Each operating state is dependent on DC – gain characteristic of the LLC converter. Region 1 and Region 2 are characterized by ZVS operating conditions. The operation of the converter in Region 3 is not recommended due to the ZCS conditions. For operation of the converter with constant DC voltage, it is recommended to operate at the boundary between Region 1 and Region 2. The region 2 is recommended for the operation when reduced DC–supply voltage occurs at the input of the converter. A detailed character of operation in each region is described at [8–10].

For evaluation of optimized commutation mode and for comparison of results with non–optimized settings we have focused only on the most complex operation, which is in the Region 2. Depending on the state of the power switches T1 and T2, the operation of the LLC converter in Region 2 can be divided into six time intervals per cycle.

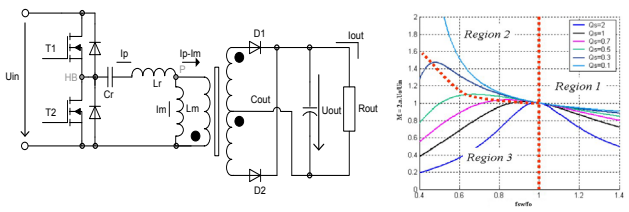

Fig. 5. Principal schematics of LLC resonant converter (left) and DC – gain characteristic (right)

Fig. 6 shows the relationship of currents and voltages in the LLC converter during each interval. Note that for operation of the LLC converter in Region 1 the interval t1 → t2 will disappear. The investigation of influence of optimized commutation mode on efficiency of converter was done by utilization of OrCAD_PSpice software. The results of simulation analysis are shown on Fig. 7.

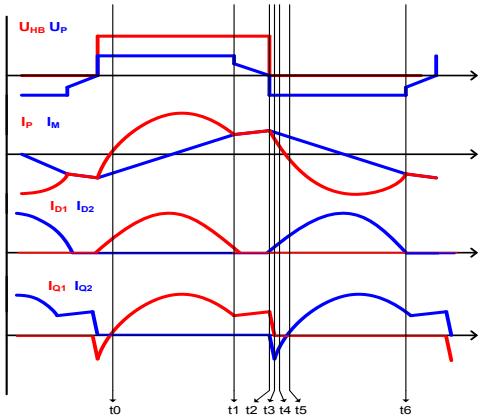

Fig. 6. LLC converter timing diagrams for operations in Region 2

Parameters of simulation: Constant parameters: input voltage of LLC, U_{IN} = 325 V; output voltage of LLC, U_{OUT} = 60V; switching frequency of LLC, f_{SW} = 100 kHz; output power of LLC, P_{OUT} = 1500W; resonant circuit parameters: L_R= 6,6 µH, C_R= 100 nF, L_M = 36 µH. Variable parameters: deadtime, t_D = 300ns, 500ns; transistor's auxiliary capacitance, C_{OSSAUX} = 0nF, 1nF.

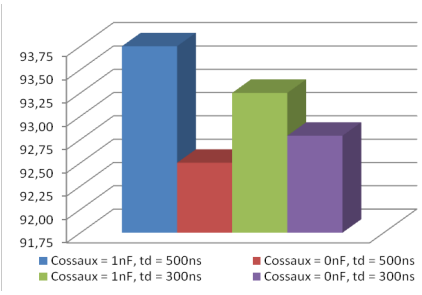

Fig. 7. Efficiency of LLC converter at full load (1500W) and various settings of ZVS commutation mode parameters

Conclusions

From the results above, when operating transistor in hard switching mode it could be said that turn – of losses can be reduced by utilization of faster device. The result of ZVS analysis is confirmation of benefits using unipolar structures in this commutation mode, namely IPW60R165CP, which due to good static and dynamic parameters has showed very low switching losses. Turn – of losses in ZVS mode has showed obvious dependency on variable parameters C_{OSSAUX} and t_D, where increase of t_D and increase of C_{OSSAUX} had decreased total power losses markedly. At settings of C_{OSSAUX} = 1nF and t_D = 500ns the transistor IPW60R165CP has showed the lowest value of power losses. The analysis of ZCS technique has showed that by its utilization the both components of switching losses could be eliminated. Ideal use is for IGBT structure. ZCS switching mode is not recommended for unipolar structures due to their high value of parasitic capacitances. The best results has occurred at setting t_D = 1us. This value of deadtime is very high for high frequency applications; therefore the results of power losses in this case are not directive.

Comparing losses of MOSFETs the total power losses in ZCS mode rose up by 37% in the case of IPW60R165CP comparing to ZVS mode with $C_{OSS(AUX)}$ = 1nF and t_D = 500ns.

The investigation of commutation mode terminates into verification of optimal settings of selected commutation technique (ZVS) through simulation analysis of selected topology of SMPS, which is LLC resonant converter. During simulation experiments at maximum load of LLC converter (1500 W), the important parameters such dead time and auxiliary capacitance of transistor were changed. The influence of these parameters were monitored and reflected on efficiency of converter. As can be seen the optimization of commutation mode caused increase of efficiency by 1,25% comparing to non – optimized solution of commutation mode. Thus in such way it is possible to increase efficiency of SMPS almost in every application.

Acknowledgements

The authors wish to thank for financial support to Slovak Research and Development Agency APVV project No. VMSP–P–0085–09, LPP–0366–09 and APVV–0535–07.

References

1. **Aghion H., Ursaru O., Lucanu S.** Three – phase motor control using modified reference wave // Electronics and Electrical Engineering. – Kaunas: Technologija, 2010. – No. 3(99). – P. 35–38.
2. **Stupak V.** Ensuring efficiency of electronic devices // Electronics and Electrical Engineering. – Kaunas: Technologija, 2010. – No. 1(97). – P. 15–18.
3. **Dobrucky B., Špánik P., Kabašta M.** Power electronic two–phase orhogonal system with HF input and variable output // Electronics and Electrical Engineering. – Kaunas: Technologija, 2009. – No. 1(99). – P. 9–14.
4. **Wang H. H., Khambadkone A.M.** Analytical power loss evaluation of 5 level H–bridge with coupled inductor and series connected H–bridge for PEBB applications // PEDS, 2009. – P. 458–463.
5. **Wang B., Xin X., Wu S., Wu H., Ying J.** Analysis and implementation of LLC burst mode for light load efficiency improvement // APEC, 2009. – 24th Annual IEEE conference. – P. 58 –64.
6. **Hargaš L., Hrianka M., Lakatoš J., Koniar D.** Heat fields modelling and verification of electronic parts of mechatronics systems. // Metalurgija, 2010. – No. 49(2). – P. 268–272.
7. **Lee B. H., Kim M. Y., Kim CH. E., Park K. B., Monn G. W.** Analysis of LLC resonant converter considering effects of parasitic components // INTELEC, 2009. – P. 1–6.
8. **Yuan B., Xu M., Yang X., Li D.** A new structure of LLC with primary current driven synchronous rectifier // IPEMC, 2009. – P. 1266–1269.
9. **Yi K. H., Kim B. CH., Moon W.** A simple and novel two phase interleaved LLC series resonant converter employing a phase of the resonant capacitor // ECCE, 2009. – P. 757–757
10. **Kováčová I., Kováč D.** Parasitic Capacitances of Power Electrical Systems and EMC // Acta Technica. – CSAV, 2009. – No. 54. – P. 99–111.
11. **Špánik P., Dobrucký B., Frivaldský M., Drgoňa P.** Measurement of switching losses in power transistor structure // Electronics and Electrical Engineering. – Kaunas: Technologija, 2008. – No. 2(82). – P. 75–78.

Received 2010 06 22

P. Špánik, M. Frivaldský, P. Drgoňa, J. Kandráč. Efficiency Increase of Switched Mode Power Supply through Optimization of Transistor's Commutation Mode // Electronics and Electrical Engineering. – Kaunas: Technologija, 2010. – No. 9(105). – P. 49–52.

The paper deals with research of actions, which are taking place during the switching of power transistor in different commutation modes. The main target is to reach optimal settings of selected commutation mode (hard switching, Zero Voltage switching, Zero Current switching) what in final result has to be reflected in efficiency increase of switched mode power supply (SMPS). Target application of SMPS is high frequency operation (from 100 kHz) with output power over 1,5kW. The paper shows simulation results of various settings of commutation mode for transistor IPW60R165CP. At the end of paper the comparison of SMPS efficiency with standard settings and optimal settings of commutation mode is being shown. Ill. 7, bibl. 11, tabl. 3 (in English; abstracts in English and Lithuanian).

P. Špánik, M. Frivaldský, P. Drgoňa, J. Kandráč. Galios šaltinių perjungimo būsenos efektyvumo didinimas optimizuojant tranzistorių perjungimo būsenas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 9(105). – P. 49–52.

Nagrinėjamos problemos, susijusios su galios tranzistorių būsenomis ir jų kitimu. Pagrindinis tikslas yra nustatyti optimalius pasirinktos perjungimo būsenos parametrus, kas padidintų galios šaltinių perjungimo būsenos efektyvumą. Tai būtų taikoma sistemose esant 100 KHz dažniui ir ne mažesnei kaip 1,5 KW galiai. Pateikti IPW60R165CP tranzistoriaus įvairių perjungimo būsenų parametrų modeliavimo rezultatai, palyginti įprasti ir optimalūs perjungimo būsenos parametrai. Il. 7, bibl. 11, lent. 3 (anglų kalba; santraukos anglų ir lietuvių k.).