

Design and Application of Full Digital Control System for LLC Multiresonant Converter

P. Špánik, P. Dragoňa, M. Frivaldský, A. Prikopová

Department of Mechatronics and Electronics, Faculty of Electrotechnical Engineering, University of Žilina, Univerzitná 1, 010 21 Žilina, Slovak Republic, e-mail: frivaldsky@fel.uniza.sk

Introduction

Resonant converters are well-known due to their high efficiency and low EMI (Electromagnetic Interference) noise. Despite of that, their utilization in most of industry and consumer applications is still limited due to their disadvantages. The perspective topology for such application is LLC resonant converter (Fig. 1), which exists for very long time but because of lack of understanding of characteristic of this converter, it was used as a series resonant converter with passive load. The benefit of frequency controlled LLC resonant converter is narrow switching frequency range, with light load and ZVS (Zero Voltage Switching) capability with even no load [1–3], also with wide input voltage range.

Steady state operation and characteristics of LLC converter are discussed in many papers as shown in references. In this paper, only basic properties of LLC converter are mentioned.

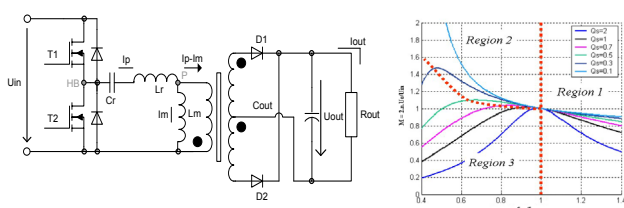


Fig. 1. Principal scheme of LLC converter

For desired operation of LLC converter, good design of control loop is necessary. For designing of digital control loop, small signal characteristics, and control-to-output transfer function is necessary. Unfortunately, standard space averaging method for revealing the transfer function cannot be used for LLC converter. For revealing the small signal characteristics and transfer function, several methods were tried, which are discussed in many papers. In this paper, new simulation based method is discussed. Advantage of full digital control system is its possibility of implementation in any microprocessor. But use of advanced floating point

processors for low-end application is not economically profitable. In this paper, application of advanced full digital control system in low price fix-point processor is proposed.

Transfer function of LLC Converter

Design of digital control system for power converter requires control-to-output transfer function. Based on this transfer function, digital controller can be obtained. For PWM converters, standard "averaged" methods can be used for revealing the transfer function of converter. One of method with good results is "direct circuit averaging". This method can be easily implemented for standard PWM converters such as boost, buck, flyback etc. Transfer function obtained with this method has duty cycle as an input value and output voltage as an output value.

Unlike the PWM converters, the control transfer function of frequency controlled resonant converters cannot be obtained by state space averaging method, due to different ways of energy processing. While state space averaging methods eliminates the information about switching frequency, they cannot predict dynamic properties of resonant converters, so the proper control-to-output transfer function cannot be evaluated.

There is a several methods for solving this problems, but some of them are too simplified and idealized, others are too complex and difficult to use[1, 2]. In this paper, new simulation based method for revealing the control transfer function is proposed.

This method is based on PSPICE simulation and use of System Identification Toolbox in MATLAB environment. First, the simulation of main circuit in PSPICE must be created. Using of PSPICE simulation, the dependency of output (voltage, current) on input (switching frequency, duty cycle) can be simulated. Data acquired from simulation in PSPICE are used in MATLAB System Identification Toolbox. Whole process used in this method is shown on Fig. 2.

Using of this toolbox offers several models for identification of system. With use of different models from

System Identification Toolbox (SIT), identification of all converters is possible.

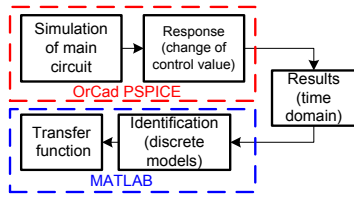


Fig. 2. Simulation based method for identification of transfer function

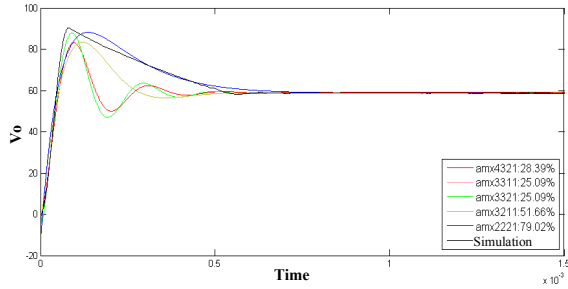


Fig. 3. Accuracy of ARMAX models with different degree (up to down 4, 3, 2)

System Identification Toolbox includes number of models in continuous or discrete form, which can be used for identification of systems: ARX (Auto Regressive Exogeneous Input Model), ARMAX (Auto Regressive Moving Average Exogeneous Input Model) OE (Output Error Model), BJ (Box-Jenkins Model), SS (State-Space Model). Accuracy of the models depends on degree of polynomials used in transfer function. Fig. 3 shows accuracy of identified transfer function on its polynomial degree for ARMAX model of LLC converter. All models are in discrete form (z-domain), so the exact specification of sampling interval is necessary. Sampling interval used for models in SIT must be equivalent with integration step used for simulation in OrCad PSPICE. Requested discrete transfer function is in form

$$G(z) = \frac{B(z)}{A(z)} = \frac{b_0 + b_1z^{-1} + b_2z^{-2} + \dots + b_{nb}z^{-nb}}{a_0 + a_1z^{-1} + a_2z^{-2} + \dots + a_{na}z^{-na}} \quad (1)$$

After acquiring of transfer function, the proper discrete controller can be designed.

Design of discrete controller

Due to implementation in microprocessor, the controller must be in discrete form. There are two ways to design a discrete controller - design by emulation and direct digital design[5].

In the design by emulation approach, also known as digital redesign method, first an analog controller is designed in the continuous domain, by ignoring the effects of sampling and hold of A/D converter and computing delay of microprocessor. In next step, the controller can be converted into discrete-time domain by one of discretization method. This approach is good for systems

of lower degree, but in discrete systems of higher degree, the transient responses does not reflect the required values because of ignoring sample and hold and computation delay effects.

On the other side, direct digital design approach offers design of controller directly in z-domain, without conversion, including effects of A/D converter and microprocessor. Block diagram of this approach is on Fig. 4.

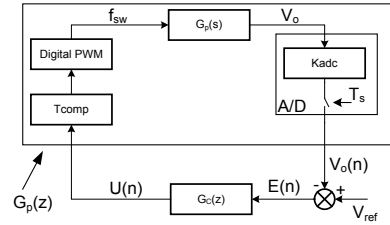


Fig. 4. Direct digital design control loop

Sampling of measured value with A/D converter can be represented by ideal Zero-Order-Hold block with sample time T_s . Gain of A/D converter is represented by block K_{adc} . Computing delay of microprocessor, also with delay from PWM module are represented by block T_{comp} . A/D converter with PWM module together form a sampling-and-hold device. Sample and hold block brings additional time delay of $T_s/2$ and phase lag of $\omega T_s/2$, which means, that reconstructed signal has time or phase lag.[3,5]. Block T_{comp} represents delay between conversion of A/D converter and PWM duty cycle or modulo update. Time between this two events is necessary for computing the values for PWM block. Discrete transfer function of whole converter including Zero-Order block, Sample-and-Hold effect and gain of A/D converter is

$$G(z) = Z \left\{ \frac{1}{s} (1 - e^{-sT_s}) \cdot H_C(s) \cdot G_p(s) \cdot K_d \right\} \quad (2)$$

Fig. 6 shows effect of sampling interval with computing delay on stability of closed control loop. Table 1 shows transfer functions with different sampling intervals and different computational delays. Sampling times were used from A/D converter included in DSC 56F8013, the computing times were used from same processor. Application was for digital control system for 200kHz LLC multiresonant converter. In this system discrete regulator of third order was used [3].

Table 1. Sampling times and computational delays for transfer functions in Fig. 6

Sampling time	T_s	Computing delay T_{comp}	Mark
5 μ s		0	Gz1
10 μ s		0	Gz2
5 μ s		3 μ s	Gdlyz1
10 μ s		3 μ s	Gdlyz2
5 μ s		6 μ s	Gdlyz3
10 μ s		6 μ s	Gdlyz4

From Fig. 5 is clear, that computing delay has significant effect on stability of the control loop. With rising computing and sampling time stability of system drops.

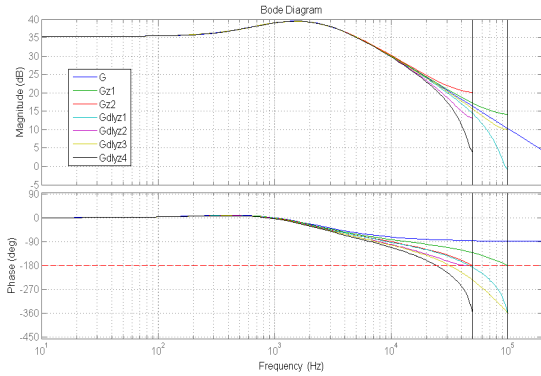


Fig. 5. Effect of sample and hold and computation delay on stability of control loop

For design of controller in z-domain, all above mentioned delays must be taken into account. With use of MATLAB Siso Design Tool, the proper discrete controller can be designed. Advantage of this tool is possibility of direct placing of zeroes and poles of controller on bode diagram of closed or open loop. After placing the poles or zeros of controller, the different responses of closed control loop can be displayed for verification.

Implementation in DSC

Discrete controller proposed in previous chapter was implemented into 16b digital signal controller (DSC) Freescale 56F8013, which is primary designed for motor and converter control. Advantage of this microprocessor are high performance peripherals, on the other side, disadvantage of this processor is low core frequency - 32MHz. For better performance, fraction arithmetic with intrinsic functions were used in this DSC.

Block scheme of digital control system with DSC 56F8013 on 200kHz LLC converter is on Fig. 6.

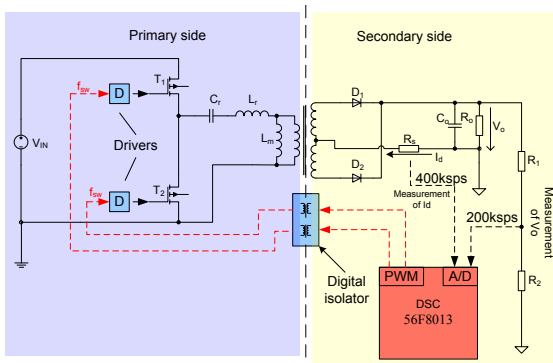


Fig. 6. Block scheme of full digital control system with DSC 56F8013

Another option for implementation is use of 32b microprocessor ColdFire V1 which offers better computing performance, but sampling time of A/D converter is twice as in DSC 56F8013. For measurement of output voltage, this time is sufficient, but for current sensing, the A/D

converter on ColdFire is too slow. This problem was eliminated by use of special algorithm for computing of diode current from value of output voltage, value of load and ripple. Detailed method is described in [3]. Times required for computing on both processors are in table 2.

Table 2. Sampling times and computational delays for two processors

Processor	Bits	Core frequency	A/D sampling time	Computing of control loop	Computing of current value
56F8013	16b	32Mhz	1.126 μ s	2.98 μ s	3.01 μ s
ColdFireV1	32b	50,3Mhz	2.252 μ s	1.8 μ s	1.12 μ s

Verification of proposed full digital system

Waveforms from digital control system at no load condition are shown in Fig. 7 - output voltage 58.8V at 201kHz switching frequency.

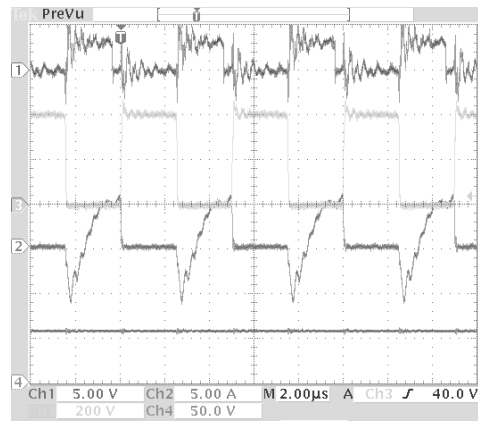


Fig. 7. Measured waveforms with digital control system - no load: (top to down): pwm pulses(1), transistor voltage(3), transistor current(2), output voltage(4)

For measurements of control systems at full load conditions, the requested output voltage was changed to 50V due to lower tolerance of used MOSFETs against current peaks. Input voltage was 325V due to verification of dynamic properties of controllers. Waveforms from analog integrated circuit are in Fig. 8, where output voltage was 45.2V at 150kHz switching frequency.

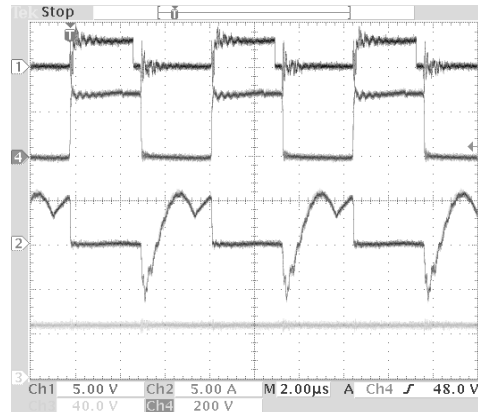


Fig. 8. Measured waveforms with analog control system - full load: (top to down): pwm pulses(1), transistor voltage(4), transistor current(2), output voltage(3)

Conclusions

Design procedure and measurements of proposed digital control system shows good accordance. Comparison of measured waveforms at full load, shows good accuracy for digital control system. Accuracy of output voltage control is better than hysteretic regulators used in market available analog integrated circuits (FAN7621, HIPERPLC(PLC810PG)). Also, the stress of the high frequency transformer, is lower with digital control system, due to linear change of the switching frequency during operation. On the other side, from measurements at no load condition results, that digital control system has lower resistance against EMI. Also, the stability of analog control system was better than digital, which was caused by long computing time compared to switching frequency of converter (200kHz). This problem can be solved by use of faster microprocessor, or by eliminating of current control loop - this option is described in [3]

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With use of microprocessors and digital signal controllers as a control systems in power semiconductor converters, the new approaches for design of digital control must be implemented. Designing a digital control system requires use of control to output transfer function. For new, frequency controlled resonant converters, like LLC converter, new simulation based, numerical methods must be employed. This paper deals with new method for revealing the transfer function. For proposal of optimal controller, the direct digital design was used. Verification of designed digital control system is shown at the end of paper. Ill. 8, bibl. 12 (in English; abstracts in English and Lithuanian).

P. Špánik, P. Drgoňa, M. Frivaldský, A. Příkopová. Visiška skaitmeninio LLC konverterio valdymo sistemos projektavimas ir taikymas // *Elektronika ir elektrotechnika*. – Kaunas: Technologija, 2010. – Nr. 10(106). – P. 75–78.

Skaitmeninė galios puslaidininkų konverterių kontrolė gerinama naudojant mikrovaldiklius ir skaitmeninių signalų kontrolierius. Kontroluojama išėjimo perdavimo funkcija, naudojama projektuojamojoje skaitmeninėje valdymo sistemoje. Tokioje sistemoje turi būti įvertinti konverteriai (LLC), modeliavimo rezultatai bei siūloma naujų metodų. Perdavimo funkcija aprašyta pasiūlytu nauju metodu. Suprojektuotas naujas skaitmeninis kontrolieris. Atliktas ir pateiktas valdymo sistemos patikrinimas. Il. 8, bibl. 12 (anglų kalba; santraukos anglų ir lietuvių k.).