Comparative Study of Rectifier Topologies for Quasi-Z-Source Derived Push-Pull Converter

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***Abstract*—Quasi-Z-source derived push-pull converter is a new topology intended for energy harvesting from renewable energy sources. Use of the topology shows that currents in the input and output parts strongly depend on the implementation of the output rectifier. This paper presents a comparative study and an experimental evaluation of the four output rectification stages. Analytical expressions for the voltage and current stress of rectifier components are presented. Experimental verification with the 400 W prototype was performed in the input voltage range of 40 V to 400 V at 400 V output voltage. Efficiency and duty cycle of active state, i.e. the DC gain characteristic, were measured in that range. Experimental waveforms for each topology are presented. Waveforms were measured at the input voltage 80 V, i.e. at the DC gain factor equal to 5.**

***Index Terms*—DC/DC power converters, rectifiers, circuit optimization, renewable energy sources.**

I. INTRODUCTION

The concept of the quasi-Z-source inverter (qZSI) was proposed by Prof. F. Z. Peng in 2008 [1]. It is based on the two-port impedance network that couples inverter circuit to the input DC source. qZSI provides high EMI immunity, wide regulation freedom and continuous input current. These advantages make the qZSI suitable for renewable and alternative power applications (solar panels, fuel cells, wind power generators, etc.) [2]–[5] and propulsion motor drive applications [6], [7]. DC/DC converters derived from the qZSI show high performance as intermediate voltage matching converters between the renewable energy source and the grid-tied inverter [8]-[11]. Usually output voltage should be stabilized at 400 V level for single-phase inverters and 600 V for three-phase inverters regardless of the variation of the input voltage.

The new topology shown in Fig. 1a was first proposed in 2012 [12]. It is derived by the combination of a single-switch non-isolated quasi-Z-source converter (qZSC), coupled inductors, and the conventional push-pull topology. The converter utilizes two quasi-Z-source networks. Each of them consists of a coupled inductor, a diode, and two capacitors. Coupled inductors TX_1 and TX_2 combine several functions: input current filtering, energy storage, and galvanic isolation. Coupling coefficients between all windings are close to unity.

Primary side windings contain N_{12} turns, and secondary windings utilize N_3 turns.

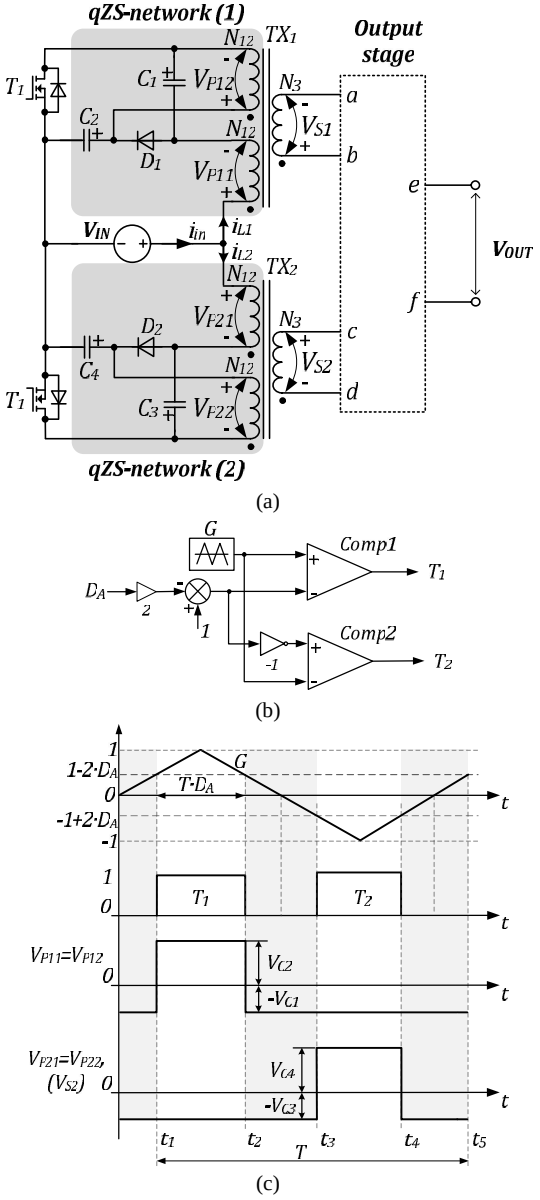

Fig. 1. General schematic (a), switching controller (b), and operational principle (c) of the investigated quasi-Z-source derived push-pull converter.

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Secondary windings are connected to the output rectifier. Magnetizing inductances of three-winding coupled inductors serve as energy storage elements in the corresponding arms. A detailed steady-state analysis of this topology with a bridge rectifier and an LC filter was presented in [13]. Each transistor is switching with a duty cycle of active state $D_A < 0.5$.

Transistors operate interleaved in order to reduce current ripple at the input. Coupled inductors turns ratio

$$k = \frac{N_3}{N_{12}}. \tag{1}$$

Voltage values in the quasi-Z-source networks depend on the duty cycle of active state (D_A) and the input voltage:

$$V_{C1} = V_{C3} = \frac{D_A}{1-2D_A} V_{IN}, \tag{2}$$

$$V_{C2} = V_{C4} = \frac{1-D_A}{1-2D_A} V_{IN}. \tag{3}$$

Fig. 1(b) and Fig. 1(c) show the simplest switching controller and idealized voltage waveforms across the primary windings of the isolation transformer. According to the steady state analysis, capacitor voltage in the quasi-Z-source (qZS) network is independent of the output stage topology. Rectifier implementation influences the currents in the transformer windings. Selected rectifier topology defines current shapes, DC gain characteristics and influences the efficiency of the converter.

Investigated topology was initially intended for operation with a bridge rectifier and an LC-filter [12], [13]. This paper applies different rectifier topologies to the quasi-Z-source derived push-pull converter in order to examine overall converter performance in each case.

II. Overview of Rectifier Topologies

Four rectifier topologies were selected for our analysis: Fig. 2(a) shows the bridge rectifier (B4); Fig. 2(b) – the doubled half-wave rectifier (2C-HW); Fig. 2(c) – the full-wave rectifier with three capacitors (3C-FW); Fig. 2(d) – the full-wave rectifier with two capacitors (2C-FW). In our analysis of the different topologies, leakage inductances of the coupled inductors were not taken into account, but their influence was considered in the idealized waveforms of rectifier elements currents in Fig. 3. In the figure, P_O is the output power of the converter.

A. Bridge Rectifier

A bridge rectifier is a conventional solution. The B4 topology consists of four diodes and one output filtering capacitor. It requires series connection of secondary windings. Energy is transferred to the output when one of the transistors is turned on. Idealized waveforms of voltages and currents of the B4 rectifier are shown in Fig. 3(a). This topology is a rather simple conventional solution. The main disadvantage is voltage oscillations across the rectifier diodes when both transistors are switched off. This leads to additional losses in semiconductor components. In our experiments this topology was unable to operate in the input voltage range of 40 V to 400 V at the output power 400 W due to the overvoltage across the semiconductor elements in the primary part.

The main advantage of the bridge rectifier is the low ripple of the input current. Currents in secondary windings are equal in absolute value and have different directions: $i_{s1} = -i_{s2}$. Current from the secondary winding is partially reflected in the primary windings. This means that different direction of currents in the secondary winding leads to partial ripple compensation between the input currents of two qZS networks (i_{L1} and i_{L2}).

With regard to expressions (1)–(3), the ideal DC gain factor of the B4 topology is as follows

$$G_{B4} = \frac{V_{OUT}}{V_{IN}} = k \cdot (V_{C1} + V_{C4}) = \frac{k}{1-2D_A}. \tag{4}$$

B. Doubled Half-Wave Rectifier

Doubled half-wave rectifier is the simplest solution. It does not require series connection of secondary windings. Each branch works separately with a 180° phase shift. Energy is transferred to the output only when one of the transistors is turned on. Idealized waveforms of voltages and currents of the 2C-HW rectifier are shown in Fig. 3(b). This topology utilizes only two diodes, but it requires two series connected capacitors at the output.

The main disadvantages are voltage oscillations across rectifier diodes when the diode is reverse biased, and high current ripple in the output capacitors. These oscillations occur between the parasitic capacitance of the diode and the leakage inductance of the transformer, leading to the high overvoltage and low reliability. This problem could be solved with the snubber circuit, but it will lead to either price rise or lower efficiency. Moreover, of all the topologies, this topology has the highest input current ripple. High current ripple in the output diodes and no ripple compensation effect, which is observed in the B4 topology, lead to relatively high input current ripple.

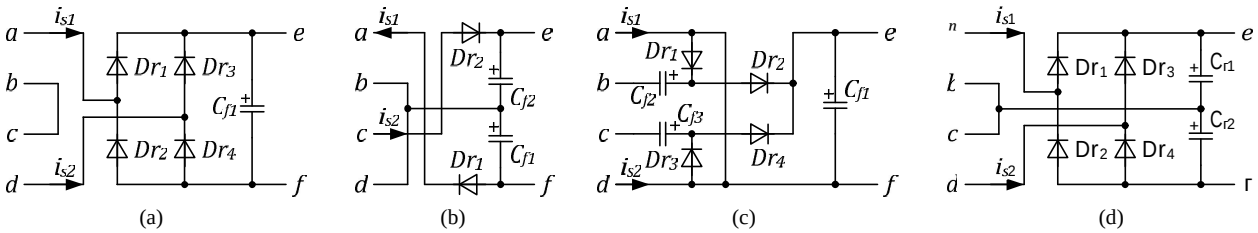
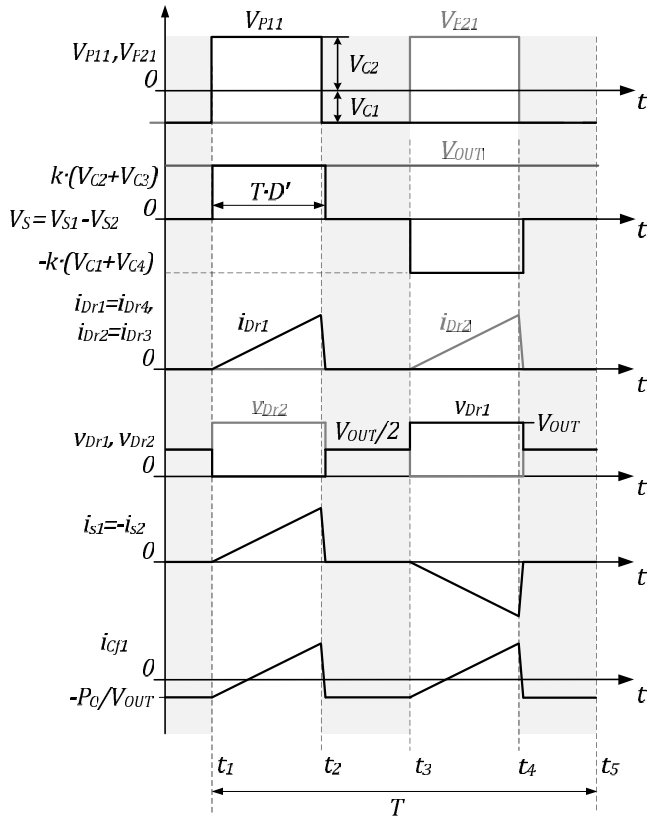
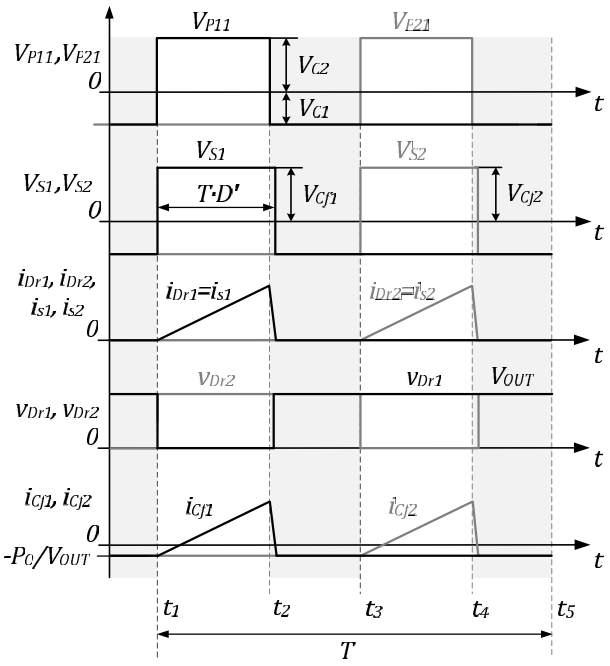


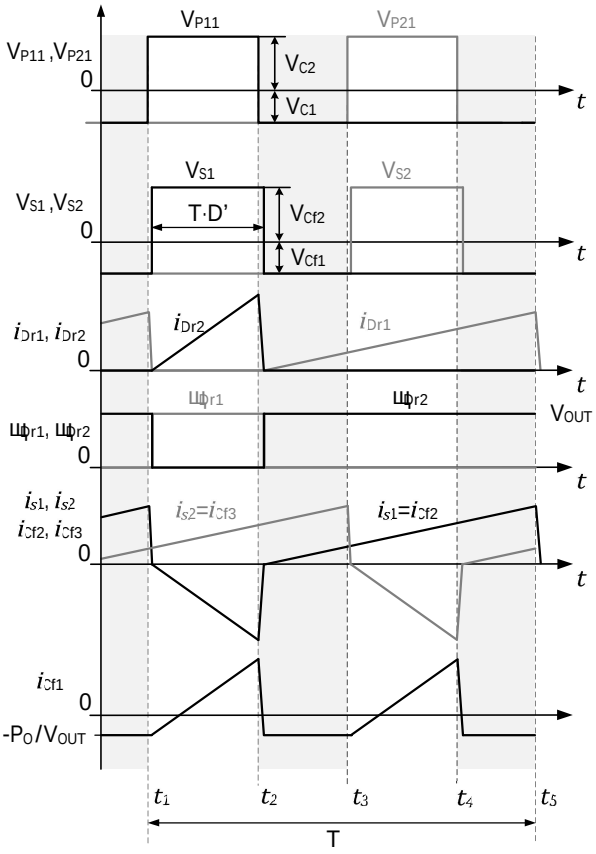
Fig. 2. Output rectifier topologies used in our comparative study: a) B4, b) 2C-HW and c) 3C-FW and d) 2C-FW.



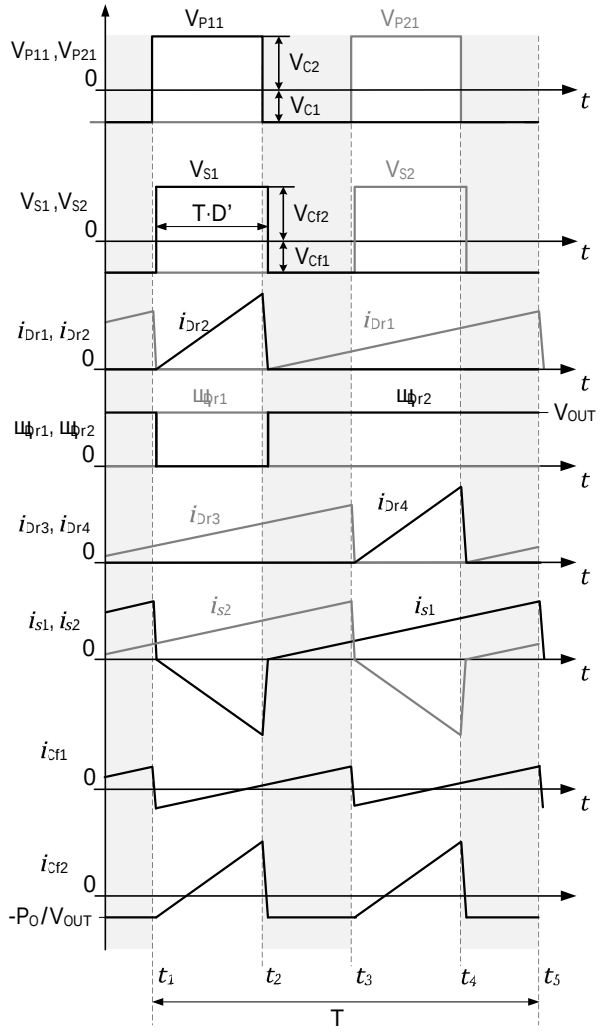
(a)



(b)



(c)



(d)

Fig. 3. Idealized waveforms of voltages and currents for the selected rectifiers: a) B4, b) 2C-HW and c) 3C-FW and d) 2C-FW.

2C-HW topology can be represented as two isolated converters with input-parallel-output-series (IPOS) connection. An ideal DC gain factor of a doubled half-wave rectifier can be calculated taking into account (1) and (3)

$$G_{C2-HW} = \frac{V_{OUT}}{V_{IN}} = k \cdot (V_{C2} + V_{C4}) = 2k \cdot \frac{1-D_A}{1-2D_A}. \quad (5)$$

C. Full-Wave Rectifier Topologies

Operation principles of full-wave rectifiers are almost similar. In this case each branch of the converter is working independently, connected to the same capacitor (capacitors) of the output filter. 2C-FW and 3C-FW topologies can be represented as two independent converters that are working interleaved. Converters are connected in the input-parallel-output-parallel (IPOP) configuration. These topologies completely utilize both half-waves of the secondary winding voltage. This means that both capacitor voltages from the quasi-Z-source network are reflected to the output. Operation principles for the 3C-FW and the 2C-FW are shown in Fig. 3(c) and Fig. 3(d), respectively. Diodes of the output rectifier turn on and turn off at zero current due to the influence of the leakage inductance of the transformers. Diodes could be separated into pairs: D_{r1}, D_{r2} and D_{r3}, D_{r4}. In each pair only one diode is conducting simultaneously, the other one is reverse biased with the output voltage. No oscillations occur in these two topologies. The main difference lies in the energy transfer principle.

In the 3C-FW topology capacitors C_1 and C_3 charge output capacitors C_{f2}, C_{f3}, respectively. Part of the energy stored in C_{f2}, C_{f3} will be transferred to C_{f1}. It leads to additional losses in intermediate capacitors C_{f2}, C_{f3} due to their equivalent series resistance. Capacitors C_{f2}, C_{f3} have high RMS current because the corresponding secondary winding current flows through them, as shown in Fig. 3(c). In the 2C-FW topology energy is transferred to the capacitor of the two output capacitors without intermediate charging processes. 2C-FW has fewer elements and offers the same advantages and somewhat higher efficiency with the performance similar to that in the 3C-FW rectifier.

Full-wave rectifier topologies and the bridge rectifier have the same DC gain factor. Ideal DC gain factors are shown in Fig. 4. Half-wave topology tends to have higher boost abilities. Taking into account (1)–(3), DC gain factor for full-wave topologies can be expressed as follows

$$G_{FW} = \frac{V_{OUT}}{V_{IN}} = k \cdot (V_{C1} + V_{C2}) = \frac{k}{1-2D_A}. \quad (6)$$

III. COMPARISON OF RECTIFIER TOPOLOGIES

Table I compares all the investigated topologies for the number of elements, possible parasitic oscillations, and paralleling possibilities. As it follows from the table, all the topologies, except B4, allow parallel connection of several convertors. Extended topology on the basis of 2C-HW can provide high DC voltage step-up ratio due to series connection of outputs. Full-wave rectifiers show the possibility of parallel connection of several converters in the IPOP modular structure.

Table II provides steady state current and voltage stresses for all elements of the rectifier stage. In this table a new variable is used – D'. It is close to the duty cycle D_A.

TABLE I. COMPARISON OF TOPOLOGIES.

Parameter	B4	2C-HW	3C-FW	2C-FW
Half-wave (HW) or full-wave (FW)	FW	HW	FW	FW
Number of diodes	4	2	4	4
Voltage oscillations across diodes	Yes	Yes, with overshoot	No	No
Number of capacitors	1	2	3	2
Parallel configuration	N/A*	IPOS	IPOP	IPOP

*N/A- not applicable

TABLE II. STEADY STATE VOLTAGE AND CURRENT STRESSES.

Parameter	Element	B4	2C-HW	3C-FW	2C-FW
Average current	Dr_1	$\frac{1}{2}\cdot\frac{P_O}{V_{OUT}}$	$\frac{P_O}{V_{OUT}}$	$\frac{1}{2}\cdot\frac{P_O}{V_{OUT}}$	$\frac{1}{2}\cdot\frac{P_O}{V_{OUT}}$
	Dr_2				
	Dr_3		N/A*		
	Dr_4		N/A		
Maximum current	Dr_1	$\frac{1}{D'}\cdot\frac{P_O}{V_{OUT}}$	$\frac{2}{D'}\cdot\frac{P_O}{V_{OUT}}$	$\frac{1}{1-D'}\cdot\frac{P_O}{V_{OUT}}$	$\frac{1}{1-D'}\cdot\frac{P_O}{V_{OUT}}$
	Dr_2			$\frac{1}{D'}\cdot\frac{P_O}{V_{OUT}}$	$\frac{1}{D'}\cdot\frac{P_O}{V_{OUT}}$
	Dr_3		N/A	$\frac{1}{1-D'}\cdot\frac{P_O}{V_{OUT}}$	$\frac{1}{1-D'}\cdot\frac{P_O}{V_{OUT}}$
	Dr_4		N/A	$\frac{1}{D'}\cdot\frac{P_O}{V_{OUT}}$	$\frac{1}{D'}\cdot\frac{P_O}{V_{OUT}}$
Voltage stress	Dr_1	V_{OUT}	V_{OUT}	V_{OUT}	V_{OUT}
	Dr_2				
	Dr_3				
	Dr_4				
	C_{f1}	V_{OUT}	$V_{OUT}/2$	V_{OUT}	$D'\cdot V_{OUT}$
	C_{f2}	N/A	$V_{OUT}/2$	$D'\cdot V_{OUT}$	$(1-D')\cdot V_{OUT}$
	C_{f3}	N/A	N/A		N/A

*N/A- not applicable

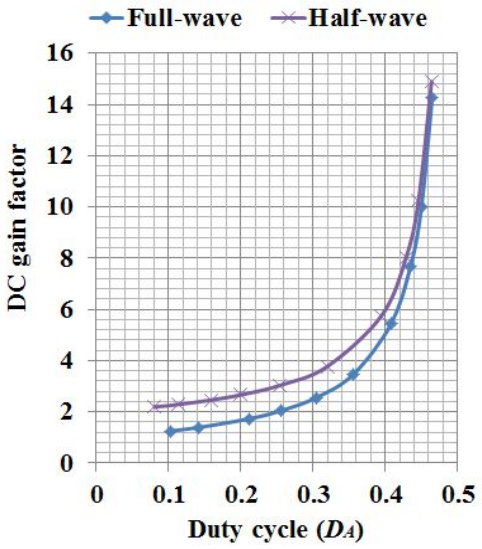


Fig. 4. Ideal DC gain factors.

A difference between the duty cycles of voltage half-waves at primary and secondary windings occurs as a result of the influence of the leakage inductance of coupled inductors. This influence is shown by the idealized waveforms in Fig. 3. The table shows that at low DC gain factor in the full-wave and bridge topologies, some diodes suffer from narrow current pulses with high magnitude. It happens because average values should remain unchanged. Also, in the 2C-FW topology voltage distribution between output capacitors is almost even at high step-up operation mode (when *D'* is close to 0.5).

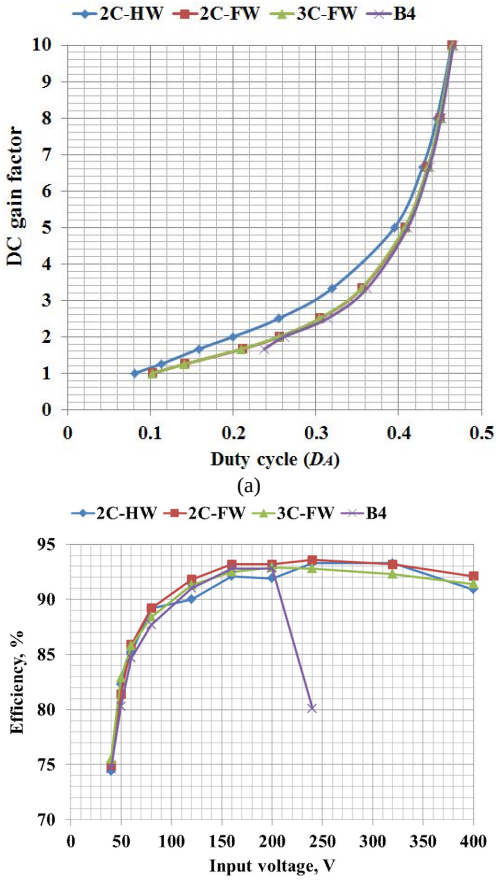


Fig. 5. Experimental results: (a) duty cycle of active state versus DC gain factor and (b) efficiency versus input voltage.

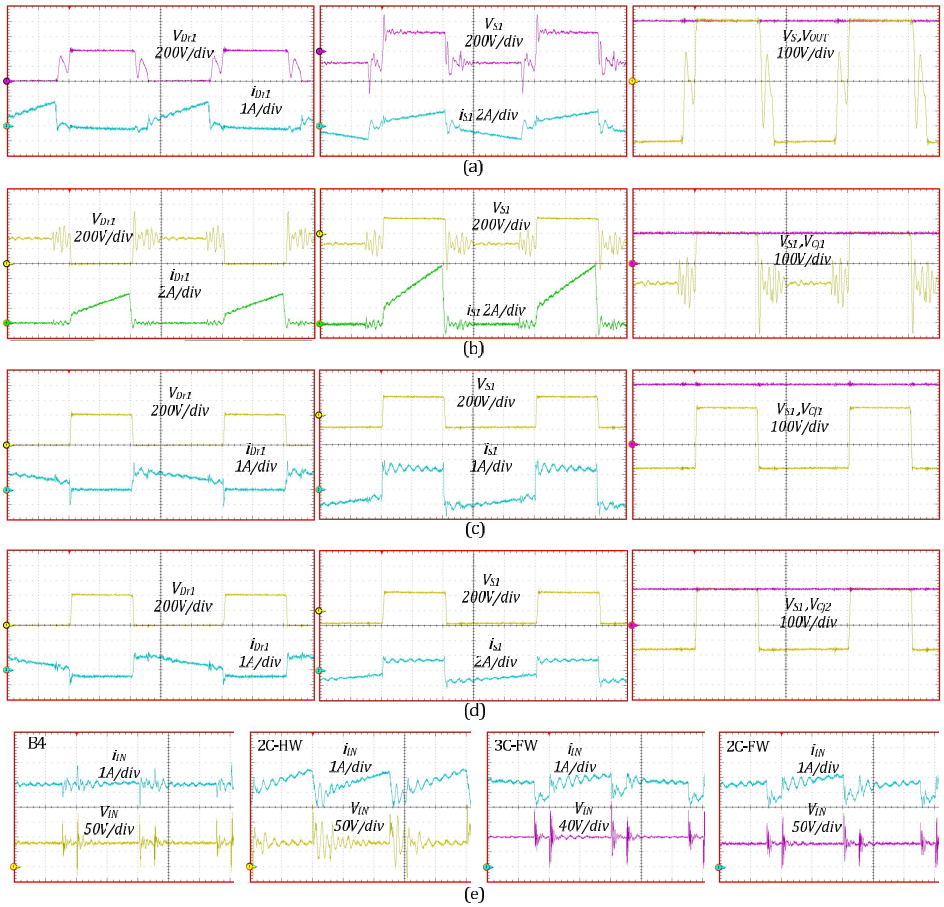


Fig. 6. Experimental waveforms of voltages and currents in a) B4, b) 2C-HW and c) 3C-FW, d) 2C-FW topology and e) input currents for all rectifiers in the time scale 2μs/div.

IV. EXPERIMENTAL RESULTS

To verify theoretical predictions, the converter was tested with four different output rectifiers. Switching frequency was selected equal to 100 kHz. The isolation transformer with $k = 1$ has the magnetizing inductance of 1 mH and the leakage inductance of 30 uH and 15 uH in the primary and secondary windings, respectively. Metalized polypropylene capacitors 60 uF/800 V were used in the quasi-Z-source networks and at the output of the converter.

All the experiments were performed under constant output power of 400 W and constant output voltage of 400 V. Results of measurements of the DC gain characteristic and the efficiency are summarized in Fig. 5. It follows from the obtained results that the 2C-FW rectifier has better performance for applications requiring a wide regulation range of the input voltage. The real step-up characteristic is close to the full-wave type at the low DC gain. B4 topology was not able to cover the whole range of the input voltage. It can operate in a wide range of input voltage when the input power rises with the input voltage, like in the systems with a variable speed wind turbine [14]. Relatively high efficiency of the prototype of this hard-switching topology was achieved by the implementation of SiC- semiconductors. Experimental waveforms for V_{IN} = 80 V, V_{OUT} = 400 V and P_O = 400 W are shown in Fig. 6. Measured waveforms confirm our assumptions about parasitic oscillations in some topologies.

V. CONCLUSIONS

Our theoretical and experimental verification of the output rectifier topologies for the quasi-Z-source derived push-pull converter showed that full-wave topology with two capacitors provides superior performance under given conditions. It enables simple paralleling of several converters, suffers from no parasitic oscillations and operates with soft commutation of the rectifier diodes. Doubled half-wave topology could be also considered as a cheaper solution for renewable energy systems.

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