Generic Losses Model for Traditional Inverters and Neutral Point Clamped Inverters

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***Abstract*—This paper presents a model of two very common inverters, a traditional inverter and neutral point clamped inverter, for calculating the losses in function of the parameters of the inverter datasheet. The model allows simulating the inverter branch under any conditions, not only nominal sinusoidal, and monitoring its losses at the same time, so the most significant parameters could be determined in losses terms. The optimization of the losses in inverters could create an important energy saving since it is present in most of the power applications, mainly renewable energies. Obviously, the model is based on the electrical equations of both semiconductors inverters so the mathematical development is exposed. Finally, the model is validated by solving the equations analytically together with the model simulation under nominal sinusoidal environment.**

***Index Terms*—Power system modelling, multilevel systems, inverters.**

I. INTRODUCTION

Year after year, mankind increases amounts of energy demand due to the continuous increase in their level of development. Conventional energy resources are limited, so the authorities and governments are promoting energy saving and efficiency. Nor should we forget the support that these entities are making for renewable energy as an alternative to conventional energy resources.

Taking into account the number of the output possibilities of one inverter branch, one of the most used converter topologies is the traditional two level Voltage Source Inverter (VSI) (Two Level Inverter, TLI), which is used to integrate the main renewable energy sources (wind and photovoltaic generation power plants) and to control typical electrical loads (most of them, AC motors). Another increasingly used topology is the three level voltage source inverter with clamping diodes (Neutral Point Clamped inverter, NPC), as it allows working with high power while offering improved quality waveform [1] [2]. The optimization of the losses in VSI could have a great impact on energy savings due to the large number of existing converters in power applications. There have been studies of losses in converters for different applications in recent years [3]–[6], including multilevel inverters.

There is free software that offers the possibility of calculating losses, such as "Semikron" webpage, the Mitsubishi "Melcosim" application or the Fuji "IGBT simulator" program, but they are limited to sinusoidal modulations for traditional inverters.

Two methods for calculating the losses for TLI and NPC converters have been developed, an analytical one and the model one. In the first section an analytical losses study of both converters is done in order to obtain a general expression for calculating conduction and switching losses, although some simplifications are needed depending on the modulation technique. Secondly, the losses equations of the semiconductors are implemented in a model without any simplification in order to calculate the losses regardless of the inverter operation, that is, no simplifications are introduced. Finally, sinusoidal currents case is analysed with both methods validating the model and comparing the results obtained for each converter.

II. VOLTAGE SOURCE INVERTER OPERATION

The losses produced by the semiconductor devices of the two level inverter (Fig. 1(a)), the three level inverter with clamping diodes (Fig. 1(b)) and, in general, the *n* level inverter could be calculated through a branch analysis.

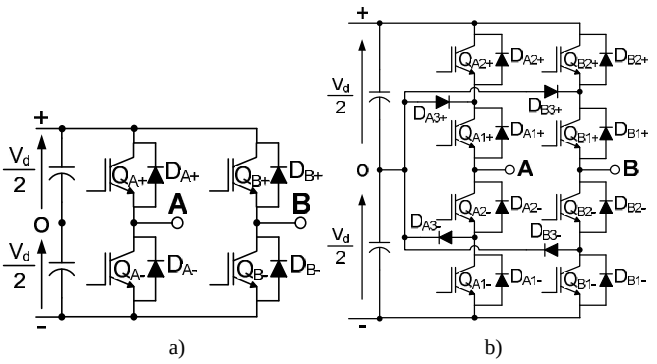

Fig. 1. Single-phase inverter topology: (a) Traditional two level inverter; b) Three level neutral point clamped inverter (NPC).

Considering a single branch, the output current, i_A, will pass from it to the load through A terminal. Usually, the transistors of a branch switch in a complementary way technique to avoid DC link short circuits (excepting shoot through strategies). The output current will always pass

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through a single semiconductor in the case of a TLI. The conducting semiconductor depends on the branch state and the direction of the current:

$$s_{A+}^{\text{TLI}}\begin{cases}=0=\text{St. }2 \;\Rightarrow\; V_{Ao,\text{TLI}}=-\dfrac{V_d}{2} & \begin{cases} i_A>0\Rightarrow D_{A-}, & (1)\\ i_A<0\Rightarrow Q_{A-}, & (2)\end{cases}\\ =1=\text{St. }1 \;\Rightarrow\; V_{Ao,\text{TLI}}=\dfrac{V_d}{2} & \begin{cases} i_A>0\Rightarrow Q_{A+}, & (3)\\ i_A<0\Rightarrow D_{A+}, & (4)\end{cases}\end{cases}$$

where s_{A+} is the switching signal of the transistor Q_{A+} (complementary to Q_{A-}), V_d is the DC link voltage and $V_{Ao,\text{TLI}}$ is the TLI output branch voltage with respect to the middle point of the DC link.

The current will flow through two different semiconductors in the case of the NPC:

$$\begin{matrix}s_{A2+}\\ s_{A1+}\\ \text{NPC}\end{matrix}\begin{cases}=\begin{pmatrix}0\\0\end{pmatrix}=\text{St. }3\Rightarrow V_{Ao,\text{NPC}}=-\dfrac{V_d}{2}\begin{cases} i_A>0\Rightarrow D_{A2-},\ D_{A1-}, & (5)\\ i_A<0\Rightarrow Q_{A2-},\ Q_{A1-}, & (6)\end{cases}\\ =\begin{pmatrix}0\\1\end{pmatrix}=\text{St. }6\;\Rightarrow\; V_{Ao,\text{NPC}}=0\begin{cases} i_A>0\Rightarrow D_{A3+},\ Q_{A1+}, & (7)\\ i_A<0\Rightarrow D_{A3-},\ Q_{A2-}, & (8)\end{cases}\\ =\begin{pmatrix}1\\1\end{pmatrix}=\text{St. }12\Rightarrow V_{Ao,\text{NPC}}=\dfrac{V_d}{2}\begin{cases} i_A>0\Rightarrow Q_{A2+},\ Q_{A1+}, & (9)\\ i_A<0\Rightarrow D_{A2+},\ D_{A1+}, & (10)\end{cases}\end{cases}$$

where s_{A2+} and s_{A1+} is the switching signal for transistors Q_{A2+} and Q_{A1+} respectively (Complementary to Q_{A2-} and Q_{A1-}), and $V_{Ao,\text{NPC}}$ is the NPC output branch voltage with respect to the middle point of the DC link.

The use of complementary signals switching involves the use of the branch valid states, so that the non-allowed states are avoided and the rest are used only for transitions. Table I and Table II shows the whole possible states of the branch for a TLI and NPC respectively.

TABLE I. POSSIBLE STATES ON A TLI BRANCH.

State	Q_{A+}	Q_{A-}	Comments
0	OFF	OFF	Only transitions
1	**ON**	**OFF**	**Valid state**
2	**OFF**	**ON**	**Valid state**
3	ON	ON	Not allowed

TABLE II. POSSIBLE STATES ON A NPC BRANCH.

State	Q_{A2+}	Q_{A1+}	Q_{A2-}	Q_{A1-}	Comments
0	OFF	OFF	OFF	OFF	Only transitions
1	OFF	OFF	OFF	ON	Only transitions
2	OFF	OFF	ON	OFF	Only transitions
3	**OFF**	**OFF**	**ON**	**ON**	**Valid state**
4	OFF	ON	OFF	OFF	Only transitions
5	OFF	ON	OFF	ON	Only transitions
6	**OFF**	**ON**	**ON**	**OFF**	**Valid state**
7	OFF	ON	ON	ON	Not allowed
8	ON	OFF	OFF	OFF	Only transitions
9	ON	OFF	OFF	ON	Only transitions
10	ON	OFF	ON	OFF	Only transitions
11	ON	OFF	ON	ON	Only transitions
12	**ON**	**ON**	**OFF**	**OFF**	**Valid state**
13	ON	ON	OFF	ON	Only transitions
14	ON	ON	ON	OFF	Not allowed
15	ON	ON	ON	ON	Not allowed

III. ANALYTIC LOSSES CALCULATION

Defining d_{A+} as the duty cycle for TLI transistor Q_{A+} and $(1\text{-}d_{A+})$ for its complementary one, the output mean voltage in a switching period is

$$V_{Ao,\text{TLI}}=\frac{V_d}{2}(2d_{A+}-1), \tag{11}$$

where V_d is the DC link voltage.

Subsequently, the duty cycle of Q_{A+} is

$$d_{A+}=\left(\frac{1}{2}+\frac{V_{Ao,\text{TLI}}}{V_d}\right). \tag{12}$$

For the NPC the switching period is divided into the three possible valid states, so d_+ is defined as the cycle fraction on state 12, d_o on state 6 and d_- on state 3

$$V_{Ao,\text{NPC}}=\frac{V_d}{2}d_+ +0d_o+\left(-\frac{V_d}{2}\right)d_-=$$
$$=\frac{V_d}{2}d_+ +\left(-\frac{V_d}{2}\right)d_-, \tag{13}$$

where $d_+ + d_o + d_- = 1$. Supposing a control technique based on PWM (see Fig. 2), a simplification could be introduced by taken into account the states when the output voltage is positive or negative. In the first case the state 12 is not used, and in the second case the state 3 is not used:

$$\text{Int. +: } d_-=0 \;\Rightarrow\; d_+ + d_o = 1 \;\Rightarrow\; V_{Ao,\text{NPC}}=$$
$$=\frac{V_d}{2}(1-d_o), \tag{14}$$

$$\text{Int. -: } d_+=0 \;\Rightarrow\; d_o + d_- = 1 \;\Rightarrow\; V_{Ao,\text{NPC}}=$$
$$=\frac{V_d}{2}(d_o-1). \tag{15}$$

The NPC duty cycles could be obtained in the two intervals:

$$\text{Int + } \Rightarrow\; d_o=1-\frac{2V_{Ao,\text{NPC}}}{V_d}, \tag{16}$$

$$\text{Int - } \Rightarrow\; d_o=1+\frac{2V_{Ao,\text{NPC}}}{V_d}. \tag{17}$$

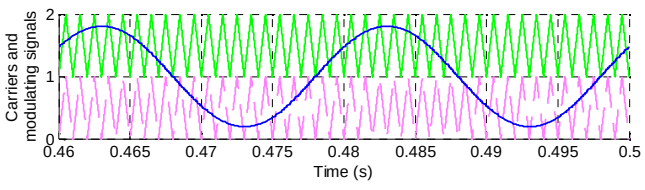

Fig. 2. PWM modulation in the NPC.

A. Conduction Losses

The semiconductor of an electronic switch (ES) presents a voltage drop that is function of the current flowing. Considering the first order function one has

$$v_{ES}=V_{ES,on}+r_{ES,on}I_A, \tag{18}$$

where $V_{ES,on}$ is the voltage drop of the ES when conducting

and $r_{es,on}$ is the conducting resistance. The conduction losses of an ES are

$$p_{on} = v_{ES} i_A = V_{ES,on} i_A + r_{ES,on} i_A^2. \quad (19)$$

The instantaneous conduction losses could be divided into two terms, one for the transistor with *ES* = *Q* and other for the diode with *ES* = *D*. Then, supposing identical semiconductors, the conduction losses for the TLI are:

$$I_{A,\mathrm{TLI}} \begin{cases} >0 \begin{cases} P_{QA+} = \left(V_{onQ} I_A + r_{onQ} I_A^2\right) d_{A+}, & (20) \\ P_{DA-} = \left(V_{onD} I_A + r_{onD} I_A^2\right)\left(1 - d_{A+}\right), & (21) \end{cases} \\ <0 \begin{cases} P_{QA-} = \left(V_{onQ} I_A + r_{onQ} I_A^2\right)\left(1 - d_{A+}\right), & (22) \\ P_{DA+} = \left(V_{onD} I_A + r_{onD} I_A^2\right) d_{A+}. & (23) \end{cases} \end{cases}$$

Doing the same way for the NPC and taking into account the positive and negative intervals:

$$I_{A,\mathrm{NPC}} \begin{cases} >0 \begin{cases} \text{Int. +} \Rightarrow \begin{cases} P_{QA2+} = \left(V_{onQ} I_A + r_{onQ} I_A^2\right)\left(1 - d_o\right), & (24) \\ P_{QA1+} = V_{onQ} I_A + r_{onQ} I_A^2, & (25) \\ P_{DA3+} = \left(V_{onD} I_A + r_{onD} I_A^2\right) d_o, & (26) \end{cases} \\ \text{Int. -} \Rightarrow \begin{cases} P_{QA1+} = \left(V_{onQ} I_A + r_{onQ} I_A^2\right) d_o, & (27) \\ P_{DA3+} = \left(V_{onD} I_A + r_{onD} I_A^2\right) d_o, & (28) \\ P_{DA2-} = \left(V_{onD} I_A + r_{onD} I_A^2\right)\left(1 - d_o\right), & (29) \\ P_{DA1-} = \left(V_{onD} I_A + r_{onD} I_A^2\right)\left(1 - d_o\right), & (30) \end{cases} \end{cases} \\ <0 \begin{cases} \text{Int. +} \Rightarrow \begin{cases} P_{QA2-} = \left(V_{onQ} I_A + r_{onQ} I_A^2\right) d_o, & (31) \\ P_{DA3-} = \left(V_{onD} I_A + r_{onD} I_A^2\right) d_o, & (32) \\ P_{DA2+} = \left(V_{onD} I_A + r_{onD} I_A^2\right)\left(1 - d_o\right), & (33) \\ P_{DA1+} = \left(V_{onD} I_A + r_{onD} I_A^2\right)\left(1 - d_o\right), & (34) \end{cases} \\ \text{Int. -} \Rightarrow \begin{cases} P_{QA2-} = \left(V_{onQ} I_A + r_{onQ} I_A^2\right), & (35) \\ P_{QA1-} = \left(V_{onQ} I_A + r_{onQ} I_A^2\right)\left(1 - d_o\right), & (36) \\ P_{DA3-} = \left(V_{onD} I_A + r_{onD} I_A^2\right) d_o. & (37) \end{cases} \end{cases} \end{cases}$$

The conduction losses in the *k-th* switching period could be determined through expression (20)–(21) for TLI and through (24)–(30) for NPC when the current is flowing out of the branch:

$$\begin{aligned} P_{on,\mathrm{TLI}}(k) &= P_{QA+} + P_{DA-} = \\ &= I_A\left(V_{onQ} d_{A+} + V_{onD}\left(1 - d_{A+}\right)\right) + \\ &+ I_A^2\left(r_{onQ} d_{A+} + r_{onD}\left(1 - d_{A+}\right)\right), \quad (38) \\ P_{on,\mathrm{NPC}}(k) &= P_{QA2+} + P_{QA1+} + P_{DA3+} + \\ &+ P_{DA2-} + P_{DA1-} = \\ &= I_A\left(V_{onQ}\left(2d_{A+} + d_o\right) + 2V_{onD}\left(d_o + d_-\right)\right) + \\ &+ I_A^2\left(r_{onQ}\left(2d_{A+} + d_o\right) + 2r_{onD}\left(d_o + d_-\right)\right), \quad (39) \end{aligned}$$

Substituting the duty cycle obtained in (12) into (38)

$$P_{\underset{TLI}{on}}(k) = I_A(k)\left(\frac{V_{onQ} + V_{onD}}{2} + \frac{V_{onQ} - V_{onD}}{V_d} V_{Ao}(k)\right) + I_A^2(k)\left(\frac{r_{onQ} + r_{onD}}{2} + \frac{r_{onQ} - V_{onD}}{V_d} V_{Ao}(k)\right). \quad (40)$$

Knowing that the positive interval is symmetric with respect to the negative interval in most of the PWM, the NPC conduction losses are calculated with (16) and (39)

$$\begin{aligned} P_{\underset{\mathrm{NPC}}{on}}(k) &= I_A(k)\left(V_{onQ} + V_{onD} + \right. \\ &\left. + \frac{2\left(V_{onQ} - V_{onD}\right)}{V_d} V_{Ao}(k)\right) + \\ &+ I_A^2(k)\left(r_{onQ} + r_{onD} + \frac{2\left(r_{onQ} - r_{onD}\right)}{V_d} V_{Ao}(k)\right). \quad (41) \end{aligned}$$

The expressions (40) and (41) obtained are similar when the current flows into the branch, so a general expression is taken for each converter:

$$P_{\underset{TLI}{on}}(k) = \left|I_A(k)\right|\left(\frac{V_{onQ} + V_{onD}}{2} + \frac{V_{onQ} - V_{onD}}{V_d} V_{Ao}(k)\right) + I_A^2(k)\left(\frac{r_{onQ} + r_{onD}}{2} + \frac{r_{onQ} - V_{onD}}{V_d} V_{Ao}(k)\right), \quad (42)$$

$$P_{\underset{\mathrm{NPC}}{on}}(k) = \left|I_A(k)\right|\left(V_{onQ} + V_{onD} + \frac{2\left(V_{onQ} - V_{onD}\right)}{V_d} V_{Ao}(k)\right) + I_A^2(k)\left(r_{onQ} + r_{onD} + \frac{2\left(r_{onQ} - r_{onD}\right)}{V_d} V_{Ao}(k)\right). \quad (43)$$

The difference between the expression of the NPC and the TLI is a factor of 2, so the conduction losses will be the double for the same semiconductor.

B. Switching Losses

The switching losses could be determined by knowing the energy a semiconductor needs to switch on and switch off, which is a parameter that could be found in the datasheet. These parameters are E_{on} and E_{off} for the transistor switching and E_{rr} for the diode reverse energy recovery. These energies depend on the current that flows through the semiconductor and they are usually defined for a reference voltage, V_{ref}, and a reference current, I_{ref}.

Calculations could be simplified here by assuming a lineal relation between the energies and the current, so in any switching period one has:

– The TLI presents the switching transitions detailed in Table III. The switching losses are then

$$P_{sw}(k)=\left(E_{on}+E_{off}+E_{rr}\right)f_s\frac{|I_A(k)|V_d}{I_{ref}V_{ref}}, \quad (44)$$

where f_s is the switching frequency.

– The NPC has more switching transitions as it can be seen in Table IV. However, only switching 0, 2, 3 and 5 are used with symmetric PWM modulation. The switching losses for the NPC are

$$P_{sw}(k)=\left(E_{on}+E_{off}+(1+s)E_{rr}\right)f_s\frac{|I_A(k)|V_d}{I_{ref}V_{ref}}, \quad (45)$$

where s is a boolean that is one when two diodes switch in a switching period.

C. Total Losses

Total losses are obtained with the next expression:

$$P=\frac{1}{NT_s}\sum_{k=1}^{N}\left(P_{on}(k)+P_{sw}(k)\right). \quad (46)$$

where N is the number of switching periods in a modulated waveform period and T_s is the switching period.

TABLE III. POSSIBLE SWITCHES OF A TLI BRANCH.

Switch	Transition	i_a	Switch ON	Switch OFF
0	1 → 2	> 0	Q_{A+}, D_{A+}	Q_{A-}, D_{A-}
		< 0	Q_{A+}, D_{A+}	Q_{A-}, D_{A-}
1	2 → 1	> 0	Q_{A-}, D_{A-}	Q_{A+}, D_{A+}
		< 0	Q_{A-}, D_{A-}	Q_{A+}, D_{A+}

TABLE IV. POSSIBLE SWITCHES OF A NPC BRANCH.

Switch	Transition	i_a	Switch ON	Switch OFF
0	3 → 6	> 0	Q_{A1+}, D_{A1+}, D_{A3+}	Q_{A1-}, D_{A1-}
		< 0	D_{A3-}	Q_{A1-}, D_{A1-}
1	3 → 12	> 0	Q_{A2+}, D_{A2+}, Q_{A1+}, D_{A1+}	Q_{A2-}, D_{A2-}, Q_{A1-}, D_{A1-}
		< 0	Q_{A2+}, D_{A2+}, Q_{A1+}, D_{A1+}	Q_{A2-}, D_{A2-}, Q_{A1-}, D_{A1-}
2	6 → 3	> 0	Q_{A1-}, D_{A1-}	Q_{A1+}, D_{A3+}
		< 0	Q_{A1-}, D_{A1-}	D_{A3-}
3	6 → 12	> 0	Q_{A2+}, D_{A2+}	D_{A3+}
		< 0	Q_{A2+}, D_{A2+}	Q_{A2-}, D_{A2-}, D_{A3-}
4	12 → 3	> 0	Q_{A2-}, D_{A2-}, Q_{A1-}, D_{A1-}	Q_{A2+}, D_{A2+}, Q_{A1+}, D_{A1+}
		< 0	Q_{A2-}, D_{A2-}, Q_{A1-}, D_{A1-}	Q_{A2+}, D_{A2+}, Q_{A1+}, D_{A1+}
5	12 → 6	> 0	D_{A3+}	Q_{A2+}, D_{A2+}
		< 0	Q_{A2-}, D_{A2-}, D_{A3-}	Q_{A2+}, D_{A2+}

Note: Semiconductors that switches in black, and the rest in grey.

If the switching period, T_s, is much smaller than the waveform period, T, one has

$$P=\frac{1}{T}\int_0^T\left(P_{on}(t)+P_{sw}(t)\right)dt. \quad (47)$$

IV. Losses Model

Fig. 3 and Fig. 4 depict the designed conduction and switching losses model. These models calculate the losses in a more exhaustive way, that is, no symmetric PWM intervals for conduction and switching losses simplification are added. Both figures details the losses calculation for both TLI and NPC (symbol "\" separates each case).

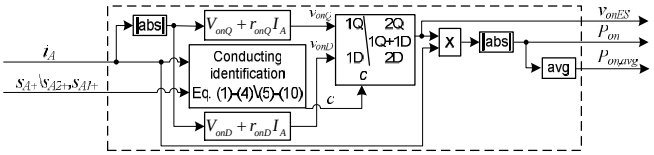

Fig. 3. Designed conduction losses model for TLI and NPC.

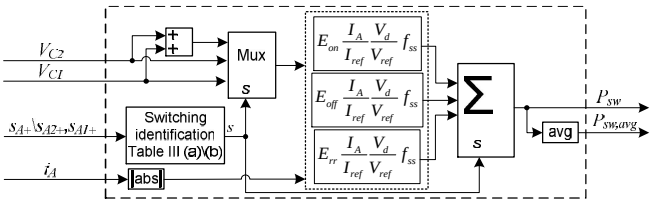

Fig. 4. Designed switching losses model for TLI and NPC.

The conduction losses model (Fig. 3) solves expressions (18) and (19) depending on the conducting semiconductor, which is identified through (1)–(4) and (5)–(10) by indexing them with c for each converter. The voltage drop is used in the voltage applied to the load.

The switching losses model (Fig. 4) identifies the switching semiconductor by means of Table III and Table III (where the first columns are the s selector) and adds the power losses of each one (see (44) and (45)).

V. Inverter Losses with Sinusoidal PWM

A sinusoidal PWM technique for single phase inverters with inductive loads (Fig. 5) has been studied to evaluate the losses. The values of the system are resumed in Table V, and the parameters of the semiconductors correspond to the SK80GB125T device [7] for the TLI and the SK75MLI066T device [9] for the NPC.

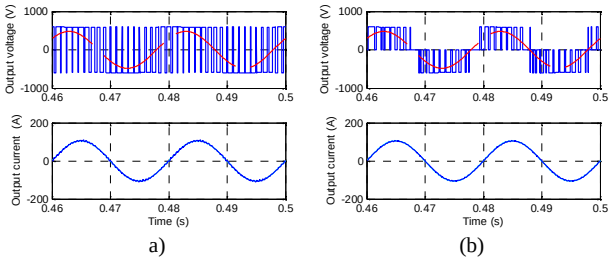

Fig. 5. Voltage and current of a branch modulated with PWM together with the fundamental component voltage and the current reference respectively: (a) TLI; (b) NPC.

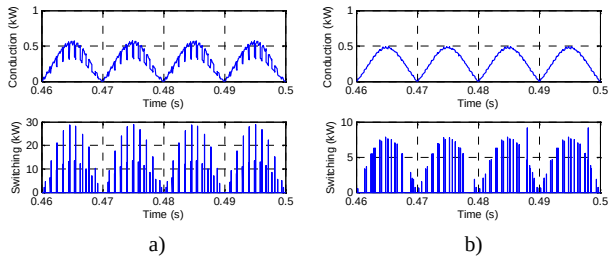

Fig. 6. Conduction and switching losses of a single phase inverter with PWM modulation. (a) TLI and (b) NPC.

TABLE V. OPERATION CONDITIONS.

DC Link voltage	1200 V	Power factor	0.8
Load current	75 A	Modulation index	0.8
Inductor resistance	7 Ω	Switching frequency	1 kHz
Inductance	18 mH	Waveform frequency	50 Hz

A. Analytic Solution

Expressions (42)–(45) could be applied here assuming the next voltage and current components with a φ gap and a modulation index of m_a:

$$\begin{cases} I_{A,1}(\theta) = \sqrt{2} I_A \sin\theta, \\ V_{Ao,1}(\theta) = \sqrt{2} V_A \sin(\theta + \varphi), \end{cases} \tag{48}$$

$$V_{Ao,\mathrm{TLI}} = m_a V_d \sqrt{2}/4, \tag{49}$$

$$V_{Ao,\mathrm{NPC}} = m_a V_d \sqrt{2}/2, \tag{50}$$

so, integrating the expressions one has the losses:

$$P_{on,\mathrm{TLI}} = I_A \left[0.9 \left(\frac{V_{onQ} + V_{onD}}{2} \right) + \left(V_{onQ} - V_{onD} \right) \frac{V_{Ao}}{V_{dc}} \cos\varphi \right] + I_A^2 \left[\left(\frac{r_{onQ} + r_{onD}}{2} \right) + \frac{8\sqrt{2}}{3\pi} \left(r_{onQ} - r_{onD} \right) \frac{V_{Ao}}{V_{dc}} \cos\varphi \right], \tag{51}$$

$$P_{on,\mathrm{NPC}} = I_A \left(0.9 \left(V_{onQ} + V_{onD} \right) + 2 \left(V_{onQ} - V_{onD} \right) \frac{V_{Ao}}{V_{dc}} \cos\varphi \right) + I_A^2 \left(r_{onQ} + r_{onD} + \frac{16\sqrt{2}}{3\pi} \left(r_{onQ} - r_{onD} \right) \frac{V_{Ao}}{V_{dc}} \cos\varphi \right), \tag{52}$$

$$P_{sw,\mathrm{TLI}} = \left(E_{on} + E_{on} + E_{rr} \right) 0.9 f_s \frac{I_A}{I_{ref}} \frac{V_d}{V_{ref}}, \tag{53}$$

$$P_{sw,\mathrm{NPC}} = \left(E_{on} + E_{on} + \left(1 + \frac{\varphi}{\pi} \right) E_{rr} \right) 0.9 f_s \frac{I_A}{I_{ref}} \frac{V_d}{V_{ref}}. \tag{54}$$

where the NPC *s* term is the fraction of time when is one.

B. Model Simulation

The model has been simulated with the same configuration the analytical solution had, so it could be validated. The instantaneous conduction and switching losses are shown in Fig. 6(a) and Fig. 6(b) for the TLI and for the NPC. By doing the mean value of the total losses, a result with a deviation of tenths with respect to the analytical solution ((51)–(54)) is obtained, so the model is validated.

VI. CONCLUSIONS

In this work a generic model for calculating the losses of a traditional inverter and a neutral point clamped inverter. The models are based on the semiconductors equations so any device could be evaluated by introducing their parameters from the datasheet.

The model was validated by matching the results with the ones obtained analytically for a typical symmetrical PWM. The model could allow optimizing power application by analysing the inverter losses. A great benefit of the designed models is that they provide a result whatever the control strategy is, not only PWM, as they did not need any simplification, something that is very hard to achieve with an analytical development. Also, the method could be applied to an inverter of *n* levels in general.

The models also allow comparing the losses of each studied converter in order to evaluate which is better for the user. The conduction losses seems the double for the NPC however the semiconductors could be the half blocking voltage with respect to the TLI so it presents better parameters. With the same premise one has that the switching losses will be less for the NPC so it will have less semiconductor stress at the same switching frequency. As the switching frequency increases, the conduction losses are the less important term so the NPC could be a better choice.

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