Improved Power Supply Performance of Vibratory Conveyor Drives

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***Abstract*—A practically realized solution of a power supply for vibratory conveyor drives is presented. The solution is an improvement from the quality of electrical energy point of view. An analysis is given of the AC/DC converter used as the input active filter serving for reduction of the undesired higher harmonics of the input (network) current and improvement of the power factor. The experimental results are presented together with an analysis of the characteristic waveforms (oscilloscopic records of the network voltage and current) at steady state, obtained by the realized converter.**

***Index Terms*—Vibratory-conveyor drive; AC/DC converter; power factor correction.**

I. INTRODUCTION

An ever increasing application of modern electronic converters in regulated electric drives in the recent years, seriously affects the quality of electrical energy. Input currents of these converters have complex periodic waveforms creating harmonic distortions, while the voltage is approximately of sine-wave shape [1]. Current-voltage ratio is nonlinear, thus these consumers are characterized as nonlinear loads. Harmonics in a supply network have negative influence upon other equipment supplied by the same network [2], [3].

An intensive work has been recently put in the development of high-frequency (HF) transistor power converters with tracking sine-wave reference [4]–[6] in order to obtain sine half-wave of current in the coil of electromagnetic vibratory actuator (EVA) used in vibratory-conveying drives (VCD) [4], [7].

Vibratory conveyors are widely applied in many technological processes involving gravimetric transport, processing, and dosing of granular materials. From the macroscopic point of view, the process of vibratory conveyance is based on recurrent micro-throws of particles of the material being conveyed [8]–[11]. A typical vibratory conveyor in a system of dosing granular material is shown in Fig. 1.

Topologies involving two switching transistors and two feedback diodes have mainly been adopted: *forward* topology having an asymmetric half-bridge and symmetric *half-bridge* topology as shown in Fig. 2(a) and Fig.2(b), respectively. In some cases, is applied the full-bridge topology (Fig. 2(c)) [12].

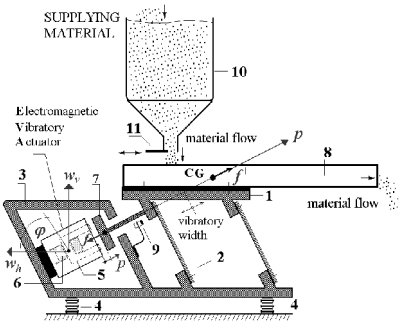


Fig. 1. Vibratory conveyor having electromagnetic drive [12]: 1 – load carrying element (LCE), 2 – elastic elements, 3 – base, 4 – rubber supports, 5 – magnetic core, 6 – electrical coil, 7 – armature, 8 – vibrating trough, 9 – inductive sensor, 10 – storage hopper, 11 – movable shutter.

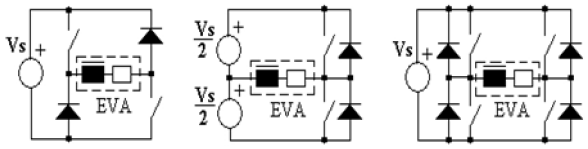


Fig. 2. Switching converter topologies for EVA excitation: (a) – the asymmetric half-bridge, (b) – the symmetric half-bridge; (c) – the full-bridge [12].

The required half-wave of EVA current can be realized by using these topologies, provided the current control is based on tracking a sine-wave reference and adjust duration time, amplitude and frequency. This way of generating excitation has the advantage that one can achieve independent adjustments of the frequency and amplitude of the electromagnetic force of EVA which driving mechanical oscillatory circuit of VCD [4].

Despite the significant benefits, HF transistor converters have a disadvantage that at high frequencies their switching losses become dominant. This reduces the efficiency of VCD's. The switching losses, which more dominate then the "on-state" losses in the HF transistor power converter, originate due to switching commutation between the power switches (standard MOS HEXFET) and ultra-fast free-wiling diodes (topology in Fig. 2(a)), or between the power

Manuscript received 12 September, 2015; accepted 14 October, 2016.
This research was funded by a grant No: TR 33022 from the Ministry of Education, Science and Technological Development of Republic Serbia.

switches in the half/full bridge application (topologies in Fig. 2(b), Fig. 2(c)). These losses are proportional to the switching frequency and may be significant (up to 70 %) reduced using modern switching components such as super junction MOSFET's [13]–[15] and SiC Shotki barrier diode (SBD) [16]–[17]. Also, these losses can be reduced by using resonant half/full bridge topology of power converter or applied standard half/full bridge topology in which can provide a resonant gate drive of the power switch [18]–[19]. For example, a possible solution for obtaining smooth sine half-wave current of EVA (excluding high-frequency ripple) using a resonant half-bridge switching power converter is given in detail into reference [20].

The problem may be overcome by applying a suitable method of control whereby the mentioned topologies are used, but the excitation of EVA, instead by sinusoidal, is accomplished by low frequency triangular current pulses. In general, the operating frequency range of majority of VCDs is from 20 Hz to 150 Hz [21].

The mentioned switching topologies for driving VCDs require dc voltage supply. Therefore, for power supplies from a 50 Hz network using a diode rectifier provided by a »*bank*« of electrolytic capacitors in the dc-link circuit is applied. It is well known that power factor of this module is very poor. In addition, the input current is rich of harmonics [22].

From the above mentioned reasons, an additional requirement, the optimization of the input rectifier circuit as a part of the global optimization of a VCD, is required in order to reduce harmonic content of the input current and improve the power factor. This is significant from several points of view, the two being very important: energy saving and satisfying the requirements set by the standards being introduced. Power factor correction is of particular significance for high power VCDs or for several low power vibratory conveyors operating within the system. This case is very often encountered in the processing industry and practice.

Several topologies allow improving power factor and reduction of harmonic content of the current. The most popular and most often used is the conventional *boost* topology. Considered in many references, it became almost a standard. Several types of integrated controllers and circuits used for controlling this type of converters are available at the market.

II. Optimization of Topology of VCD Input Rectifier

Despite wide usage of *boost* topology (Fig. 3) and advantages it offers as regards realization of rectifiers incorporating power factor correction (PFC), there are several serious shortcomings: a relatively high switching frequency is required leading to increased power losses and reduced efficiency; a diode connected in series with the load causes an additional voltage drop and additional loses, since in one half-wave of the main power circuit there are three voltage drops (two in the rectifier and one in the converter); using a choke in the dc-link circuit implies a dc current in its windings, which may lead to magnetic saturation; high frequency ripple of this current may increase power losses in iron [23]–[24]. It is considered that the active resistance of the winding is significantly less than the reactance.

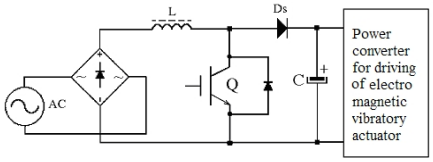


Fig. 3. Conventional "boost" circuit of a PFC rectifier.

A new type of converter having a higher efficiency and which allows a considerable improvement of the input power factor and reduction of harmonic content in the supply network has been proposed in [4], [23]–[25]. Block diagram of such high performance single phase rectifier is shown in Fig. 4.

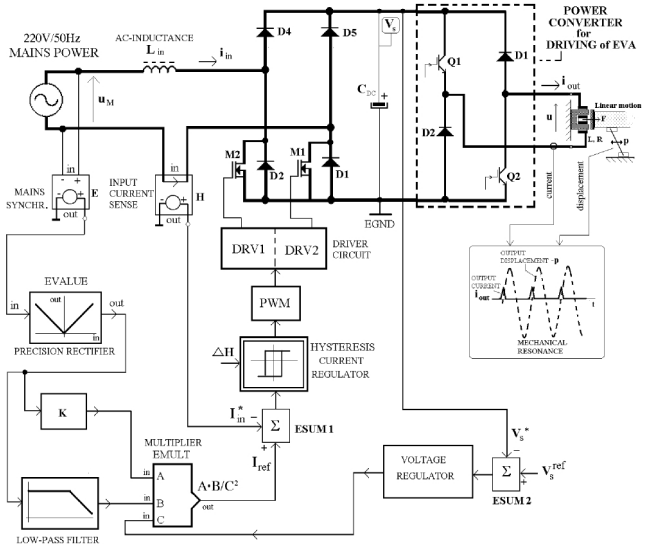


Fig. 4. Single phase rectifier comprising the input PFC circuit.

Series diode Ds of *boost* topology has been rejected. The role of this diode takes over the diodes in the rectifier bridge. A choke is not required on the dc side, but is relocated to the side of the ac supply network. The advantages of the presented topology compared to other topologies are that there are only two voltage drops across semiconductor elements in the main power flow circuit (one transistor and one diode); currents of transistors M1 and M2 are relatively small; since the choke is on the ac side, there are no problems associated with saturation; electromagnetic interference is significantly reduced; excitation of transistors M1 and M2 is simple since the transistors and the corresponding driving circuits have common power ground in the dc-link circuit.

This converter consists of two *boost* converters: one comprising MOSFET transistor M1 and diode D5 and the other comprising MOSFET transistor M2 and diode D4. Common choke L_{in} is positioned at the side of the supply network, while the dc-link circuit contains capacitor C_{DC}.

The advantage of this converter compared to the classical *boost* converter, containing one transistor and a diode rectifier, is that its operating losses are considerably lower. This converter can operate in two different regimes which will be considered in more details.

In operating *mode* I, shown in more details in Fig. 5, at

each half-period of the supply voltage one of the two MOSFETs is conducting throughout the half-period, while the other is operating in the switching mode within the voltage booster. During positive half-period of the supply voltage, shown in Fig. 5(a), M1 is conducting all the time, while M2 operates in the switching mode. During negative half-period of the supply voltage, shown in Fig. 5(b), M2 is conducting throughout, while M1 operates in the switching mode.

Current in the transistor conducting throughout the half-period flows in the inverse direction, from source to drain, i.e. the main part of the current will flow through its channel, not through the inversely biased diode integrated in its structure. Total voltage drop in the conducting loop consists of the voltage drop across two semiconductor elements: directly conduction MOS transistor or the *boost* diode, and the inversely conduction MOS transistor. Figure 5(c) shows signals at the gates of transistors M1 and M2 and synchronization of the driving signals with the supply voltage. This operating mode, in view of the driving signals at the gate of the switching transistor, is more complex compared to the operation of a conventional *boost* converter containing one transistor and one diode.

In operating *mode* II, shown in Fig. 6, both transistors M1 and M2 are simultaneously switched on and off during each half-period of the line voltage. During positive half-period of the line voltage, current flows through M2 in forward and through M1 in inverse direction, as shown in Fig. 6(a). When both transistors are in "off-state" current flows through diode D4 and internal inverse diode of M1. A similar sequence of events occurs during negative half-period of the network voltage, when current flows through M1 in forward and through M2 in inverse direction, as shown in Fig. 6(b). When both transistors are in "off-state", current flows through diode D5 and through internal inverse diode of M2. This operating mode is characterized by smaller conductive losses compared to those of mode I. The total voltage drop in the conducting loop is across two semiconductor elements. Figure 6(c) shows waveforms of the driving voltage at the gates of transistors M1 and M2. It can be seen that no special logic is required since both transistors are driven simultaneously. In addition, this operating regime is accessible to the functions of the most PFC circuits, available at the market. This operating mode has been implemented in the practical realization of the input AC/DC converter, supplying the asymmetric half-bridge power converter of EVA.

The described topology of the input PFC rectifier represents a possible solution leading to optimization of the power of VCD's. A shortcoming of this topology is high commutation losses of transistor M1 and diode D5, also of transistor M2 and diode D4. These losses are particularly significant at high frequencies which are usual in practical applications (40 kHz–100 kHz) [23]. One of the methods for reducing these losses is introduction of an additional resonant circuit in the dc-link circuit which provides "*soft*" commutation between the mentioned transistors and diodes. One such converter applying a similar topology for reducing commutation losses is presented in [24].

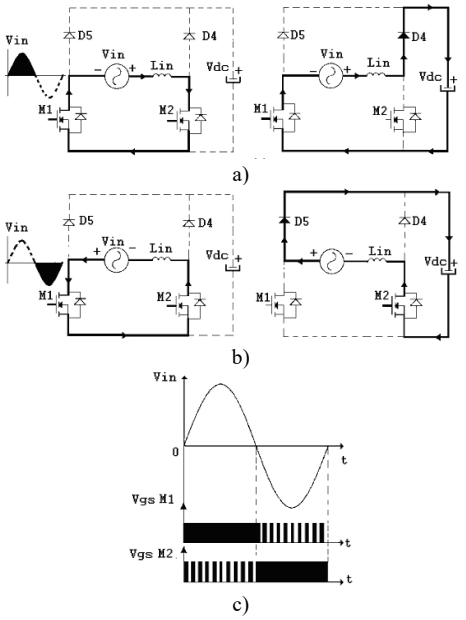


Fig. 5. Topology of PFC rectifier operating in mode I: (a) – positive half-period of the line voltage; (b) – negative half-period of the network voltage; (c) – synchronization of driving signals with the line voltage.

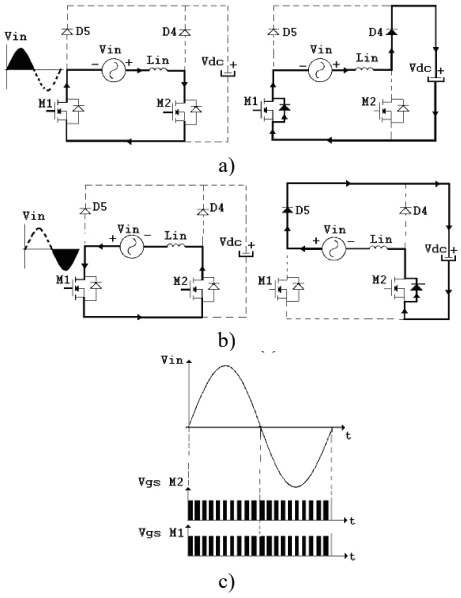


Fig. 6. Topology of PFC rectifier operating in mode II: (a) – negative half-period of the line voltage; (b) – negative half-period of the line voltage; (c) – synchronization of driving signals with the network voltage.

The proposed PFC circuit provides a favourable harmonic content of the input current and considerably reduces the input reactive power of VCD. In addition, the voltage regulated rectifier containing PFC circuit eliminates the effects of line voltage variations to performance of VCD.

III. SIMULATION RESULTS

The simulation results of the characteristic values of the regulated rectifier of Fig. 4 are shown in Fig. 7. The simulation has been realized by using software package PSPICE. The considered variables were: input voltage, input current, voltage of the dc-link circuit, and output current which supplying EVA coil. The presented results correspond to the case of asymmetric half-bridge converter with half-wave triangular output current.

Irrespective of the triangular form of the current wave at

the output, by applying the described topology of the input rectifier (AC/DC) it is accomplished that the input current is sinusoidal and in phase with the input voltage, therefore the converter takes only active power from the network line.

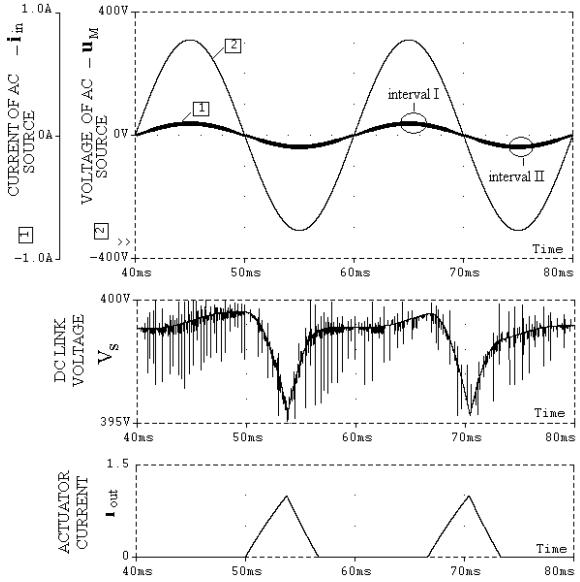


Fig. 7. Characteristic waveforms for a single phase PFC rectifier supplying regulated VCD.

This power is used for covering the losses in the converter itself, in resistance of the EVA coil, and active losses of the mechanical oscillatory system (damping and friction of the conveying material).

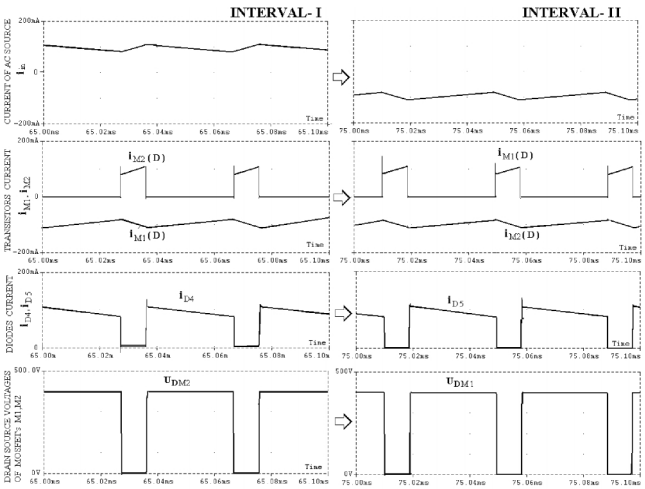


Fig. 8. Detailed scope of the simulation waveforms for intervals I and II.

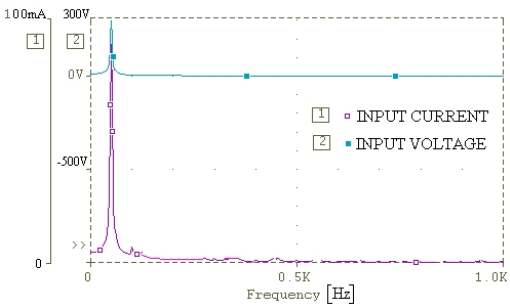


Fig. 9. Fourier spectra of the input voltage and current of a single phase PFC rectifier.

Figure 8 shows in detail the intervals denoted in Fig. 7. *Interval* I which correspond to the positive half-period of the supply voltage, while *interval* II corresponds to the negative half-period of the supply voltage. The switching frequency of transistors M1 and M2 in this simulation has been set to f_{sw} = 33.33 kHz.

Fourier spectra of the input voltage and current of the PFC rectifier obtained by the simulation are shown in Fig. 9.

IV. EXPERIMENTAL RESULTS

The PFC rectifier that is applied to the AC/DC power of regulated VCD drive, which is described in this paper, is with the input voltage range 85 V–264 V, 50 Hz. In the rectifier are used as switches HEXFET transistors (IRF 450) and ultra-fast diode MUR 460. The operating switching frequency of converter amounted 33.33 kHz and dc-link voltage +400 VDC. Its rated power was 100 W, and the bridge-less AC/DC rectifier is adapted to the regulated VCD drive in order to improve its input characteristics, which are in accordance with the European standard IEC61000-3-2. This was also the requirements that should fulfil of the input power of the regulated VCD in terms of power quality

The experimental results for a PFC input rectifier have been obtained for two characteristic cases of current half-waves supplying to EVA coil: sinusoidal and triangular.

Figure 10 shows oscilloscopic records of the line voltage and current at steady state when a full load 100W has been connected to output. The Fig. 10 shows that current is of a fine sinusoidal shape of amplitude I_{in_max} = 0.7 A, i.e. of the rms value I_{in} = 0.5 A. The current ripple was about Δi = 0.03 A which is in a relatively good agreement with the calculated value for the above switching frequency. The current is in phase with the mains voltage.

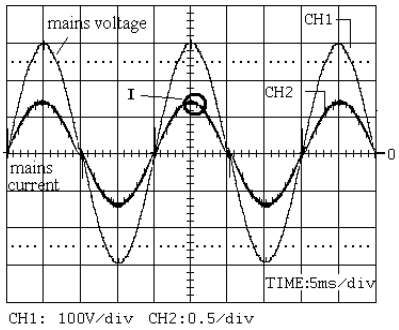


Fig. 10. The input voltage and current of a VCD having power factor correction in the input AC/DC converter.

Detailed presentation of the voltage and current of the input PFC rectifier for time *interval* I (Fig. 10) is given by oscilloscopic records on Fig. 11.

Figure 11(a) shows commutation between MOS transistor M1 and diode D3 during positive half-period of the supply voltage. Current peaks in both waveforms are the consequence of the reverse recovery of the diode. They are very short, but their influence upon dissipation is strong and their contribution to the losses is prevalent. Duty cycle of the current of transistor M2 is 0.27 (9μs/33μs).

Conduction time of *boost* diode D3 is 24 *μs*. Figure 11(b) shows waveforms of the drain current of MOS transistors M1 and M2. While current through input choke L_{in} is growing, transistor M2 is in forward conduction, while transistor M1 conducts in the inverse direction. In this case

voltage of the drain of transistor M1 is approximately V_{DS} (M1) ≈ -0.2 V at drain current I_D(M1) = 0.7 A. It should be mentioned that within this interval most of the drain current is taken over by transistor M1 while only a small part of the current flows through its inverse diode, since the diode is then forward biased by a small voltage of approximately 0.2 V. Upon removal of driving voltages at the gates of both transistors, they are turned off. Then drain voltage of M2 very quickly rises to +400 V, while drain voltage of M1 becomes approximately equal to V_{DS} ≈ -0.7 V. This is a consequence of conduction of its inverse diode when drain voltage of M1 is equal to the negative value of the voltage drop across its inverse diode. This is confirmed by oscilloscopic records of Fig. 11(c) which shows waveforms of the drain current and drain-source voltage of transistor M1.

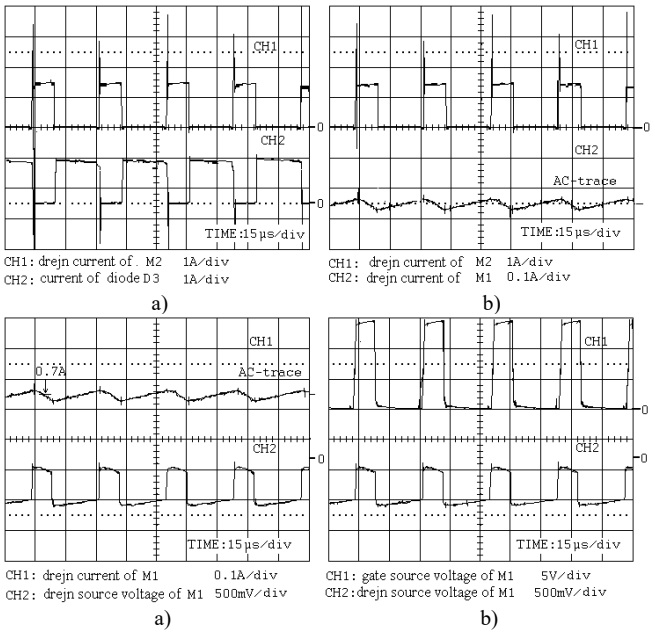


Fig. 11. Detailed oscilloscopic records of the characteristic voltages and currents of the input PFC converter within the specified *interval* I: (a)-drain current of transistor M2 and current of diode D3; (b)-currents of transistors M1 and M2; (c)-drain current voltage between drain and source of transistor M1; (d)-gate-source and drain-source voltages of transistor M1.

Relation between the driving gate voltage and drain voltage of transistor M1 is shown in Fig. 11(d). It can clearly be seen that upon removal of gate voltage of M1, its conduction is stopped and the current is taken over by its inverse diode.

It should be mentioned that qualitatively and quantitatively the waveforms are the same for the negative half-period of the supply voltage, except that in this case transistor M1 will be in forward conduction, transistor M2 will be in inverse conduction, while the commutation will occur between transistor M1 and diode D4.

Figure 12 shows oscilloscopic records of the input current and voltage (the characteristics of the input part of the system), output current (current of the EVA), and voltage of the dc-link circuit for the frequency of the output excitation current f_{exc} = 50 Hz.

Figure 13 presents oscilloscopic records of the input current of VCD for the case when a resonant regime is realized at frequency f_{res} = 70.5 Hz. The frequency of EVA excitation current is adjusted to approximately the same value as resonant frequency, i.e. f_{exc} = 70 Hz ≈ f_{res}. The Fig. 13(a) shows that there is no distortion of the input current as in the case when voltage of the dc-link circuit is obtained by a diode rectifier and a bank of electrolytic capacitors. The input current is a sinusoidal containing a high frequency ripple. Input power taken by the VCD from the line, for the recorded values of input current and supply voltage, is in this case only P_{in} ≈ 8 W since a resonant regime is present.

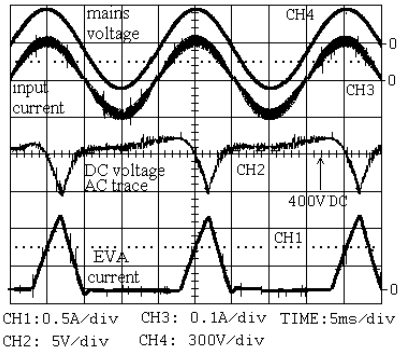


Fig. 12. The characteristic waveforms for the case when EVA coil is supplying by sinusoidal half-wave of frequency f_{exc} = 50 Hz: (a)-supply voltage and input current; (b)- output current and voltage of the dc-link circuit.

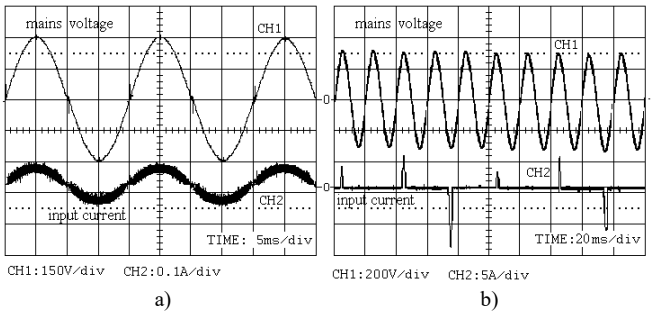


Fig. 13. Oscilloscopic records of the input variables of VCD for the case of the excitation frequency f_{exc} = 70 Hz; C_{DC} = 220 µF: (a)-PFC input rectifier; (b)-full wave diode rectifier.

Figure 14 shows oscilloscopic records of the input current of VCD for the case when the resonance regime is realized at frequency f_{res} = 30.2 Hz. The frequency of EVA excitation current was f_{exc} = 30 Hz ≈ f_{res}. Figure 14(a) shows waveforms of the input current the converter takes from the line, output current of the converter, and voltage of the dc-link circuit when EVA coil is driven by sinusoidal current half-waves at 33.33 kHz frequency. Input power in this case was P_{in} = 6 W.

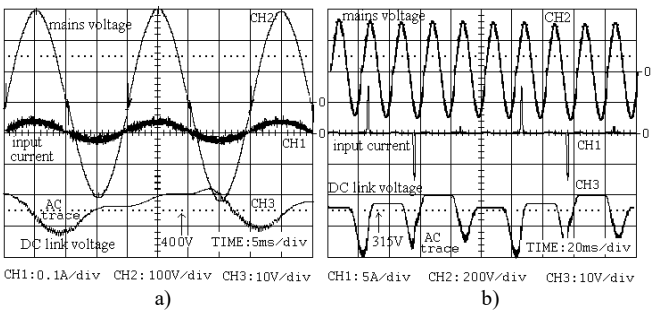
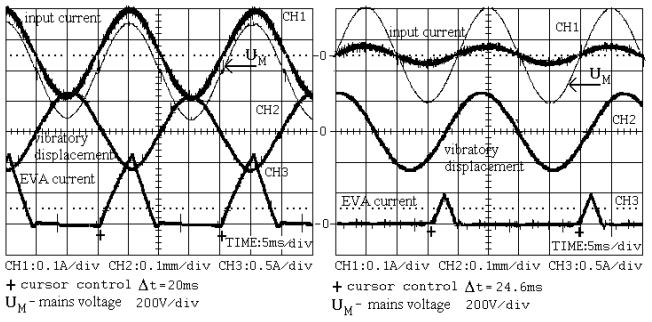


Fig. 14. Oscilloscopic records of the input variables of VCD for the case of the excitation frequency f_{exc} = 30 Hz; C_{DC} = 220 µF: (a)-a PFC input rectifier; (b)-a full wave diode rectifier.

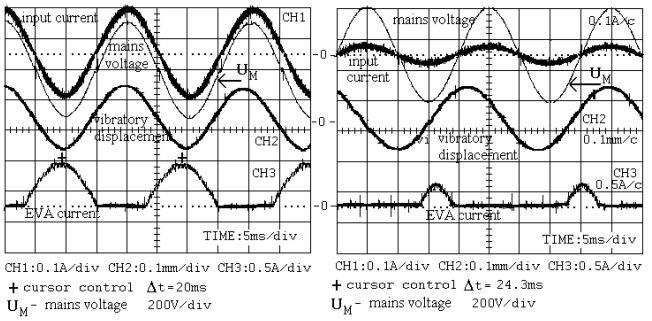
Figure 14(b) shows oscilloscopic records of the same variables as in the previous case, but for an input full wave diode rectifier. Compared to the previous case, when input current was in phase with the supply voltage, the input current consists of asymmetric pulses with a quite unfavourable harmonic content.

Favourable influence of the resonant regime of VCD on power taken from the line, for excitations of EVA coil by triangular and sinusoidal half-waves, is shown by oscilloscopic records on Fig. 15 and Fig. 16, respectively. In the presented cases, excitation frequency is higher or equal than the mechanical resonant frequency.



a) b)

Fig. 15. Influence of the operating regime of a VCD, having EVA coil driven by triangular half-wave, on input current: (a)-super-resonant regime - $f_{exc} > f_{res}$ = 40.6 Hz and f_{exc} = 50 Hz; (b)-resonant regime $f_{esc} = f_{res}$ = 50 Hz.



a) b)

Fig. 16. Influence of the operating regime of a VCD, having EVA coil driven by sinusoidal half-wave, on input current: (a)-super-resonant regime - $f_{exc} > f_{res}$ = 40.4 Hz and f_{exc} = 50 Hz; (b)-resonant regime $f_{esc} = f_{res}$ = 50 Hz.

Specifically, Fig. 15(a) shows the state when the vibratory conveyor was loaded by a mass of Δm_k = 0,62 kg. In this case the mechanical resonance frequency was f_{rez} = 40.6 Hz.

For the purpose of maintaining the value of vibratory width of P_{p-p} = 0.24 mm at excitation frequency f_{exc} = 50 Hz of a sinusoidal half-wave, amplitude I_m = 1.2 A and length τ = 10 ms of EVA current was required. In this process consumption of electrical energy was approximately $P_{in} \approx$ 25 W, easily obtainable form the voltage and current values on the oscilloscopic record.

Figure 15(b) shows the case when, by applying current control, frequency of the excitation current was adjusted to the value of mechanical resonant frequency of the vibratory system. In this case for maintaining the amplitude of oscillations, i.e. vibratory width, a sinusoidal half-wave of amplitude I_m = 0.5 A and length τ = 4 ms of EVA current, was required. In this process consumption of electrical energy was approximately $P_{in} \approx$ 6.3 W.

Specifically, Fig. 16(a) shows the case when the vibratory conveyor was loaded by a mas of Δm = 0.63 kg. In this case the mechanical resonant frequency of the system was f_{rez} = 40.4 Hz. For the purpose of maintaining the value of vibratory width of P_{p-p} = 0.2 mm at excitation frequency of f_{exc} = 50 Hz a sinusoidal half-wave of amplitude I_m = 0.7 A and length τ = 12 ms of EVA current, was required. In this process consumption of electrical energy was approximately $P_{in} \approx$ 23 W, easily obtainable form the voltage and current values on the oscilloscopic record.

Fig. 16(b) shows the case when, by applying current control, frequency of the excitation current was adjusted to the value of mechanical resonant frequency of the vibratory system. In this case for maintaining the amplitude of oscillations, i.e. vibratory width, a sinusoidal half-wave of amplitude I_m = 0.4 A and length τ = 5 ms of EVA current, was required. In this process consumption of electrical energy was approximately $P_{in} \approx$ 5.5 W.

During the realization and testing of PFC bridge-less rectifier presented in this paper, as part of the experimental results were obtained characteristics of efficiency (%) as a function of the output power (W). Also, it was performed a comparison in terms of efficiency with the conventional boost PFC rectifier and as a result were obtained curves shown in Fig. 17.

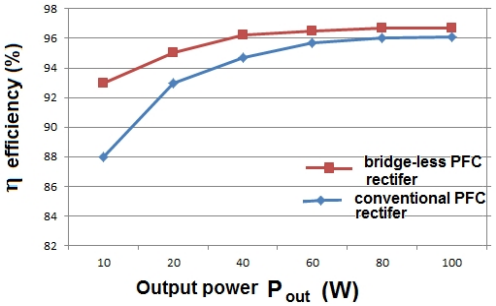


Fig. 17. The comparison of efficiency of applied bridge-less boost PFC rectifier with a conventional boost PFC rectifier.

From these results it is quite clear why the resonant regime the most suitable from the energy point of view. The consumption in the resonant regime in this case has been reduced by a factor of nearly four. The power saving effect is even higher if within a processing system operates a large number of such vibratory conveyors, or feeding units, the case most often met in practice.

We are in our research shown in the paper apply the bridge-less boost rectifier for PFC. This power converter is in the original idea described in the references [23]–[24], which were first published in the field. The paper [24] detailed study of bridge-less PFC rectifier from reference [23] in terms of reducing the switching losses using ZVS resonant circuit.

In the references to the published later, are studied various forms of bridge-less PFC topologies that could be applied to the regulated resonant VCD described in this paper. So in [26] give a comprehensive comparative review of bridge-less topology for power factor correction (PFC). The paper [27] treats the problems “one” cycle control technique of power factor correction (PFC). The references [28] gives an overview of bridge-less topology and detailed description of

the "buck" topology of Continuous Conduction Mode (CCM) bridge-less rectifier with high power factor. The input PFC rectifier can be realized with resonant topologies: LC, LLC and LCC.

The typical LLC resonant topology of AC / DC rectifier for PFC is shown in detail in reference [29]. The operation of parallel resonant power converter and the combination of series/parallel resonant power converter (LCC converter) in mode of high power factor are given in the reference [30].

A review of power converters of this class of resonant PFC rectifier is given also in references [31].

V. CONCLUSIONS

An optimum solution for the input rectifier of a VCD is proposed. On the basis of the simulation and experimental results, it has been shown that a transistor rectifier incorporating power factor correction represents an active filter whereby the undesired harmonics of the input current were eliminated and power factor correction of the VCD was accomplished. In addition, an analysis of the characteristic waveforms presented by the corresponding experimentally obtained oscillograms has been carried out. These results reconfirm the energy efficiency of resonant regimes owing to considerably reduced energy consumption.

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