Design of 4.48–5.89 GHz LC-VCO in 65 nm RF CMOS Technology

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***Abstract*—This paper describes a 4.48 GHz–5.89 GHz LC voltage-controlled oscillator (LC-VCO) as a key component in RF transceivers. The circuit is fully designed in TSMC's 65 nm radio-frequency complimentary metal-oxide-semiconductor technology process. The LC-VCO uses the structure of only one couple of NMOS differential negative resistances, tank circuit which consists of an optimal on-chip spiral inductor with switched capacitor and varactor arrays. The proposed design accomplishes wide tuning range frequency by using 6-bit switch capacitor array in addition to linearly varying MOS varactors. A switched current source block is used to improve the performance of the LC-VCO. The oscillator has a wide tuning range, between 4.48 GHz and 5.89 GHz. The LC-VCO dissipates 15.96 mW from a voltage supply of 1.8 V, whereas its phase noise is -124.1 dBc/Hz at 1 MHz offset of a at 5.89 GHz carrier.**

***Index Terms*—CMOS integrated circuits, nanoelectronics, radio transceivers, radiofrequency integrated circuits.**

I. INTRODUCTION

Over time, when wireless technology is improving so rapidly, more and more attention is appointed to high performance, low cost, low power, small area transceivers. Transceiver is the main part of the wireless system and its main function to receive and transmit data. Simplified diagram of transceiver shown in Fig. 1.

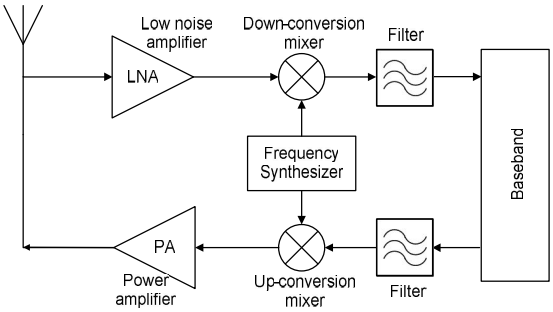

Fig. 1. Block diagram of wireless transceiver.

This transceiver consists of the following blocks: low noise amplifier (LNA), power amplifier (PA), down-conversion mixer, up-conversion mixer, filters and frequency synthesizer. In transceivers as the frequency synthesizer is mainly used the phase locked loop (PLL).

The classical PLL consists of five basic components: phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), voltage-controlled oscillator (VCO), and frequency divider (÷N), as shown in Fig. 2 below. The PFD detects the difference in frequency and phase between the F_{REF} and feedback F_{DIV} inputs and generates an UP or DN control signal based on whether the feedback frequency is lagging or leading the F_{REF} frequency. If the CP receives an UP signal, current is driven into the LPF filter. If the CP receives a DN signal, current is drawn from LPF. In next operation LPF converts these signals to a control voltage that is used to control the VCO. Thus, the principle of operation is as follows: if the PFD generates an UP signal, then the VCO frequency increases; a DN signal decreases the VCO frequency. The VCO stabilizes only when F_{REF} and F_{DIV} frequency and phase coincides. Under these conditions, the PLL is locked. Thus, the VCO is the key component that controls the frequency of the PLL.

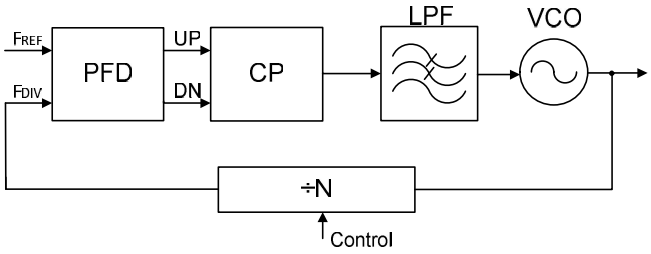

Fig. 2. Block diagram of classical PLL.

Commonly in high-frequency PLL are used two types of VCOs: ring oscillators (Ring-VCOs) and LC oscillators (LC-VCOs). The Ring-VCOs take a small area on a chip and can provide very wide tuning range but their phase noise performance is very poor when compared to LC-VCOs. LC-VCOs can operate in high frequency, but their tuning range is relatively small and on-chip inductors occupy a lot of chip area [1]–[5].

Transceivers IC design is moving toward the integration of a rapidly increasing number of frequency bands and communications standards, such as WLAN, WiMAX CDMA, WCDMA/HSPA, LTE and etc. To support a variety of wireless communication standards, multi-band and multi-standard wireless communication systems are being developed. The main objective of these systems is to support a wide frequency range from hundreds of MHz to tens of GHz [6], [7]. Such multi-band and multi-standard transceiver systems typically require several LC-VCOs to

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provide all carrier frequencies. IC designers are trying to create LC-VCO's with widest possible tuning range. This would reduce number of LC-VCO in transceiver, save area and the fabrication cost.

The paper is organized as follows: Section II describes the analysis of the proposed LC-VCO with the wide tuning range techniques; the layout and post-layout simulated results are introduced in Section III, and conclusions are summarized in Section IV.

II. CIRCUITS DESIGN

The schematic of the LC-VCO is shown in Fig. 3. The proposed LC-VCO consists of the following elements: high-quality inductor (L), varactors block, switched capacitors block, cross-coupled transistors (M1, M2) and current control block. The inductor with varactors and the switched capacitors block form a LC tank. The negative resistance of the LC-VCO is given by the transconductance of the cross coupled M1 and M2 NMOS transistors. They generate the negative resistance to cancel the loss in the LC tank so that the circuit can enable sustained oscillation.

Switched Capacitor Block. Frequency calibration is consisted by two steps of fine tuning and coarse tuning to widen the operating frequency range. The coarse tuning is obtained using the switched capacitor block. In this design, a 6-bit switched capacitor block is used. The block consists of 6 capacitors arrays connected in parallel, which can be turned on or off depending on the required capacity. All enbit[0…5] switches in the proposed LC-VCO is realized using NMOS transistors. Thus, the sixty-four curves of the sub-band cover the wide frequency range.

Varactor Block. The fine tuning is obtained using the varactors block in order to get precise operation frequency. This block consists of parallel connected multi-fingered NMOS varactors. These varactors maximize the tunability of the proposed LC-VCO. The external voltage V_{tune} is used for varying linearly the equivalent capacitance of NMOS varactors. V_{tune} control voltage range is from 1.5 V to 2.5 V.

Current Control Block. The last component of the proposed LC VCO is the current control block. In this block bias current is controlled by 4 bits. As can be seen in Fig. 3, ictrl[0…3] is a binary array of four independent control signals for four corresponding bias current switches. Therefore, by choosing ictrl[0...3] signals, the LC-VCO can get various bias current values, which means that LC-VCO can adjust its power consumption to the optimum. Compared with bandgaps reference current biasing this structure has the advantage of simplicity and power consumption selection flexibility.

III. SIMULATIONS RESULTS

The layout of the LC-VCO, designed in 65 nm RF CMOS technology process with Cadence Virtuoso environment, is shown in Fig. 4. The layout of the proposed LC-VCO is designed in accordance with the symmetry. It can not only reduce the effects of parasitic parameters but also improve the match between devices. In order to avoid as much as possible parasites, layout elements are oriented in minimum distances to each other and connected with the shortest as possible nets. The total layout area of the proposed LC-VCO is 385 μm × 325 μm. The largest part of the layout takes the inductor L, it's area about 274 μm × 325 μm (71,17 % of the total area). The one turn spiral, high-quality (Q = 26.5) inductor L is designed for 4.5 GHz frequency. Its value is small (373 pH) to allow the inclusion of more capacitance for a larger tuning range. This inductor is designed in top-metal layer (for higher quality factor) and has 4 terminals: 2 for signals, the third terminal is for guard-ring and the fourth terminal – for centre-tap connection.

The switched capacitors block is oriented in the centre of layout. In the middle of this block goes 6-bit control bus, which is connected to the vertical bus.

The varactors block is divided into two separate blocks, consisting of twelve parallel connected varactors. These varactors blocks are placed on the sides of the switched capacitors block. At the bottom of the switched capacitors block is the cross coupled M1 and M2 transistors. These transistors connected to the current control circuit from both sides.

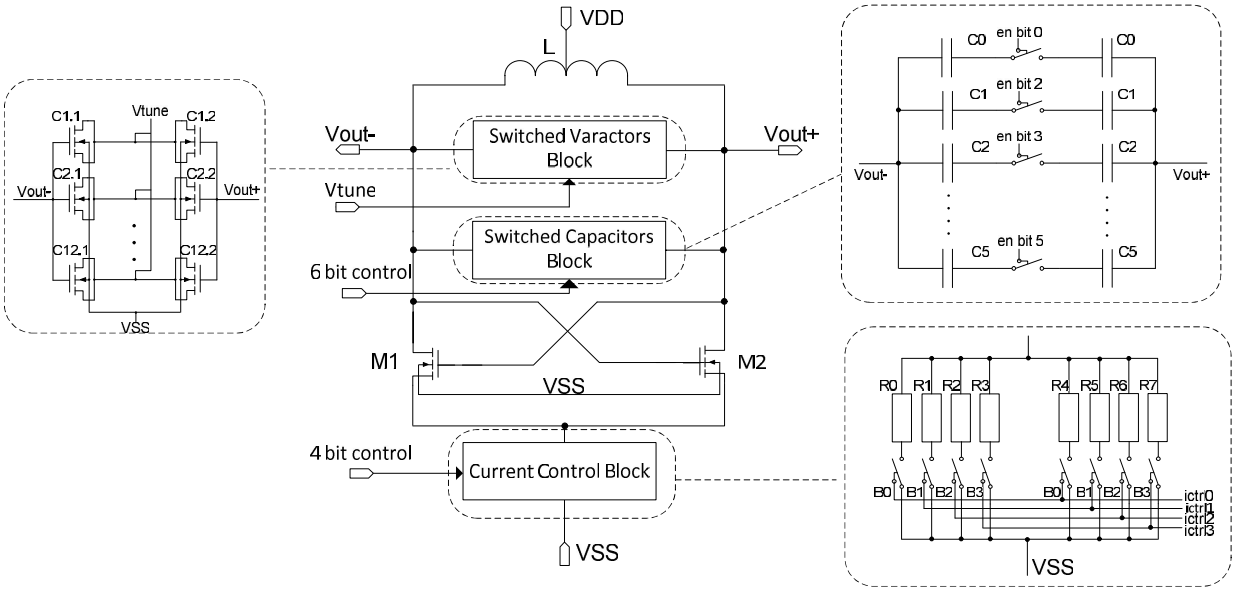


Fig. 3. Schematic of the proposed LC-VCO.

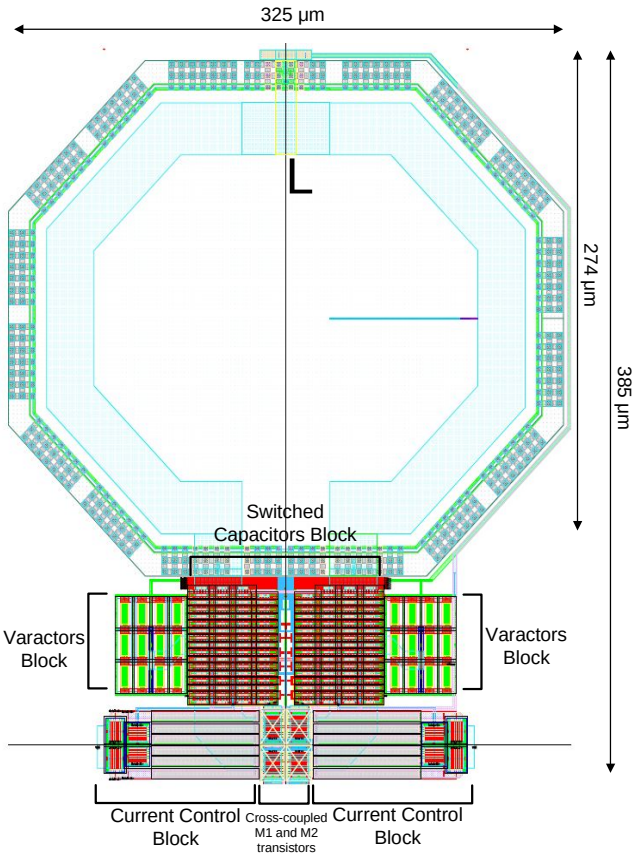


Fig. 4. Layout of the proposed LC-VCO.

The LC-VCO tuning range is illustrated in Fig. 5, showing all 64 overlapping frequency sub-bands. With a tuning voltage V_{tune} ranging from 1.5 V to 2.5 V, the upper sub-band LC-VCO achieves a tuning range from 5.57 GHz to 5.89 GHz and the lower sub-band LC-VCO achieves a tuning range from 4.48 GHz to 4.65 GHz.

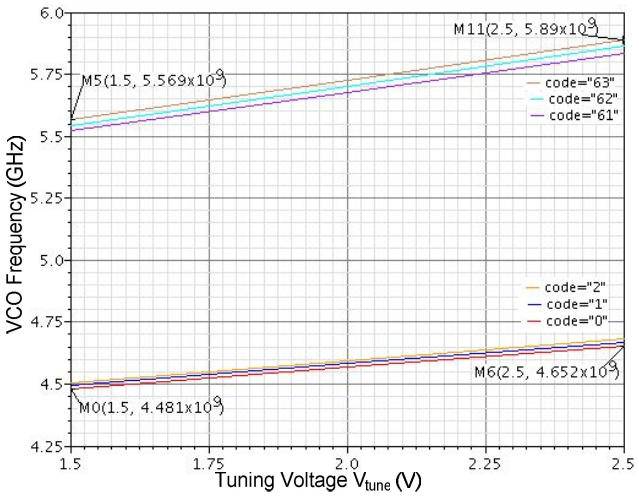


Fig. 5. Tuning range of the proposed LC-VCO.

The simulation results of phase noise, when changing the V_{tune} voltage and capacitor block code, are shown in Fig. 6. When V_{tune} = 2.5 V and the switched capacitor block code = 63, the phase noise is about -124.1 dBc/Hz at 1 MHz offset from carrier frequency f_{osc} of 5.89 GHz, -78.1 dBc/Hz, when the offset is 10 kHz, and -156.5 dBc/Hz, when the offset is 40 MHz.

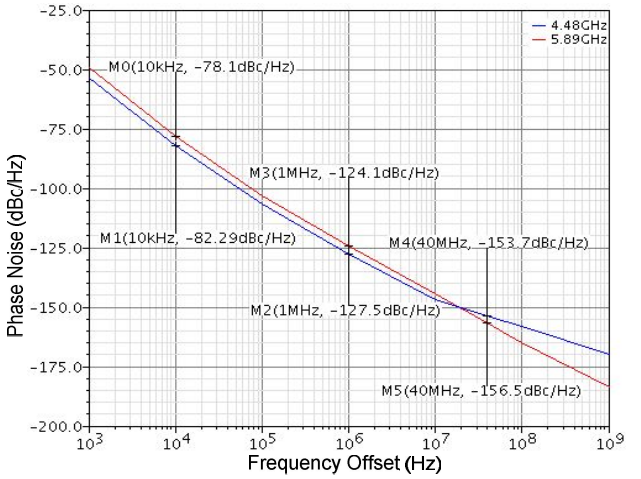


Fig. 6. Phase noise of the proposed LC-VCO, when V_{tune} = 1.5 V and the switched capacitor block code = 0, and when V_{tune} = 2.5 V and the switched capacitor block code = 63.

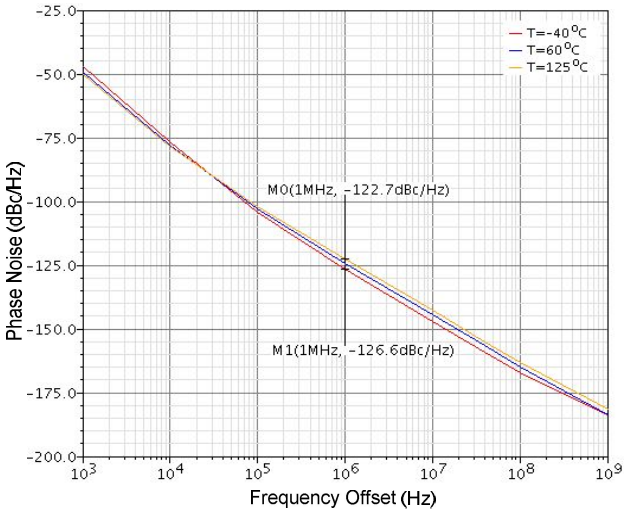


Fig. 7. Phase noise versus temperature, when V_{tune} = 2.5 V and code = 63.

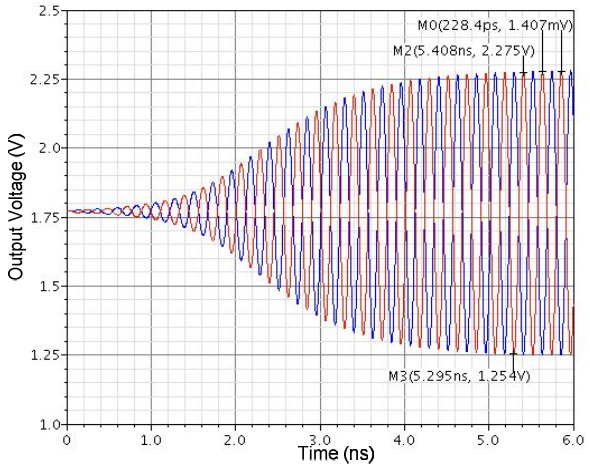
Thermal analysis simulated in the extended range from –(-45 ºC) to +120 ºC shows changes of phase noises (Fig. 7). Phase noise at the temperature -45 °C decreases to -125.6 dBc/Hz up to -122.7 dBc/Hz when temperature is equal +120 °C.

The figure of merit (FoM) of the LC-VCO can be approximately calculated from the power consumption and the phase noise in the oscillation frequency by

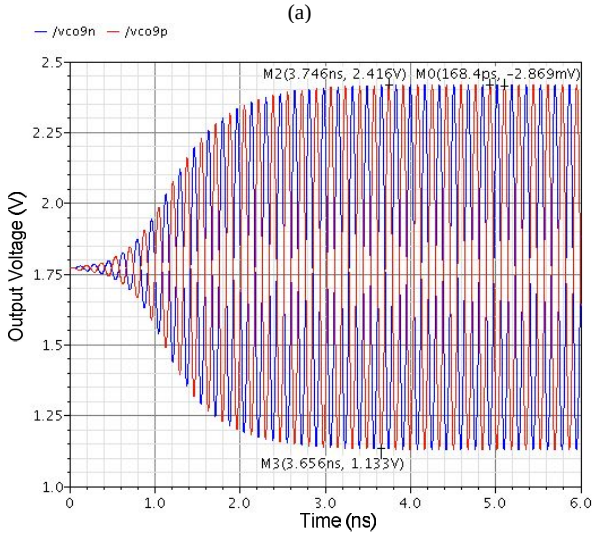
$$\mathrm{FoM} = L(\Delta f) - 20\log\left(\frac{f_{\mathrm{OSC}}}{\Delta f}\right) + 10\log\left(\frac{P_{\mathrm{diss}}}{\mathrm{mW}}\right), \quad (1)$$

where L is phase noise in Δf offset frequency, f_{osc} is the oscillation frequency, and P_{diss} is the power dissipation. The FoM of this proposed LC-VCO is about -187.5 dBc/Hz at 1 MHz offset from f_{osc} = 5.89 GHz.

Figure 8 shows the transient characteristics of the proposed LC-VCO at frequencies of 4.48 GHz and 5.89 GHz, when the tuning voltages V_{tune} at 1.5 V and 2.5 V respectively. As can be seen in Fig. 8, the output signals of the designed LC-VCO have 511 mV amplitude at 4.48 GHz, and 642 mV at 5.89 GHz.



(a)



(b)

Fig. 8. Transient response of the LC-VCO when: a. V_{tune} = 1.5 V and the switched capacitor block code = 0; b. V_{tune} = 2.5 V and the switched capacitor block code = 63.

Table I summarizes the performance of this LC-VCO and compares it with other previous reported LC-VCOs [8]–[17].

TABLE I. PERFORMANCE COMPARISON WITH OTHER VCO'S.

Ref.	**Tech.**	**V_{dd},** V	**f_{OSC},** GHz	**Tuning range,** %	**Phase Noise,** dBc/Hz @ 1MHz	**P_{diss},** mW	**FoM** dBc/ Hz
[8]	0.35µm	2.4	5.87	3.7	-112	19.2	-174
[9]	0.35µm	1.5	6.00	16.9	-98	18.0	-161
[10]	0.25µm	1.8	4.88	13.1	-125	22	-185
[11]	0.18µm	1.8	4.65	62.4	-95	12.0	-157
[12]	0.18µm	1.8	5.3	8	-122	13.5	-186
[13]	0.13µm	2.5	6.0	5.2	-115.2	12.5	-184
[14]	90nm	1.6	5.63	45	-108.5	14	-185
[15]	65nm	2.1	1.73	10	-120.7 at 400 kHz	28.8	-188
[16]	65nm	1.2	6.5	27.7	-118.3	20.2	–
[17]	65nm	0.65	5.49	28.6	-113.3	8.71	-179
This work	**65nm**	**1.8**	**5.89**	**27.2**	**-124.1**	**15.96**	**-188**

IV. CONCLUSIONS

A 4.48 GHz–5.89 GHz wideband and low phase noise LC-VCO is designed. The proposed LC-VCO design is accomplished with extensive tuning by using 6-bit switching capacitor array and linearly varying varactors. The circuit is implemented in 65 nm RF CMOS technology process. The functionality of the designed LC-VCO is evaluated by simulation in Cadence using foundry provided models. Post-layout simulation results show that: the tuning range is from 4.48 GHz to 5.89 GHz; phase noise is -124.1 dBc/Hz at 1 MHz offset from 5.89 GHz carrier; the figure of merit (FoM) is -187.5 dBc/Hz; power dissipation is only 15.96 mW at 5.89 GHz; the layout area of the proposed LC-VCO is 385 µm × 325 µm.

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