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Tunable Multiphase Oscillator Using Diamond Transistors with Voltage Controlled Condition of Oscillation for Amplitude Stabilization

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***Abstract*—The main aim of this paper is to present simple and low-cost solution of oscillator utilizing very simple method for automatic amplitude stabilization using adjustable current gain control. It provides satisfying total harmonic distortion results and adjusting of oscillation frequency over one decade. Experimental results confirmed workability and gave opportunity to consider and evaluate practically achievable performances of this oscillator type.**

***Index Terms*—Electronic control, automatic gain control circuit, amplitude stabilization, quadrature and multiphase oscillator, current amplifier, negative resistor.**

I. INTRODUCTION

A sinusoidal oscillator is very important part of communication systems and applications. There are many active elements suitable for construction of oscillators [1]. However, many hitherto published types are not studied in the point-of-view of output signals with low total harmonic distortion (THD) and stable amplitudes. There are many works where stabilization of output amplitudes was not discussed or explained and THD is really terrible [2]. There are some ways how to implement circuit for amplitude stabilization or electronic control of oscillation frequency. The easiest way is to use adjustable resistor (replaced by FET (Field-effect transistor) transistor [3], [4]). It is useful in cases of grounded passive elements in the oscillator circuit. Using of FET as a replacement of floating resistor(s) is quite complicated [4]. An opto-coupler should be a better choice if there are floating elements to be controlled as shown in [5]–[7]. Diode limiters are sufficient in some oscillator structures that are based on highly selective filtering band-pass structures (high quality factor) [8].

Utilization of parameters of active elements (transconductance, intrinsic resistance, gain) is also suitable for control of oscillation condition. Our contribution deals with very simple utilization of current gain of current-mode multiplier in oscillator design which is driven by output voltage. It ensures low THD and quite stable output levels in quite wide range of oscillation frequency adjusting.

II. OSCILLATOR STRUCTURE

Proposed oscillator uses integrators in the loop complemented by negative resistance which was realized by current-mode multiplier. Similar principle was used with transconductors (OTA) only, in [9], [10], for example. However, solution from [9], [10] is only quadrature (inverting output is not available), uses different (non-inertial) AGC (automatic gain control) and principle of CO (condition of oscillation) control (control is performed by nonlinearity of positive resistor). Block diagram that explains our modification is shown in Fig. 1.

Current-mode multiplier connected as controllable current amplifier (CA) allows electronic control of current gain in order to adjust resistance to negative value [11]. This is the most important part of the AGC circuit. Principle of operation is briefly given in Fig. 2. Symbol R_X represents intrinsic resistance of current input of current amplifier. In our case, the current gain B is given by DC control voltage V_G (for EL2082 type of multiplier was used, $B \approx V_G$ [11]). Input resistance is given by following equation

$$R_4^* = \frac{R_4}{1-B}, \tag{1}$$

which leads to

$$R_4^{*/} = \frac{R_4 + R_X}{1-B} \cong \frac{R_4 + 95}{1-V_G}, \tag{2}$$

in case when real behavior is considered ($R_X \approx 95\ \Omega$ in case of EL2082 [11]). Value of R_4^* is negative for $V_G > 2$.

Overall circuit diagram of proposed oscillator is shown in Fig. 3. It also contains values of parameters (passive elements) and detailed principle of AGC circuit employing

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one bipolar transistor which produces DC voltage for control of current gain B (negative resistance value). Increase of output level causes higher base-emitter voltage of BJT (bipolar-junction transistor) and therefore decrease of collector voltage and B of CA (R_4* value increases). Decreasing output level of the oscillator causes opposite reaction of this inertial AGC loop. This method uses nonlinear dependence of collector voltage on base-emitter voltage of BJT.

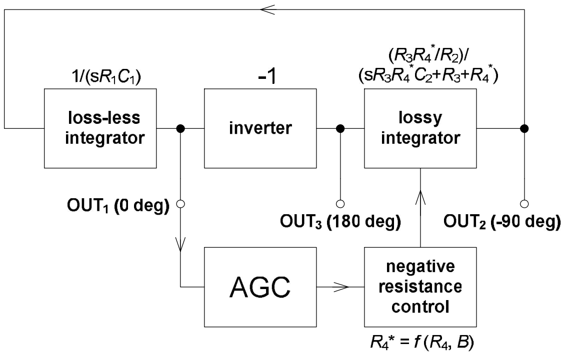


Fig. 1. Block diagram of proposed oscillator structure.

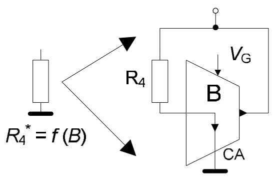


Fig. 2. Structure of grounded negative resistance made from current amplifier.

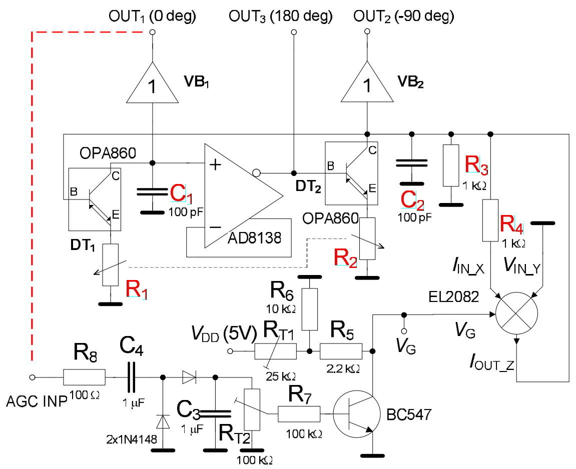


Fig. 3. Complete circuit diagram of the oscillator.

Two integrators are constructed from two diamond transistors [12] and time constants are controllable (simultaneously) by two grounded resistances, R_1 and R_2, in accordance to block diagram from Fig. 1. Very simple oscillators using DT-s (diamond transistors) were investigated in [13] but qualitative tunable features (low THD and unchangeable output levels) were not the main aim of contribution. All voltages in high-impedance nodes (at C_1, C_2) are available through voltage buffers (part of OPA860 package [14]) and therefore are available at low-impedance outputs without any further circuit complexity. Inverting voltage buffer (created by AD8138 [15]) is connected between integrators and provides also availability of low-impedance output of signal with 180 degree phase shift. Routine analysis of characteristic equation provides the following results

$$s^2+\frac{C_1\left(R_3+R_4^*\right)}{C_2R_3R_4^*}s+\frac{1}{R_1R_2C_1C_2}=0, \tag{3}$$

where R_4^* can be replaced by (1) in ideal case

$$s^2+\frac{C_1\left(R_3+\dfrac{R_4}{1-B}\right)}{C_2R_3\dfrac{R_4}{1-B}}s+\frac{1}{R_1R_2C_1C_2}=0. \tag{4}$$

Final form of characteristic equation is

$$s^2+\frac{C_1\left[R_3\left(1-B_3\right)+R_4\right]}{C_2R_3R_4}s+\frac{1}{R_1R_2C_1C_2}=0, \tag{5}$$

where we can find oscillation condition and oscillation frequency very easily as:

$$1+\frac{R_4}{R_3}=B, \tag{6}$$

$$\mu_0=\sqrt{\frac{1}{R_1R_2C_1C_2}}. \tag{7}$$

Relations between generated voltages achieve -90 and 180 degrees as we can determine from:

$$V_{OUT1}=-j\sqrt{\frac{R_2C_2}{R_1C_1}}V_{OUT2}, \tag{8}$$

$$\frac{V_{OUT1}}{V_{OUT2}}=-\sqrt{\frac{R_2C_2}{R_1C_1}}e^{arctg(0)j}=\sqrt{\frac{R_2C_2}{R_1C_1}}e^{-\frac{\text{®}}{2}j} \tag{9}$$

and from

$$V_{OUT1}=-V_{OUT3}=e^{-\text{®}j}V_{OUT3}. \tag{10}$$

Relative sensitivities of oscillation frequency (μ_0, f_0) on all influencing parameters are −0.5, as obvious from (7). Simultaneous control of R_1 and R_2 (for example by digital potentiometers) allows linear control of f_0.

III. EXPERIMENTAL VERIFICATION

We utilized commercially available active elements for experimental laboratory tests of designed oscillator. It allows fast, appropriate, efficient and low-cost analysis of real behavior.

A. Discussion of Main Parasitic Influences

The most important (for f_0 accuracy) are $R_E \approx 13\ \Omega$ [14] (intrinsic resistance of emitter port of the DT), output (collector) resistance of DT (it is the lowest value in high impedance nodes $R_{C1,2} \approx 54\ \mathrm{k\Omega}$) and capacitances in high impedance nodes as total sum of collector capacitance

(DT_2), base capacitance (DT_1) and output capacitance of current-mode multiplier [11] ($C_{B1} = C_{C2} \approx 2$ pF; $C_{inp\_buffer2} \approx 2$ pF; $C_{Z\_multiplier} \approx 5$ pF) in node C_2 and total sum of collector capacitance (DT_1) and inverter input capacitance [15] ($C_{C1} \approx 2$ pF; $C_{inp\_buffer1} \approx 2$ pF; $C_{inp\_inverter} \approx 1$ pF) in node C_1.

B. Design of Oscillator

Design parameters are: $R_1 = R_2 = R \in <119;\ 9783>\ \Omega$ (parasitic values of R_E of DT are taken into account [14]), $C_1 = C_2 = C = 470$ pF, $R_3 = R_4 = 1$ kΩ. Range of R value adjusting was calculated from (7). Adjustable trimmers allow careful setting of oscillation condition.

C. Measured Results

Comparison of measured and ideal dependence of oscillation on simultaneous change of both $R_1 = R_2 = R$ is shown in Fig. 4. Dependences of achieved output levels on frequency are in Fig. 5.

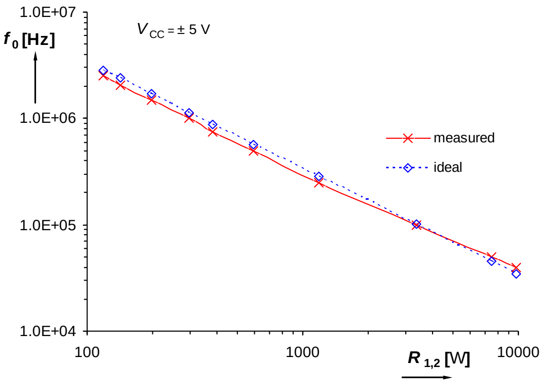


Fig. 4. Dependence of oscillation frequency on resistance value of tandem potentiometer.

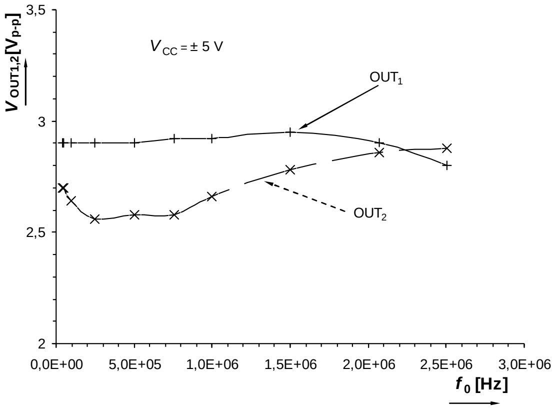


Fig. 5. Output levels vs. oscillation frequency.

Figure 6 shows progression of total harmonic distortion (THD), which is sufficiently low (around 0.5 %) almost in whole range of f_0 adjusting. Because OUT_3 is only inversion of OUT_1 analyses for OUT_1 and OUT_2 are sufficient (output levels and parameters are the same). We achieved ideal range of an f_0 adjusting from 35 kHz to 2.859 MHz. Measured results showed range from 40 kHz to 2.510 MHz. Equation (6) allows calculation of sufficient B for start of oscillations. In our case it is $B = 2$. Response of automatic gain control circuit (controlling voltage V_G respectively) on oscillation frequency and changes of oscillation condition in the loop (Barkhausen criterion [16]) are shown in Fig. 7.

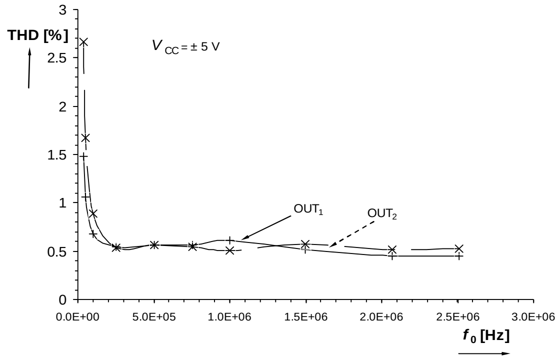


Fig. 6. THD vs. oscillation frequency.

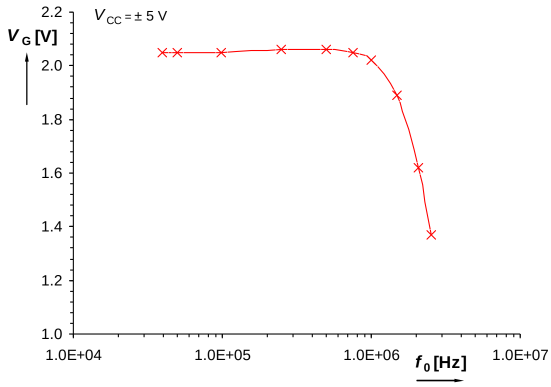


Fig. 7. Response of AGC (V_G control of current-mode multiplier) on tuning performance.

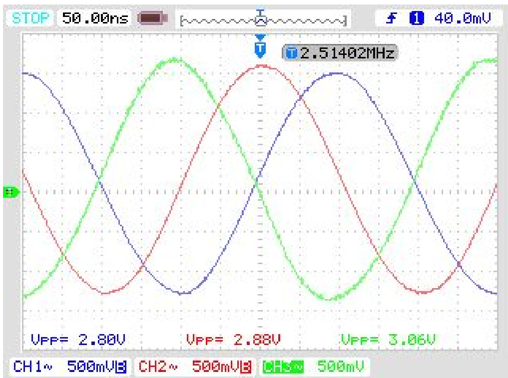
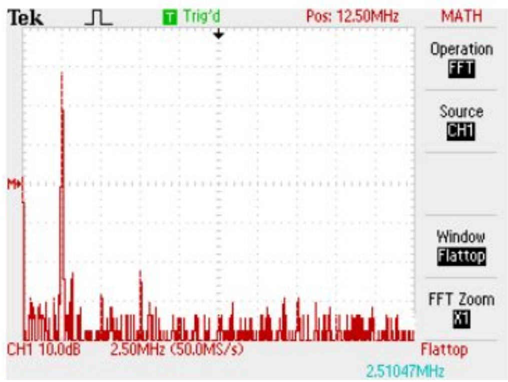
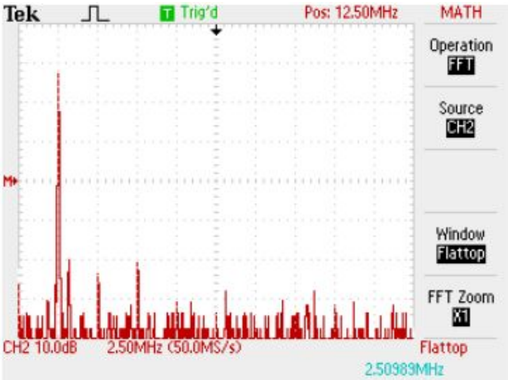


Fig. 8. Transient responses (CH_1 - OUT_1, CH_2 = OUT_2, CH_3 = OUT_3) for $R = 119\ \Omega$ and $V_G = 1.55$ V ($f_0 = 2.514$ MHz).



(a)



(b)

Fig. 9. Examples of FFT spectrum of a) OUT_1 and b) OUT_2; for R = 119 Ω and V_G = 1.55 V (f_0 = 2.514 MHz).

Higher f_0 frequencies mean higher gain in the open-loop circuit and therefore AGC causes decreasing of sufficient B to the lower values.

Transient response of available output signals and FFT spectrum in both high-impedance nodes (C_1, C_2 - after buffering) are shown in Fig. 8 and Fig. 9. Suppression of higher harmonic components is higher than 48 dBc.

IV. CONCLUSIONS

In this contribution, adjustable oscillator was presented. Oscillation condition is controlled by simple AGC employing current gain control and using nonlinearities of bipolar transistor and simple diode doubler for detection of control magnitude from output voltage. In combination with suitable oscillator structure, this approach allows to achieve wideband and linear oscillation frequency control. In our case, we achieved range of adjusting 1:60. Adjusting in range where THD is low (around 0.5%) achieves 1:25 approximately.

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