

# Six-Phase Voltage Forming Method Using the Largest Magnitude Space Vectors

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**Abstract**—In this paper, a six-phase voltage source inverter with a single-neutral star connected load is investigated. A space vector PWM (SVPWM), which uses largest magnitude vectors is proposed and implemented. Simulation results of the six-phase voltage source inverter (VSI), which uses the proposed SVPWM method, are compared to the results when a standard sinusoidal PWM scheme is used. Analysis of the results shows that proposed SVPWM scheme is suitable to form a six-phase sinusoidal output voltage. The main advantage of proposed SVPWM scheme is that it requires the same computational resources as the three-phase SVPWM.

**Index Terms**—Multi-phase circuit systems, multiple d-q planes, space vector modulation, voltage source inverters.

## I. INTRODUCTION

Multi-phase systems have many advantages over three-phase counterparts such as decreased torque pulsations, lower phase currents and improved reliability. Because of these advantages, multi-phase (more than three phases) machines are commonly used in electric cars, locomotives, ships, and aircraft [1]–[4]. Recent advances in power electronics made multi-phase AC induction motors even more attractive to use.

Since there are no multiphase electricity grids in the world, a multi-phase inverter is required to feed a multi-phase AC motor. Multi-phase inverters take a standard one phase or three phase mains, rectify it, and form a new output voltage for required number of phases by using pulse width modulation (PWM) technique to modulate the rectified voltage. If inverter's load is a motor with sinusoidal distribution of windings, VSI needs an appropriate PWM switching scheme, for the output voltage waveforms, which have to be as close as possible to sinusoidal [5].

Over the years, since the first multi-phase five-phase system was considered in 1969 [6], a lot of work has been done to investigate multiphase systems. Many PWM schemes for voltage source inverters have been proposed. Commonly used PWM techniques can be divided into two categories: continuous carrier-based PWM schemes, and space vector PWM schemes. Continuous carrier based PWM schemes can be further subdivided into sinusoidal

PWM (SPWM), sinusoidal PWM with harmonic injection and sinusoidal PWM with triangular harmonic injection [7]. Space vector PWM schemes can be grouped by the number of vectors they use to form an output voltage [8]. Both of these PWM schemes were adopted to form 5, 7, 9, 11... and basically unlimited, odd number of phases, in various load configurations [9]–[11]. However, by increasing the number of phases, DC bus utilization improvement (compared to standard SPWM), when using these advanced PWM schemes, decreases [12].

This paper focuses on six-phase voltage source inverter (VSI) with a star connected load which has one isolated neutral point. An appropriate PWM scheme is proposed to generate a sinusoidal output voltage. Theory is tested using a mathematical model of the VSI and its load in Simulink environment. Simulation results are compared to a basic sinusoidal PWM scheme.

## II. ANALYSIS OF A SIX-PHASE STAR CONNECTED LOAD

Let's consider a six-phase VSI with a load, which has a single neutral point (Fig. 1). Inverter switching function for each phase is defined as  $m_i = 1$  (where  $i = a, b, c, d, e, f$ ) when inverter's upper leg is on, lower leg is off, and  $m_i = 0$  when inverter legs are in off and on positions respectively. The instantaneous value of a phase to neutral voltage can be calculated using following expression

$$v_i = V_{dc} \left[ m_i - 1/6(m_a + m_b + m_c + m_d + m_e + m_f) \right]. \quad (1)$$

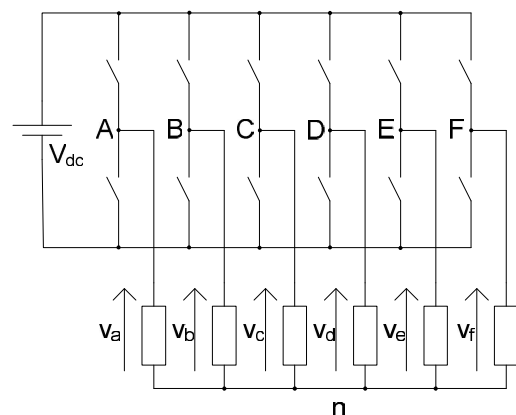


Fig. 1. Topology of the six-phase voltage source inverter with a symmetrical, single isolated neutral load.

Manuscript received February 13, 2013; accepted June 10, 2013.

This work was supported by the Agency for Science, Innovation and Technology (MITA) under High technology development programme project 31V-37.



This method was implemented and tested in Simulink to see whether the voltage could be formed by using only 6 vectors.

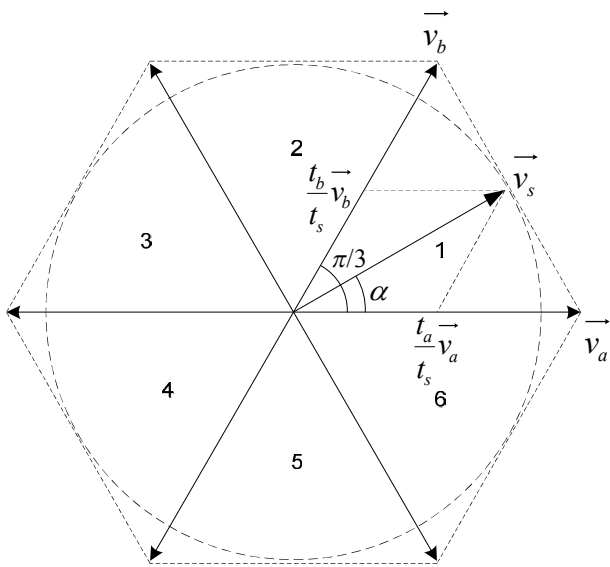


Fig. 3. Vector diagram of six-phase VSI with a single neutral star connected load, created using large space vectors.

Since only the large vectors are used to generate the output voltage vector, the diagram of 6 phases VSI takes a hexagonal shape (Fig. 3), and is divided into 6 sectors accordingly. The maximum value of the output voltage vector corresponds to the biggest circle, which can be inscribed into hexagon. Using the magnitude of the largest vector, which was calculated earlier, and knowing that circle touches hexagon's border at  $\alpha = \cos(\pi/6)$  it is possible to calculate the maximum peak output voltage of the inverter

$$V_{\max} = 0,667V_{dc} \cos(\pi/6) = 0,577V_{dc}. \quad (3)$$

In even-phase inverters, the maximum value of the output voltage peak amplitude cannot exceed  $0,5 V_{dc}$  when sinusoidal phase voltages are desired. When phase number is even, there is always two opposite phases, which share the  $V_{dc}$  voltage, so when both sinusoidal waveforms are at their minimum/maximum peaks but opposite phases, the voltage between them cannot exceed  $V_{dc}$ , therefore their amplitudes cannot exceed  $0,5 V_{dc}$ .

The calculated theoretical maximum output voltage higher than  $0,5 V_{dc}$  estimates, that using this scheme, the inverter will be operating in non-linear mode and the output waveforms will contain harmonics.

The main voltage output vector is formed from two neighbouring large vectors of the sector (Fig. 3). Vector duty cycle durations were calculated as follows:

$$t_a = \frac{|\vec{v}_s| \sin(k\pi/3 - \alpha)}{|\vec{v}_a| \sin(\pi/3)} T_s, \quad (4)$$

$$t_b = \frac{|\vec{v}_s| \sin(\alpha - (k-1)\pi/3)}{|\vec{v}_b| \sin(\pi/3)} T_s, \quad (5)$$

$$t_0 = T_s - t_a - t_b. \quad (6)$$

where  $k$  is the sector number,  $\alpha$  – absolute angle of the

output voltage vector,  $T_s$  – switching period,  $t_0$  – null vector duty cycle duration.

The null period is equally shared between two null vectors 000000 and 111111. Vector duty cycle durations in other sectors are calculated analogously. Switching table used in this implementation is shown in Table I. Fundamental frequency of output voltage is  $f = 50$  Hz, switching frequency  $f_s = 2$  kHz. Inverter's output was modelled using a 400 V DC source, connected to  $6 \times 2 = 12$  output FETs.

TABLE I. SWITCHING TABLE WHEN THE LARGEST MAGNITUDE VECTORS ARE USED.

Sector	$t_0/2$	$t_a$	$t_b$	$t_0/2$
1	000000	110001	111000	111111
2	000000	111000	011100	111111
3	000000	011100	001110	111111
4	000000	001110	000111	111111
5	000000	000111	100011	111111
6	000000	100011	110001	111111

The simulation was performed using a star connected inductive load with one neutral point (Fig. 1), line to neutral voltage was measured in phase A, and also the harmonic content of phase A voltage was monitored.

To compare the results, a basic sinusoidal PWM scheme was implemented for a six-phase VSI. Six fundamental sinusoidal waveforms with a phase difference of  $\pi/3$  between each two "neighbouring" waveforms were generated. Inverter output stage signals were obtained by comparing each fundamental waveform with a triangle function. The output stage was connected to the same star connected load. DC voltage source, output voltage fundamental frequency and switching frequency were the same as used in SVPWM simulation.

#### IV. SIMULATION RESULTS

The resulting voltage waveforms were filtered using 2<sup>nd</sup> order low pass filter with a cut-off frequency of 200 Hz. Waveform and spectrum of implemented SVPWM are shown in Fig. 4(a) and Fig. 4(b). The waveform peaks at 204 V volts, which is equal to  $0,51 V_{dc}$ . The DC bus utilization is lower than theoretically calculated. Also it is clearly seen that the waveform is not pure sinusoid of fundamental frequency, and has some harmonic content.

Analysis of the output voltage spectrum in Fig. 4(b) confirms that there is a third order harmonic present in the output voltage. Harmonics are common in odd phase number VSI when only largest magnitude vectors are used to form the output, however then it is clearly seen that harmonics appear from other than  $d_1$ - $q_1$  planes, since corresponding vectors in those planes are not being compensated, and also form a non-zero output vector. In this case, it is possible that the third harmonic is appearing either from the zero sequence components which were not taken into account, or the number of sectors is too low, and further investigation is required.

The harmonics around 2 kHz switching frequency are from the switching noises, and could not be avoided by any PWM scheme.

Sinusoidal PWM output waveform is shown in Fig. 4(a). Its amplitude is 196 V ( $0,49 V_{dc}$ ), which is almost theoretical limit ( $0,5 V_{dc}$ ) for a six-phase inverter. The

waveform is pure sinusoid, and only switching harmonics, which are unavoidable, exists in the output.

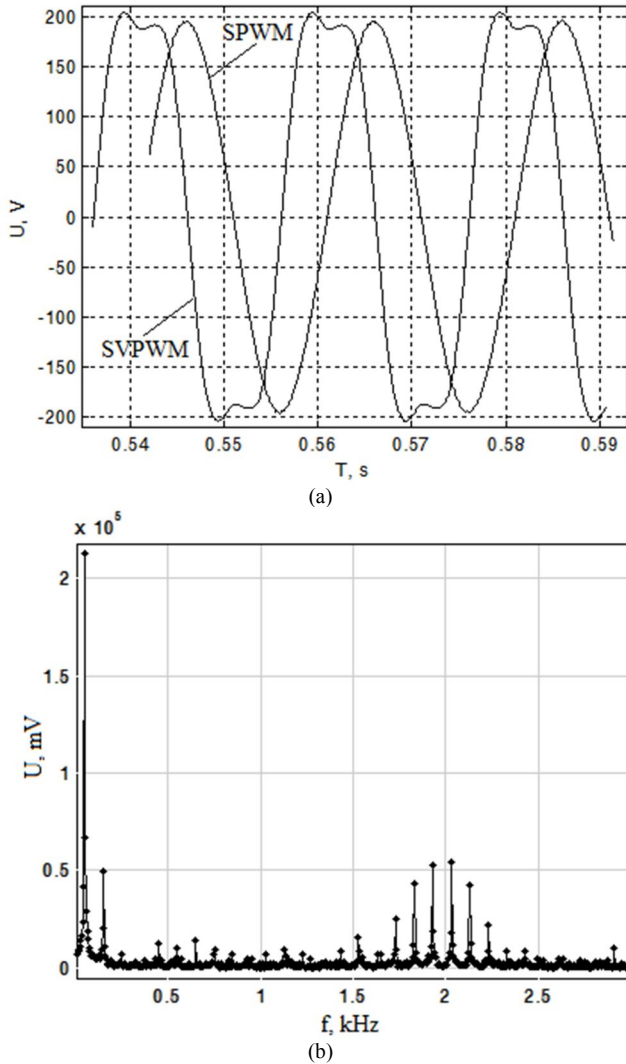


Fig. 4. Simulation results of a 6 phase VSI with a star connected load: (a) filtered phase A voltage, (b) SVPWM phase A voltage spectrum.

This type of PWM is suitable for driving 6 phase AC motors; however it could be difficult to implement in microcontroller applications, since this scheme is demanding on CPU power and memory.

## V. CONCLUSIONS

The proposed SVPWM scheme can be used to form a six-phase near sinusoidal voltage output. Its main advantage is that it requires almost the same microcontroller resources as three-phase space vector PWM scheme. The drawback of proposed SVPWM scheme is that it contains third harmonic in the output waveform.

The proposed SVPWM scheme could be further improved

by using asymmetrical SVPWM, which would use not only large space vectors. Using more vectors should allow eliminating the 3<sup>rd</sup> harmonic.

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