Analysis of Deep Level Centers in GaAs *pin*-Diode Structures

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***Abstract*—This paper presents an analysis of the DLTS (Deep Level Transient Spectroscopy) spectra of GaAs p^+-*pin*-n^+ diodes. It is shown that the background spectrum of the deep levels is reproducible and depends on the liquid-phase epitaxy mode (LPE). The temperature dependence of the capacitance-voltage characteristics showed that the *i* layer is formed by compensation involving deep levels. The space charge covers the width of the *i* layer and spreads into the depletion *p* and *n* regions of the diode structures.**

***Index Terms*—Gallium Arsenide, *pin*-diodes, capacity relaxation method, deep levels.**

I. INTRODUCTION

The development of the current global semiconductor wafer market shows clear renewed interest in semiconductor devices based on gallium arsenide. Evidence of this is the expert forecast for the market growth of GaAs wafer consumption held by Yole Développement group (Fig. 1).

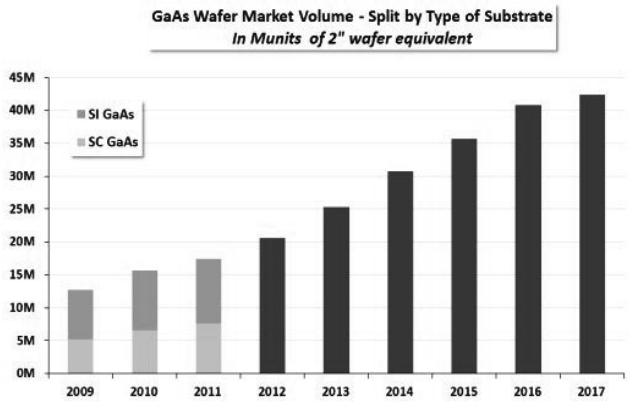


Fig. 1. GaAs wafer of 2″ equivalent market volume [1].

After the large recovery growth from 2009, GaAs substrate market has slowed sharply in 2011 due to weak demand in RF circuits and in optoelectronics.

From a growth rate of +22 % achieved in 2010, the GaAs substrate market has only increased by +4 % in 2011.

However, the market was recovered in 2012 due to the sheer volume of the handset market.

Manuscript received March 11, 2013; accepted August 23, 2013.

This research was supported by the European Union through the European Regional Development Fund, Nations Support Program for the ICT in Higher Education "Tiger University", the Estonian Ministry of Education and Research (target oriented project SF0142737s06), the Estonian Science Foundation (research grant G8592).

Hence, GaAs substrate market should reach the good results fuelled primarily by:

– Increasing GaAs content in handsets;

– Increasing in RF electronics (power amplifiers, switches…) represented the main market for GaAs wafer and will continue to feed the business for the next years with the development of sophisticated smartphones, the development of 3G/4G networks and the increased demand for data communication [1].

As seen from the diagram, in the next 5 years (2012–2017) output is expected to more than double. The another likely reason for such recovery is to serve the unfulfilled expectations in volume growth of electronic converters based on wide band gap semiconductor materials such as SiC, GaN, AlN. In this regard, the study of semiconductor devices based on gallium arsenide becomes extremely relevant once again. This work is devoted to the study of gallium arsenide *pin*-diode structures.

It is well-known that *pin*-diodes occupy a confident and ever-increasing position in RF and microwave devices. Reverse recovery time, and, therefore, the lifetime of minority carriers in such devices is a key factor in determining the frequency characteristics of the device. The lifetime in turn, depends on the processes of emission and capture of carriers at deep levels in the band gap of the semiconductor. The study of the background spectrum of the deep levels, centered in the base areas of *pin* structures, is the goal of the present work.

II. MATERIALS AND METHODOLOGY

The investigated structures were prepared as follows. The p^+-*pin*-n^+ structures were grown on p^+ GaAs substrates doped up to Na = 10^{18} cm^{-3} by liquid-phase epitaxy (LPE) [2]. The donor concentration in the n^+ layer was Nd = 10^{18} cm^{-3}. Ohmic contacts were deposited on the p^+- and n^+-surfaces: Ni+Ag and Au+Ge+Ag respectively. The structures were formed on wafers of the standard diameter, and then the wafers were separated into chips of 3 × 3 mm^2. We studied three groups of structures which differed in their manufacturing techniques: Group I, Group II and Group III. During the study, the current-voltage (I-V) and capacitance-voltage (C-V) characteristics, and their temperature dependence were measured. Spectra of deep levels were investigated by the capacity relaxation method (DLTS). For the measurements, the following equipment was used: Agilent B1500A Semiconductor Device Analyzer and Deep

Level Transient Spectroscope DLS-83D. In the course of the investigation we used the theoretical and methodological approaches that have been well developed in numerous publications, for example [3]–[5].

III. RESULTS AND DISCUSSION

Figure 2 shows the temperature DLTS spectra of the background deep levels for the samples from the three groups of structures.

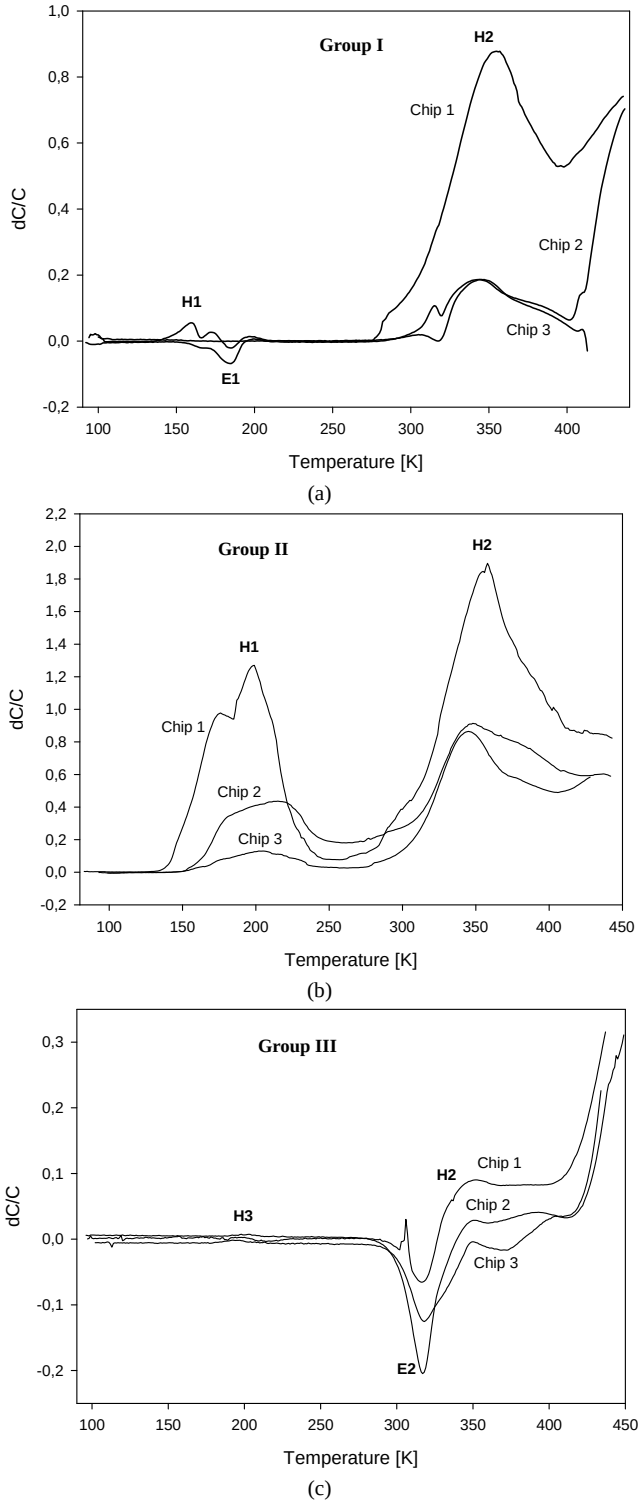


Fig. 2. Temperature spectrum of deep levels in p^+-*pin*-n^+ structures (reverse bias U_r = -10V, filling pulse U_1 = 1V, frequency f = 500Hz for (a) - Group I, (b) - Group II, (c) - Group III).

It should be noted that the comparative evaluation of the spectra were performed at a qualitative level. The Lang method, proposed in [5], can be applied uniquely for Schottky diodes or for structures with sharp *pn* junctions. In the pin structures submitted for investigations the applied external voltage is, in reality, focused on the *i* layer and weakly modulates the expansion of the space charge in the *p* and *n* layers by changes in the diffusion potential.

As a consequence, from the resulting DLTS spectra, it is impossible to calculate the depth of the energy levels, their concentration, and the captur cross section, and, therefore, to identify them.

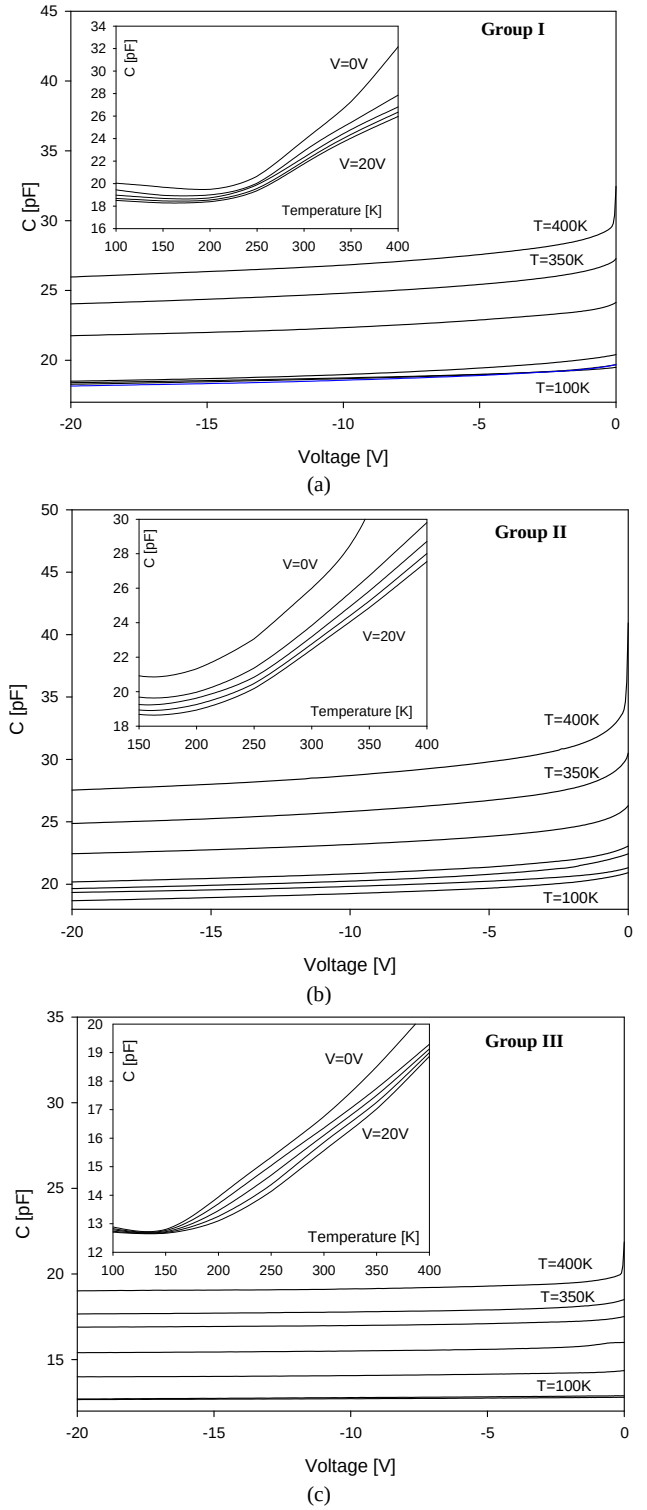
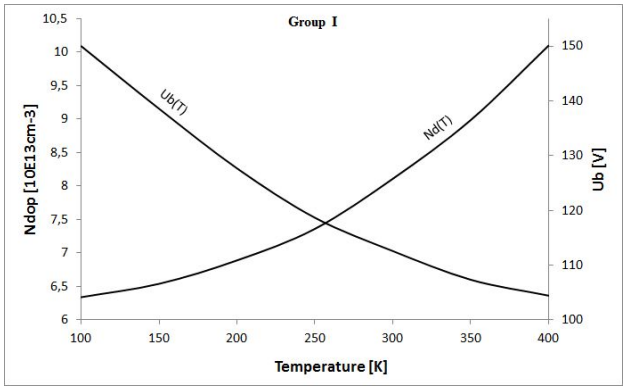


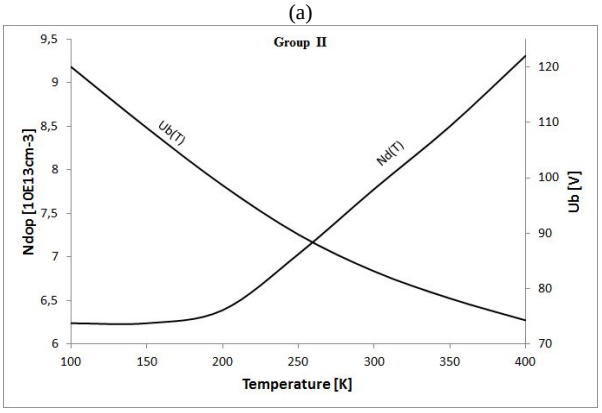
Fig. 3. The dependence of the capacitance-voltage characteristics and the stationary capacitance on the temperature (for (a) – Group I, (b) – Group II, (c) – Group III).

The presented spectra exhibit evidence of the presence of deep levels of the hole and electron type in all samples. Depending on the technology variants, the spectra of background defects have different configurations. However, within each group of samples the configuration of the spectra is identical. Ensembles of defects with similar energy parameters lead to distortion of the peaks as well as their splitting, which adds to the difficulty in identifying them. It is also essential that all three groups in the range of 350 K stable demonstrate the hole trap H2. In earlier studies, for example [6]–[11], in addition to background defects in the pin layers grown by LPE, typical hole traps A and B are present with activation energies E_v = +0.41 eV and E_v = +0.68 eV, respectively.

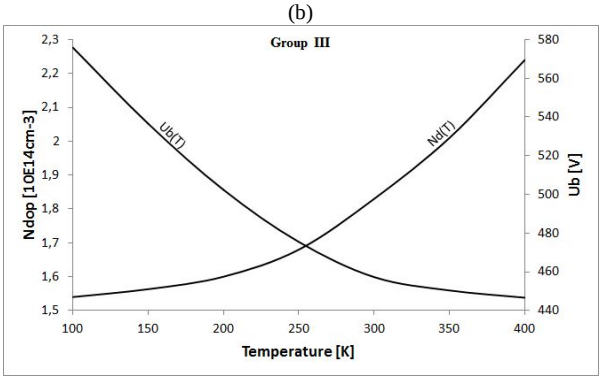
This knowledge allows us to correlate the peak of H_2 with B's center because the activation energy for this peak, determined from the p^+-pin-n^+ spectra, is +0.530 eV÷ +0.681 eV. Trap A with a more shallow level cannot be defined being "shadowed" by the background impurities.



(a)



(b)



(c)

Fig. 4. The temperature dependence of the concentration of ionized levels (N_{dop}) and built-in voltage (U_B) (for (a) - Group I, (b) - Group II, (c) - Group III).

The temperature changes of the C-V characteristics of the p^+-pin-n^+ structures showed strong dependence of the capacitance on the temperature (Fig. 3).

The concentration of ionized levels and built-in voltage defined from the C-V characteristics also depend on the temperature.

Using the method proposed in [4] we can pick out the total concentration of deep levels in the band gap. As seen from the DLTS spectra (Fig. 2), at temperatures above 400 K and below 100 K, deep levels are not fixed. This means that at T > 400 K the steady filling of deep levels has time to follow the filling pulse, but at T < 100 K the initial deep levels filling is stored. Hence, the difference $N_{dop(400K)} - N_{dop(100K)}$ will give us the total concentration of deep levels in the band gap (N_t). For the three groups of structures, the following concentrations of deep levels were obtained: Group I $N_t = 4.66 \times 10^{13}$ cm^{-3}, Group II $N_t = 3.07 \times 10^{13}$ cm^{-3}, Group III $N_t = 7.0 \times 10^{13}$ cm^{-3}.

It can be seen that the concentration of the deep levels in the structures is comparable with the concentration of shallow impurities (see Fig. 4) and, therefore, the deep levels play an active role in the compensation of the layers grown in the LPE. As a result, structures are characterized by a sufficiently wide *i* region. The *i* layer, measured by the electro optical method, for all the structures in the three groups is 30 ± 5 μm wide. As shown in Fig. 3, the structures of all three groups are characterized by strong dependence of the C-V characteristics on the temperature. With a set of formulas of the thermionic emission model binding capacitance, the width of the space charge, the built-in (diffusion) potential, and the total concentration of impurities:

$$C = \frac{\pounds\pounds_0}{w} A, \tag{1}$$

$$w = \sqrt{\frac{2\pounds\pounds_0 (U_B + U_R)}{qN_{dop}}}, \tag{2}$$

$$U_B = \ddot{}_b - (E_c - E_{Fn}), \tag{3}$$

where C is the barrier capacitance, $\mathcal{E}$ the dielectric permittivity, $\mathcal{E}_0$ the electric constant, A the area of the junction, w the width of the space charge, U_B the diffusion potential, U_R the reverse bias, q the elementary charge, N_{dop} the impurity concentration, φ_b the height barrier, E_c the bottom of the conduction band, E_{Fn} the quasi-Fermi level, we can carry out an analytical study of the experimental dependencies.

First, it should be noted that the width of the space charge calculated by (1) and (2) are almost identical in magnitude. This means that the junction active area of the structure is the same as the chip area, so the technological errors of the formation of the junction, and by the surface metallization can be avoided. The first conclusion to be drawn from these results is that the space charge region at zero bias, even at 400 K, completely overlaps the *i* layer, and spreads into the *p* and *n* depletion layers. This means that in the recharge process, two interfaces, the *p*-*i* and *i*-*n* regions, can be affected, which in turn does not allow a monosemantic

interpretation of the spectra in accordance with the Lang model. Ignoring the temperature dependence of the dielectric constant in (1), $C_{(400K)}/C_{(100K)}$ must be equal to $w_{(100K)}/w_{(400K)}$. In turn, the width of the space charge depends on the built-in voltage (thus the diffusion potential) as $w(U_B)$ α $U_B^{1/2}$. The ratio $w_{(100K)}/w_{(400K)}$ for different groups is 1.4:1.57, while $U_B^{1/2}{}_{(100K)}/ U_B^{1/2}{}_{(400K)}$ changes only as 1.1:1.27. Therefore, the main role in the temperature change of the capacitance is in changing the cumulative concentration of the impurities and defects, which in turn indicates evidence of an overcompensated layer in the base region of the structures. These considerations are also supported by the I-V temperature dependence. The resistance of the diode structure increases significantly at temperatures below 200 K. Permanent changes in the capacitance in all the temperature range suggests that the width of the overcompensated layer practically coincides with the width of the space charge region. A very weak change in the capacitance, at least in the range 1 V < U_R < 20 V, confirms the primary impact of deep levels and the evidence of a homogeneous spatial distribution of defects across the width of the space charge.

IV. CONCLUSIONS

The DLTS spectra obtained from the analyzed p^+-*pin*-n^+ structures demonstrate the presence of electron and hole type deep levels in all investigated samples. Within each group, the configuration of the spectra is identical. This indicates that the sources of defects are stable, reproducible and depend on the variations in technology for epitaxial growth. The width of the space charge calculated from the C-V characteristic exceeds the width of the *i* layer and spreads into the *p* and *n* depletion regions. The permanent change in the capacitance over all the temperature range and the very weak dependence of the capacitance on the reverse voltage indicate that the thickness of the overcompensated layer practically coincides with the thickness of the space charge, as well as indicating evidence of a homogeneous spatial distribution of defects across the width of the space charge.

The fact that, in the general spectra for all three groups, the steady presence of hole traps, such as the center of H2 (Fig. 2), can be identified is significant. This means that from the special studies on the "proper" test samples made from the p^+-*pin*-n^+ structures, for example, the Schottky diode, or a sharp *pn*-junction, the exact parameters of the key defects (centers A and B) can be set. Then, the correction factors for the peaks of interest in the general background spectra of p^+-*pin*-n^+ structures can be determined. This in turn will provide an opportunity for express DLTS control of the finished product and thus can be realized in on-line monitoring of the LPE process in order to optimize the dynamic characteristics of the devices.

In addition we hope that on the basis of more precise information about the structure of the deep levels, their concentration and capture cross sections we will have a more reliable source of data base to build a formal model of the existing pin structure. And this in turn means that during the design phase of diode structures with the required output parameters, we can use the methods of computer simulation, the use of which for the moment does not give good results because of uncertainty of situation in pin region of diodes.

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