Design of a Linear-in-dB Power Detector in 65nm CMOS Technology

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***Abstract*—In this work, design and simulation results of a linear-in-dB power detector are presented. The power detector can be used in integrated wireless communication devices for received or transmitted intermediate frequency (IF) signal power monitoring and control, local oscillator (LO) leakage detection. The whole detector block is composed of a mixer, amplifier and IF logarithmic amplifier to achieve linear-in-dB power detection. Design and simulation verification was performed using Cadence software package. The proposed integrated circuit in 65 nm CMOS technology achieves a 74 dB dynamic range, while consuming 24 mW from 1,2 V power supply.**

***Index Terms*—Dynamic range, intermediate frequency, logarithmic amplifier, power detector, radio frequency.**

I. INTRODUCTION

Optimal power consumption, in terms of speed and battery saving, is a priority in nearly all portable devices designed for wireless technologies. To achieve this, accurate tracking of the signal power is needed. A power detector is required to detect and measure the power of the signal that is being transmitted. The simplest power detector circuit is realized by using a Schottky diode, bipolar junction transistor or metal-oxide-semiconductor field effect transistor [1]–[3]. Use of the Schottky diode is limited by its large parasitic capacitance which reduces the maximum frequency range [1]. The bipolar transistor is not suitable for low cost solutions, because it requires the use of a more expensive BiCMOS technology. Parameter variation over temperature is another problem which affects all of the mentioned devices. A logarithmic amplifier is widely used in modern circuits as a power detector. It has a constant slope transfer curve corresponding to different input power (in decibels) and wide dynamic range [4], [5].

The transmission power of a mobile terminal can be optimized with a power control loop such as shown in Fig. 1. A transmit observation receiver can be incorporated on the transmitter chip to continuously observe and change the transmitted signals power and correct any modulator imperfections [6].

In this paper, we present a new architecture of a power detector that can be used as a transmit observation receiver to detect the modulated signal. The proposed architecture uses a mixer, driven by the same local oscillator (LO) used in the transmitter chain, to down convert the RF signal, thus eliminating the need for high-speed components in the power detector core. Furthermore, the detection range can be controlled via programmable gain amplifier (PGA).

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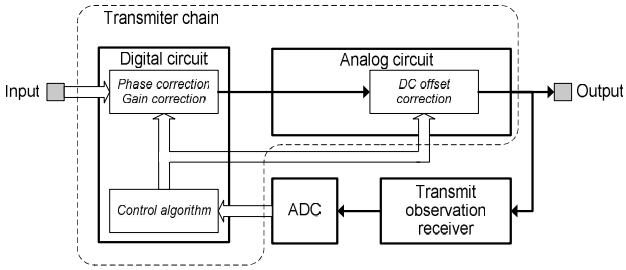

Fig. 1. Block diagram of a power and correction control loop.

II. LINEAR-IN-DB POWER DETECTOR ARCHITECTURE

The presented linear-in-dB power detector architecture is shown in Fig. 2. It consists of a decoupling element, mixer, amplifier, logarithmic amplifier and a RC circuit.

The first three stages imitate a traditional receiver chain, with the exception of a low noise amplifier (LNA). The signal from the transmitter output is demodulated via a direct-conversion mixer that is driven by the same LO as the transmitter mixer is. The demodulated intermediate frequency (IF) signal is amplified by an amplifier with controlled gain. The gain control enables to change the input dynamic range of the power detector.

A logarithmic amplifier is used for power detection. It outputs a current value based on the input signal. A simple RC circuit is used to convert the current into voltage and filter the ripple present at the output.

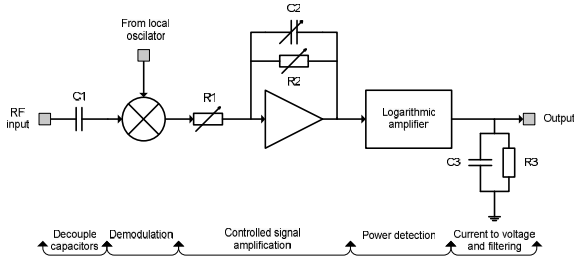

Fig. 2. Architecture of the proposed power detector.

Details of the logarithmic amplifier circuit design and its simulation results are presented in the following sections.

III. LOGARITHMIC AMPLIFIER

The logarithmic amplifier structure is shown in Fig. 3. It uses successive detection and approximates the logarithmic as a piece-wise linear function [1]. The logarithmic amplifier is composed of a cascade of limiting amplifiers, which outputs are connected to a separate rectifier. The rectifier outputs a current based on the input-output signal level of the limiting amplifier. The currents from the rectifier outputs are summed by the RC circuit shown in Fig. 2.

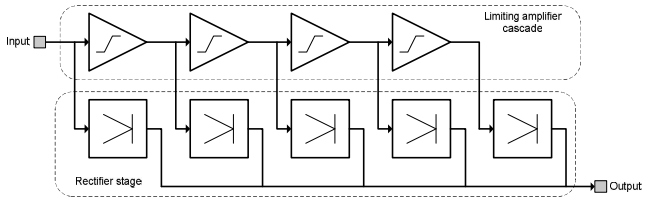

Fig. 3. Block diagram of the logarithmic amplifier.

Bandwidth, dynamic range and detection error are determined by the number N of limiting amplifier stages used in the power detector and the properties of each limiting amplifier stage. The number of rectifiers needed for the same power detector is equal to (N+1). If N identical limiting amplifier stages are used, the total bandwidth of the power detector can be written [1]

$$f_T = f_S \sqrt{2^{1/N} - 1}, \quad (1)$$

where f_T is the total bandwidth of the limiting amplifier cascade and f_S is the bandwidth of one limiting amplifier. Limiting amplifier cascade is often used in radio frequency (RF) power detection. For RF power is detection, limiting amplifier cascade must have large bandwidth. For GSM-1800 frequency band, each limiting amplifier bandwidth in a N = 4 cascade should be at least 4,3 GHz. Wireless communication technology standards are starting to use carriers near 5 GHz range. Wide power detection range with good accuracy can be obtained only by using limiting amplifiers with bandwidths above 10 GHz. So, realizing such wide band amplifiers can be a challenge, especially in low voltage CMOS technologies.

Most modern transmitters use direct-conversion mixers to modulate the carrier frequency with IF signal. Ideally, if the differential IF signal voltage is zero at the modulator input, the output differential signal voltage is also zero. Power can be calculated by measuring the amplitude of the transmitted signal when the output load is known. By detecting the IF signal amplitude, we can detect the output signal power. Also, this structure can be used for IF dc offset detection, which is the main cause of leakage at the transmitter output.

One problem of a high gain stage limiting amplifier is that the dc offset, which results from non-ideal matching of the transistors in the circuit, will be amplified through the cascade [7]. If the dc offset is high, it can saturate the output which will lead to an incorrect value at the output. To compensate this, different techniques can be used such as chopper modulation [1], ac coupling [5], [8] dc subtraction [1], [2] and the use of a comparator-DAC circuit for dc offset calibration.

A. Limiting amplifier

The limiting amplifier circuit is shown in Fig. 4. It is a one stage, fully differential amplifier with output common-mode voltage feedback loop. Transistor *N1* acts as a current mirror for the input (*N2* and *N3*) and common-mode feedback (*N5* and *N6*) differential pair current sources *N4* and *N7*. The current source and active load transistors (*P1-P4*) widths should be large, so that their saturation voltage V_{sat} could be minimized, thus extending the output voltage swing range. Transistors *N8-N10*, *P5-P7*, resistors *R1* and *R2* are used to detect output common-mode voltage. Negative feedback is used to maintain the desired output common-mode voltage equal to reference voltage U_{ref} (set to half the supply voltage to achieve highest output swing range). This ensures optimal biasing conditions for the next stages.

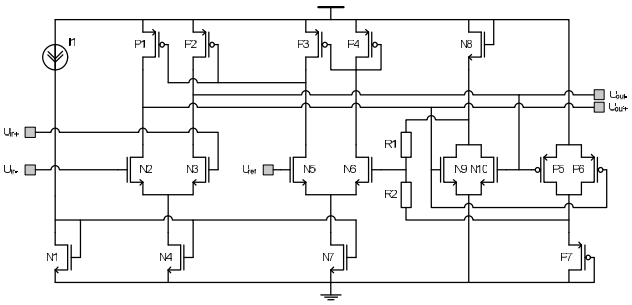

Fig. 4. Limiting amplifier circuit.

B. Full-wave rectifier

A full-wave rectifier circuit is shown in Fig. 5. It is used to detect an input signal and consists of two identical unbalanced source-coupled pairs (first pair, *N2* and *N6*; second pair, *N3* and *N7*) with different gate *width/length* ratios that are equal to *K*. The output current I_S is the summation of the current difference of the cross-coupled pairs and can be written

$$I_S = \left(I_{N2} + I_{N7}\right) - \left(I_{N3} + I_{N6}\right). \quad (2)$$

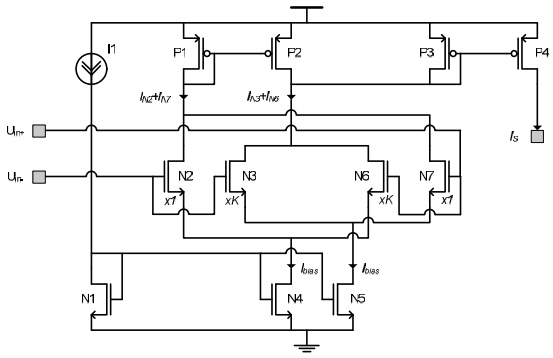

Fig. 5. Full-wave rectifier circuit.

It can be shown [8], [9], that when

$$\left|U_{IN+} - U_{IN-}\right| \le \sqrt{I_{bias} / K \cdot g_m}, \quad (3)$$

where g_m is the transconductance of the transistors, output current I_S changes as a parabolic function. When

$$\sqrt{I_{bias} / K \cdot g_m} \le \left|U_{IN+} - U_{IN-}\right| \le \sqrt{I_{bias} / g_m}, \quad (4)$$

output current I_S approximates a logarithmic function. Increasing the parameter K, reduces the input voltage range at which the output current has parabolic characteristics.

The bias current for *N1* transistor should be stabilized to minimise output current drift across temperatures. Because the output current is summed and converted to voltage via RC circuit, temperature dependency can cause voltage detection errors. Bandgap current reference source is used in the proposed power detector. Also, the current summing resistor *R3* in Fig. 2 is composed of two different type resistors with opposite temperature coefficients to maintain a constant resistance across a range of temperatures.

IV. Simulation Results

The designed linear-in-dB power detector was simulated using Cadence software. Power consumption from 1,2 V supply is less than 24 mW.

Figure 6 shows the small signal frequency response of one limiting amplifier and the entire limiting amplifier cascade. Frequencies f_S and f_T are equal to 133,4 MHz and 57,2 MHz, respectively.

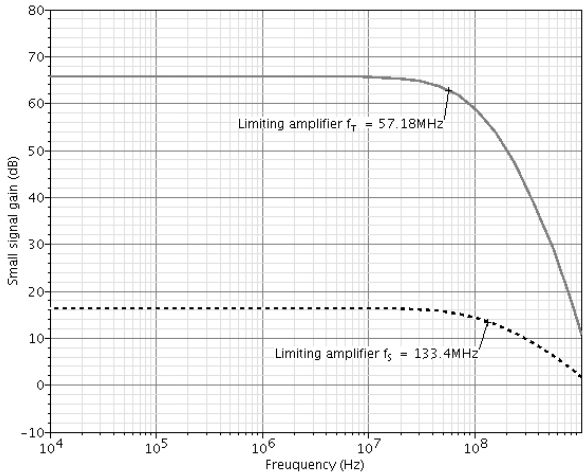

Fig. 6. Frequency response of a single limiting amplifier stage and the whole cascade.

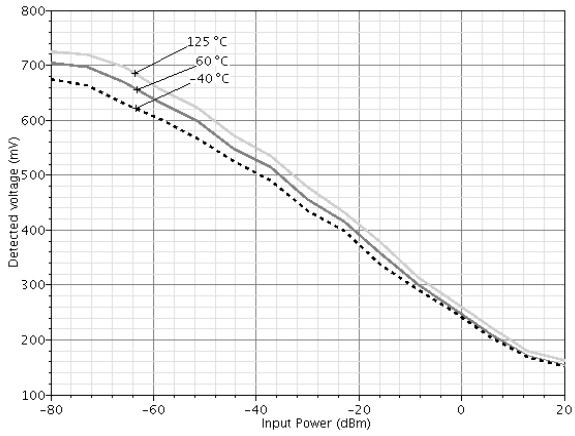

Fig. 7. Detected voltage versus input power at different temperatures.

Detected voltage versus input power at different temperatures is illustrated in Fig. 7. The biggest difference, about 40 mV, can be seen when input signal level has the lowest value. The logarithmic slope is approximately 7 mV/dB.

Figure 8 shows the detection error of the power detector at a temperature of 60^0 C. Input range of 65 dBm is achieved with ±2 dB error. The input range extends to 74 dBm at ±3 dB error.

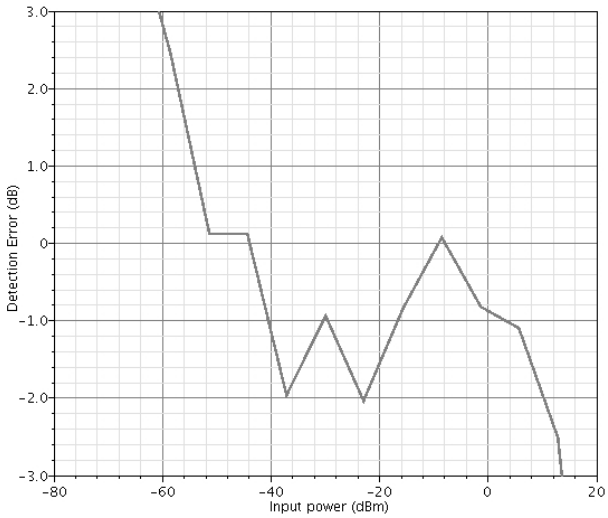

Fig. 8. Detection error versus input power at 60^0 C.

Detected voltage settling time is shown in Fig. 9 when the output voltage is taken directly from the RC circuit (Fig. 9(a)) and after it passes a low pass filter (Fig. 9(b)). Detected voltage filtering increases settling time. This should be taken into account when designing automatic calibration systems. Settling time for an unfiltered signal is 25 ns, while the filtered signal settles after 125 ns.

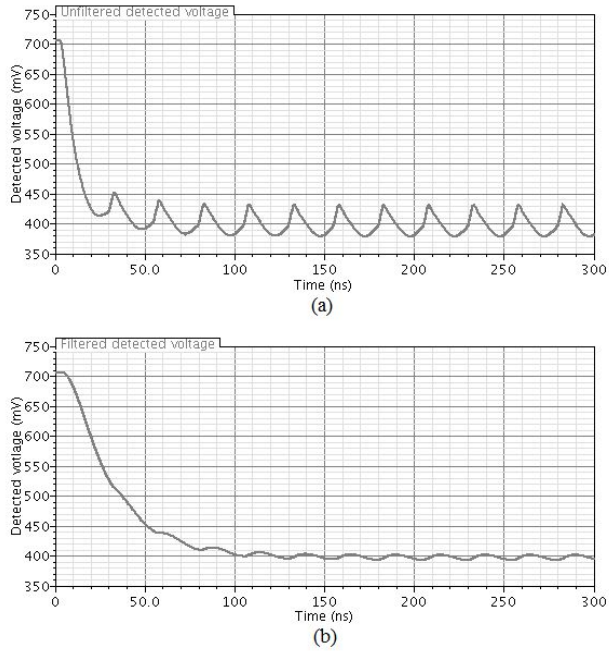

Fig. 9. Settling time differences without (a) and with (b) detected output voltage filtering.

Figure 10 shows transient simulation results of the limiting amplifier cascade when 1 GHz carrier frequency modulated by 20 MHz IF signal is fed into the power detector input. Voltage clipping (linearity degradation) starts when the output voltage reaches 0,8 V peak-to-peak.

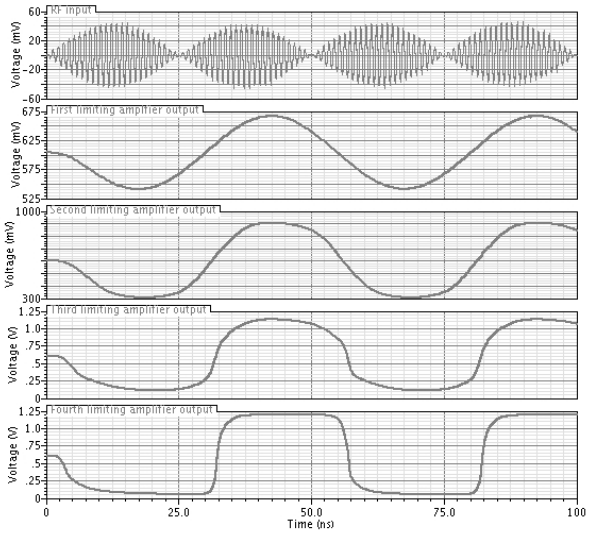

Fig. 10. Transient signals at different limiting amplifier cascade stages when and modulated RF signal is connected to the power detector input.

A summary of the simulated power detector is presented in Table I.

TABLE I. SUMMARY OF THE POWER DETECTOR.

Technology	65 nm CMOS
Supply voltage	1,2 V
Power consumption	24 mW
Dynamic range	74 dBm
Error	±2 dB (range 65 dBm) ±3 dB (range 74 dBm)
Slope	7 mV/dB
Layout area	350 µm x 240 µm

V. LAYOUT

Figure 11 shows the layout of the designed power detector.

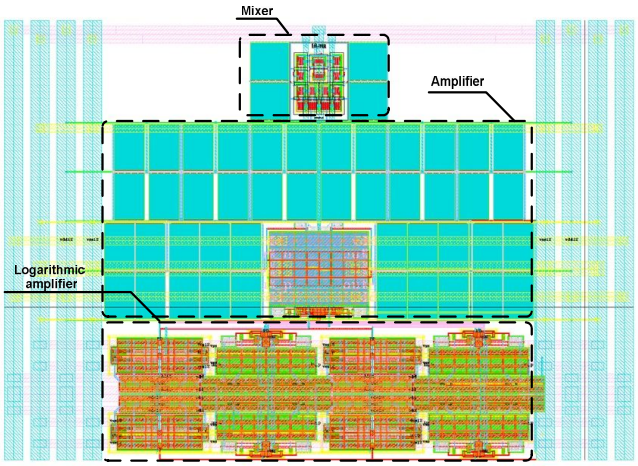

Fig. 11. Layout of the designed linear-in-dB power detector.

It occupies a die area of 350 µm × 240 µm with supply nets, where the core takes up 250 µm × 240 µm. The amplifier takes up most of the area due to large filtering capacitors that are present in the feedback loop.

VI. CONCLUSIONS

In this paper, the new architecture of the power detector (PD) is proposed with logarithmic amplifier, composed of limiting amplifiers and full-wave rectifiers, for linear-in-dB power detection. The PD architecture uses a mixer, driven by the same LO used in the transmitter chain, to down convert the RF signal, thus eliminating the need for high-speed components in the power detector core. Furthermore, the detection range can be controlled via PGA. Integrated circuit is designed and verificated using 65 nm CMOS technology and Cadence software package.

The dynamic range PD with an error of ±3 dB and ±2 dB is equal to 74 dBm and 65 dBm, respectively. A wide detection range ensures that the power detector can be used for LO leakage and output power detection. The maximum bandwidth of the IF signal that the PD can detect is equal to 57 MHz. Larger bandwidth detection is also possible, but the dynamic range will deteriorate. The supply voltage of PD is equal to 1,2 V and power consumption - 24 mW.

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