Design Considerations of an Amorphous Silicon Demultiplexer

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***Abstract*—This paper deals with the optimization of amorphous silicon gate driver circuits for active matrix array applications. It is based on static and dynamic models for hydrogenated amorphous silicon thin-film transistor operations. The models are extended to investigate amorphous silicon demultiplexer functionality. The proposed circuit is an improvement of an earlier published architecture. The circuit performance is discussed and demonstrated to be more reliable. It is shown that the response of the demultiplexer in terms of charging/discharging time is improved, the feed-through is reduced and the optimization of the circuit response is a reliable trade-off between stability and speed. This may contribute to overcome amorphous silicon technology shortcomings.**

***Index Terms*—Amorphous silicon, a-Si:H TFT, design optimization, demultiplexer.**

I. INTRODUCTION

In amorphous silicon (a-Si) technology, we deal with lower device performance compared to single crystal silicon. Successful integration of a-Si based circuits faces the challenges of low field mobility, high parasitic coupling and metastability [1]. So, we seek solutions to compensate for shortcomings inherent to amorphous silicon and build circuits meeting performance requirements. To solve the problem of metastability, two approaches are suitable. The first consists of designing circuits less sensitive to threshold voltage shifts. The second approach is to apply bipolar pulses instead of unipolar positive voltages, or to apply pulses with small duty cycle ratios which improve the circuit's lifetime [2]. Despite extensive study of amorphous silicon thin-film transistors' (a-Si:H TFTs) electrical instability [3], careful design is still needed for reliable circuits. Some of these circuits are gate drivers for AMLCDs' and AMOLEDs' applications. Several architectures were proposed [4]–[7] and, despite their feasibility and applicability, they present advantages and shortcomings due to the limitations of amorphous silicon. Their characteristics depend on the techniques used for implementation [8]. In this paper, a variant of one of these gate drivers using an analytical model of a coplanar structure of amorphous silicon TFT is presented. This model is described in detail in [9] for the static analysis and in [10] for the dynamic one. Using Cadence tools, the simulations were performed in Virtuoso analog design environment where the TFT model was described in a Verilog-A hardware description language. Typical direct and transfer characteristics obtained fora 100 µm/7µm a-Si:H TFT are illustrated on Fig.1 and Fig. 2, respectively.

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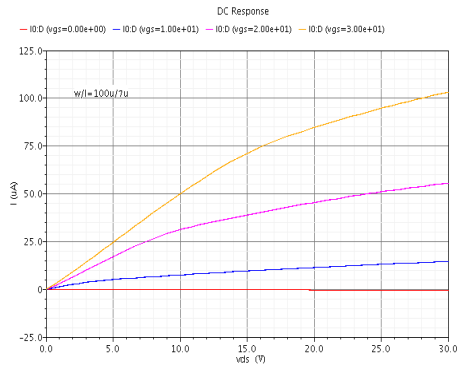

Fig. 1. Direct characteristics of an a-Si:H TFT.

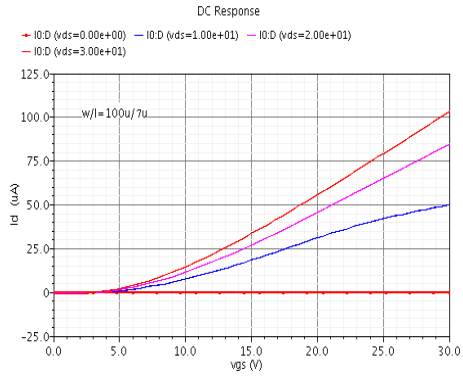

Fig. 2. Transfer characteristics of an a-Si:H TFT.

II. CIRCUIT DESCRIPTION

The proposed demux circuit is a variant of an architecture studied in [8]. The revision deals with the improvement of its performance for display applications. First, a 1:8 demux is considered. One branch of the circuit is presented on Fig. 3. It consists of three switching TFTs coupled in series in a pass transistor logic and an output transistor whose role is to make the output voltage insensitive to the variation of the TFTs' parameters. These TFTs drive the gate lines of the display array. The capacitance at the output represents the overall gate capacitance of all the TFTs connected to that

gate line. Pulse voltage sources which switch from V_{ss} to V_{dd} are used in order to avoid threshold voltage shifts. To improve the circuit response, I propose an alternative design which consists in the addition of a resistance R connected to the gate of the output transistor. Usually, this resistance is used to ensure a discharge path and to enable the output node capacitance to discharge to V_{ss} when the corresponding branch is not selected. In this case, the discharging path is ensured by the external pulse voltage source through the TFTs in series. The output transistor is forced to the saturation region instead of the linear one in order to improve demux speed. In this study, I am mainly interested in the circuit performance in terms of the effect of the additional resistance on response time and driving capability of the demux.

III. DEMUX PERFORMANCE

To estimate the requirements that the demux must yield, a frame frequency of 60 Hz is considered. As the frame rate is dominated by the time, t_{line}, for the demux to turn on all the switching TFTs on an entire row of the matrix [2], the demux must verify the condition of t_{line} value of 1/60/480 = 34.72 µs for 480 gate lines. With pass-transistors in series in each of its branches and a load capacitance at its end, a $1:2^N$ demux acts, for each selection, like an RC circuit where R is the sum of the ON resistances of the TFTs in series, and C the load capacitance C_L that it drives. This load is the gate line capacitance, normally the sum of all the capacitances of the TFTs constituting the addressed line in the matrix (neglecting the resistance of the gate metal). Thus, if a matrix of 480 × 640 pixels is considered, C_L will be estimated as 640 × C_{tft} where C_{tft} represents the gate capacitance of an a-Si:H TFT. For a TFT with WL=100 µm × 8 µm as gate surface and nitride thickness of 250 nm, C_{tft}=0.2 pF, which gives for C_L, 128 pF. In the simulations a value of 100 pF was taken. The resistance R_{ON} was found to be approximately 4 MΩ for WL=100 µm × 8 µm and V_G=30 V. Since the speed of the demux is governed by the time taken to charge and discharge the load capacitance, and if T_{ch} and T_{dis} are the times of the output (capacitance voltage) to rise from 10% to 90% and to fall from 90% to 10% of its steady state value, respectively, charging and discharging time is $2.2 \times 1 \times R_{on}C_L$, a value of approximately 0.88ms. This value is overestimated because the resistance of the transistor T_1 in saturation is neglected. According to its canonic form, a 1:2 demux should contain just one transistor per branch. The second device was added to simulate a realistic case and to estimate the effect of the on-resistance of pass-transistors on the signal applied to the gate of the output transistor. To reduce T_{ch} and T_{dis} one can reduce R_{on} and/or C_L. This leads to use transistors with higher W/L ratios respecting the pixel size. As mentioned above, the functionality of the circuit under study was tested by transient simulations performed in Virtuoso analog design environment where the developed TFT model was described in a Verilog-A code.

The select signal and the signals V_1 and V_2 are used to be bipolar pulses which vary from -30V to 30V and a duty cycle of 50%. The pulse width of V_2 is made larger to ensure that all the pixels in the display array are written. The simulation tests were run on R values varying from 50 MΩ to 1 GΩ. They revealed that this resistance must be large enough to allow maximum charging of the gate line capacitance. An example of the response of the 1:8 demux branch at different nodes is illustrated on Fig. 4.

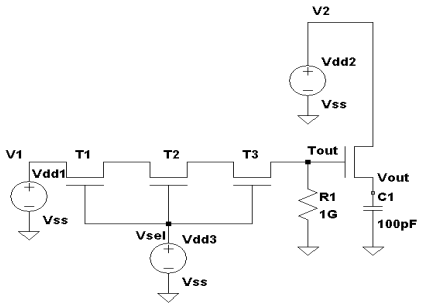

Fig. 3. One branch of the 1:8 a-Si demux.

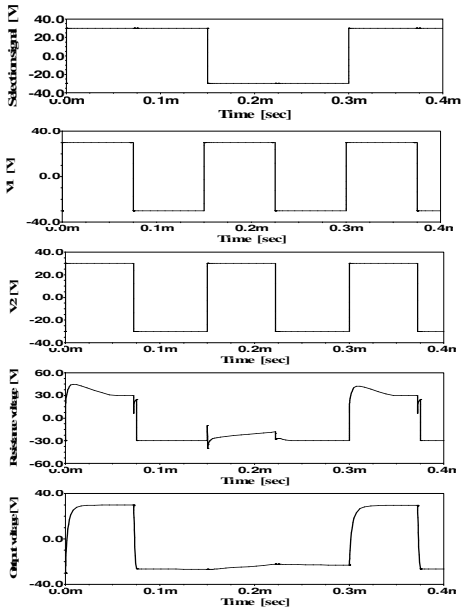

Fig. 4. Response of the 1:8 demux branch at different nodes.

The obtained waveforms show that the addition of R does not affect the demux operation. To investigate the performance of the proposed architecture, a 1:2 demux is studied for simplicity. For a larger demux, one would connect the different branches in parallel according to its canonic form. The complete circuit is shown on Fig. 5. V_{selb} is the inverted signal of the select signal V_{sel}. W_1/L_1, W_2/L_2 and W_{out}/L_{out} are, respectively, the aspect ratios of transistors T_1, T_2 and T_{out}. It should be noted that for this circuit variant, each branch has its own output transistor. This may improve the driving capability of the demux. The response in terms of charging and discharging times of C_L was investigated without, then with addition of resistance R. I first studied the effect of the output transistor sizing and the value of the resistance R on these parameters. The trends are illustrated on Fig. 6–Fig. 8. The simulations were performed for parameters, when constant, of W_1/L_1=W_2/L_2=150 µm /10 µm, L_{out}=10 µm, R= 1GΩ and W_{out}=400 µm. T_{ch} and T_{dis} were extracted as described above. The figures show that, despite the difference is not very large, the charging and discharging times values are lower when adding resistance R

compared to those without R, especially for lower values of L_{out} and W_{out}. As expected, with or without R, T_{ch} and T_{dis} decrease when L_{out} decreases, W_{out} increases and R increases. In fact, when the output transistor has a relatively short channel and when it is large enough, its current driving capability becomes important helping achieve the charging/discharging requirements. This is improved by biasing T_{out} in the saturation regime.

The resistance accelerates T_{ch} and T_{dis}. On the other hand it appears that for the same range of variation of R the charging operation is accelerated compared to the discharging one (T_{dis} is smaller than T_{ch}). Adding resistance R seems to have no effect on the discharging time, because the discharging path is ensured by the series transistors of the chain.

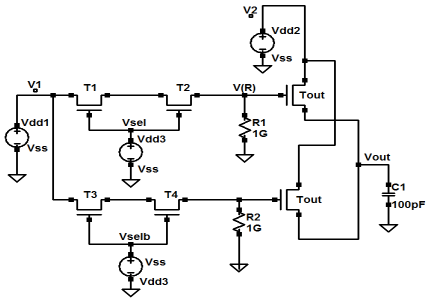

Fig. 5. The 1:2 a-Si demux under study. For the transistor added in a branch, see the text.

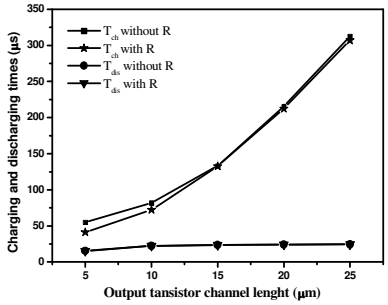

Fig. 6. Effect of the output transistor length on the charging and discharging times, with and without R.

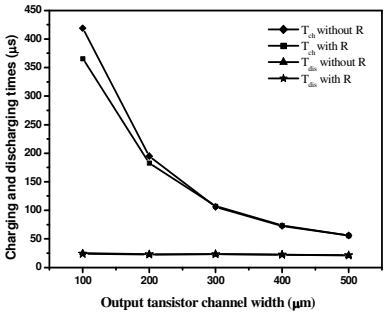

Fig. 7. Effect of the output transistor width on the charging and discharging times, with and without R.

As the voltage V(R) at the resistance node is directly applied to the gate of the output transistor, I have investigated the role that may have the sizing of the series transistors on the output gate transistor and then on the demux response, with and without addition of R. Figure 9 and Fig. 11 show this role.

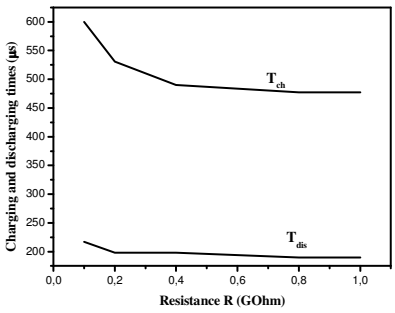

Fig. 8. Effect of the resistance value R on the charging and discharging times.

Figure 9 presents the variation of T_{out} gate voltage as a function of width of transistor T_1. While the gate voltage of T_{out} change slightly with W_1 without addition of R, it increases with this parameter from 10 µm to 100 µm, then becomes almost stable as W_1 increases when R is added.

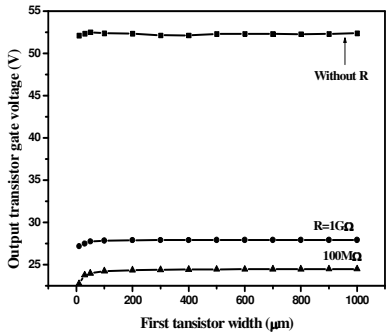

Fig. 9. Output transistor gate voltage vs first transistor width, with and without R.

The same trends are observed for the variation of the output transistor gate voltage with the width of transistor T_2 when R is added (Fig. 10). However, without addition of R, the gate voltage of T_{out} decreases with increase of W_2, then stabilizes when W_2 reaches 400 µm.

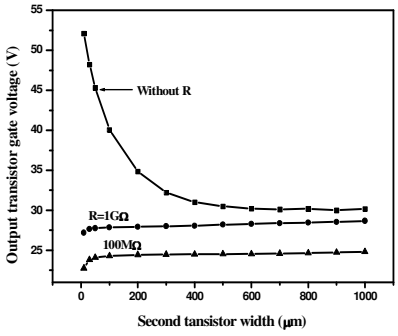

Fig. 10. Output transistor gate voltage vs second transistor width, with and without R.

Figure 12 shows the variation of T_{out} gate voltage and feed-through without and with addition of resistance R. An overlap gate-to-source capacitance of 50 nF was used. It appears that, even feed-through increases with increasing R value because of the increase of the output transistor gate voltage, it remains lower than that without addition of resistance R (a voltage of 28.52 V and a feed-through of 2.16 V). The improvement varies from 10 mV for R=1 GΩ to 20 mV for R=50 MΩ and is more significant for larger overlap capacitances. In fact, without resistance R, the pass-

transistors see the gate capacitance of the output transistor as output capacitance. If the overlap is important, feed-through may occur when T_{out} passes from on-state to off-state [11], [12]. The capacitance coupling between the transistor gate and source may lead to a voltage drop in the output signal. Therefore, adding R reduces this effect.

From the above descriptions, one can observe that the addition of resistance R gives an indication of one way to minimize the output transistor gate voltage and feed through voltage. This helps in minimizing the thresholdvoltage shift when the transistors' sizing is optimized and leads to a stability of the demux circuit and to an optimization of circuit layout. On the other hand, the driving capability and the speed of the demux are enhanced with large values of resistance R and larger transistors. Demux response is thus improved even it is not advantageous when designing the circuit layout. Thus, the trade-off between increasing transistors' aspect ratios to balance the charging and the discharging times and decreasing these parameters for a feed through voltage minimization is very clear.

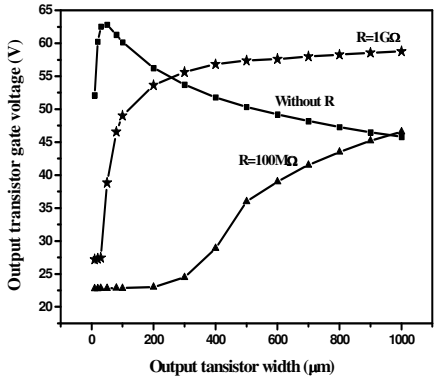

Fig. 11. Output transistor gate voltage vs output transistor width, with and without R.

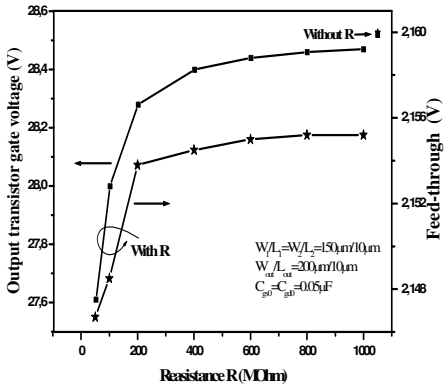

Fig. 12. Output transistor gate voltage and feed-through vs resistance R value, with and without R (the values without R are illustrated for comparison).

The obtained results, namely those related to the propagation delay, driving capability and stability are similar to those obtained in the literature where the feasibility of integrating gate drivers in amorphous silicon technology for active matrix display and imaging arrays was proven experimentally. In [2] and [5] for example, similarities in terms of order of magnitude for the delay time and resistance values, respectively confirm that higher values of resistances and larger transistors help in achieving better reliability for long term operation.

IV. CONCLUSIONS

Throughout this paper, developed static and dynamic models for a-Si:H TFTs operations have been described in a Verilog-A hardware description language and extended to probe an a-Si demux functionality. The demux is proposed for active matrix array applications as an improvement of an earlier published architecture. Some issues related to the demux design are addressed and suggestions for the optimization of the circuit layout, driving capability, stability and speed are presented. With reference to these issues, the proposed circuit exhibits better performance and is subject of a trade-off between threshold voltage immunity and speed.This is crucial to build reliable gate drivers.

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