A Low Power 0.18-µm CMOS Phase Frequency Detector for High Speed PLL

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***Abstract*—This paper presents a modified high speed CMOS dynamic phase frequency detector (PFD) for high frequency phase-locked loop (PLL). Design miniaturizations in downscaling CMOS process lead to circuit malfunction due to intrinsic effects and many other reasons. To ensure main characteristics of the PFD are preserved, the proposed dynamic PFD uses 18 transistors operated with 1.2 V power supply. The performance of the design is focused on power supply, power dissipation, wide input frequency range, dead zone size and active layout area. The circuit is designed in 0.18 µm CMOS process using Mentor Graphics environment. In this paper, the dynamic PFD dissipates 59 pW of total power when reference input frequency clock operates at 50 MHz and feedback input frequency clock operates up to 4 GHz. The dead zone has been eliminated. The simulation results show that the circuit offered an alternative for any high speed and low power PLL applications.**

***Index Terms*—Dead zone, low power, PFD, PLL.**

I. INTRODUCTION

In many designs, PLLs are widely used for clock phase synchronizations, frequency synthesizers, communication systems, high performance microprocessors and digital circuits [1], [2]. A typical PLL block diagram shows in Fig. 1.

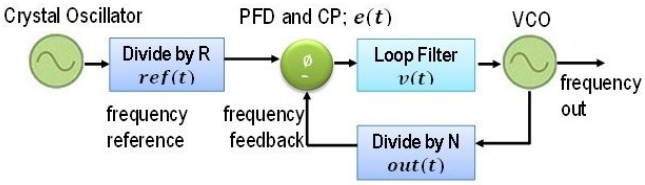

Fig. 1. Block diagram of typical charge pump PLL (CPPLL).

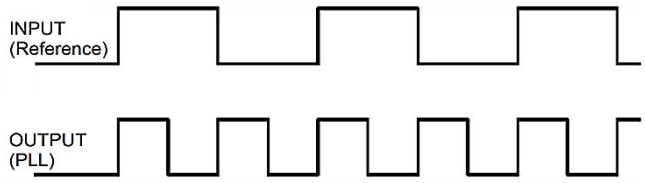

Fig. 2. PLL in lock.

A feedback system of PLL causes the output of voltage-controlled oscillator (VCO) signal tracks the external reference signal, REF in phase and frequency. When both VCO's output signal and REF signals are synchronized, i.e. phase difference between them is constant with time and their frequency difference is zero, then the PLL is said to be in locked condition as shown in Fig. 2.

A common PLL architecture uses PFD in its system to simultaneous clock phase and frequency acquisitions [3]. The accuracy of the PFD functionality will provide attractive tracking and locking performance of the PLL is crucial since a tiny difference in the input clock frequency can accumulate very fast in which the phase error can grow significantly after a few cycles and can jeopardize PLL functionality especially in multi-gigahertz applications [4].

II. LITERATURE REVIEW

The simplest comparator used XOR gates that able to generate Boolean difference between two clocks [4]. However, the primary problem of XOR PFD is it suffers the dead zone which caused by the pre-charge time of the internal nodes, especially any design that built from memory elements. A reset signal is used to clear those memory elements and reset time depends on the gate delays in the circuit, but not on the clock [5]. Consequently, if the PFD input frequencies phase difference falls into dead zone during PLL frequency acquisition, PFD tends to deliver incorrect phase information to the charge pump and shift toward the position direction which aggravates the cycle slips and prolong the frequency pull-in time. These factors caused PLL locks to a wrong phase [6], [7].

There are a few techniques to eliminate dead zone in PLL system. One of the techniques is by adding an appropriate delay to the PFD reset path and make delay reset path longer than the switching time of the charge pump current. Secondly, by activating UP and DOWN signals simultaneously just for a short time but still can quickly turn on the CP's switches for charging/discharging the load capacitance [6]–[8]. In this work we are focusing on the former technique in which sufficient delay reset is achieved by using internal signal routing.

Heat dissipation has limited the feasible packaging and performance of the VLSI chip. Since dynamic power dissipation in synchronous digital integrated circuit is determined by the product of parasitic capacitance (C), square of supply voltage (V) and operating or clock frequency (f), thus, keeps a low supply voltage is an

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effective way to reduce power dissipation of the modern electronic system. Previous works on [3]–[4], [6] PFDs have been employed and simulated in 0.18 µm process. The simulation results indicated that the simulated designs have drawback on high power dissipations when operated at high frequency. They also consumed large layout area due to a large number of transistors due to the implementation of delay cells placed at external reference input signal (CLKREF) path and feedback VCO input signal (CLKVCO) path to avoid the dead zone effects.

A conventional PFD as depicted in Fig. 3. It consists of logic gates which suffer from dead zone, blind zone, limited frequency range, slow PLL locking time and frequency acquisition. Conventional PFD also has inappropriate delay to reset internal nodes which affect the PLL speed. In modern era, dynamic PFD shown in Fig. 4 dominates the market to overcome the problems. It is also called as tri-state PFD which referring to the operations of UP circuit, DOWN circuit and reset circuit. Flip-flops with dynamic logic design techniques are including non-clock PFD, tspc-PFD, pre-charged PFD and fe-PFD. However the dead zone remains a challenge for the PFD to operate in high speed PLL.

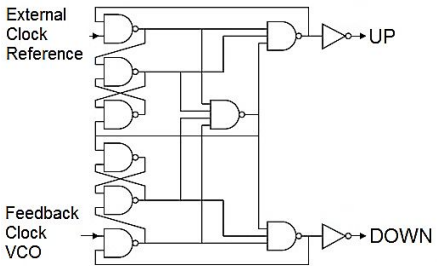


Fig. 3. Conventional logic gates PFD.

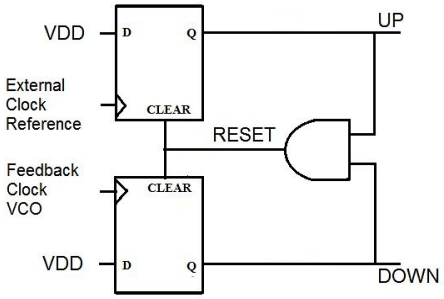


Fig. 4. Typical tri-state PFD block diagram.

In this paper, we analysed digital transfer characteristic of different dynamic PFD topologies. The simulations and analysis have considered all three possible conditions of the operating PFD; (1) when both CLKVCO and CLKREF inputs matched (2) when CLKREF leads CLKVCO input (3) when CLKVCO leads the CLKREF input. We have further investigated high speed dynamic PFD by using pre-charge principles. Finally we have overcome the misleading PFD output in [9] when the CLKREF leads the CLKVCO occurred due to the design miniaturization issue. Furthermore, by having the smallest channel length in circuit design, it allows a direct device shrink with the scaling of CMOS technology. We have also further reduced the dead zone effect, developed small and compact layout architecture, improved the total power dissipations and introduced a lower power supply which is 1.2 V compared to 1.8 V used in the similar works by Ismail *et al.* [2] and Thakore *et al.* [9]. We have also exceeded the limited input frequency range as reviewed Lule *et al.* [10].

III. CIRCUIT DESCRIPTION

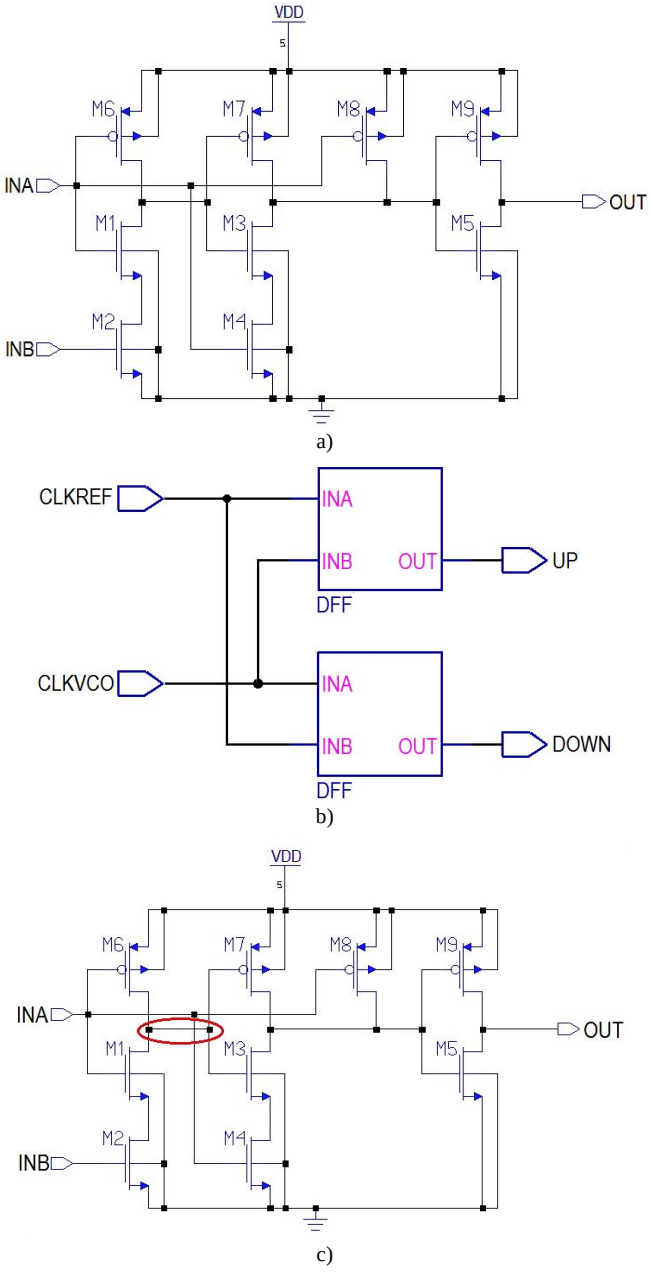


Fig. 5. Utilized UP dynamic schematic with inverter [9] (a), top level schematic of the high speed PFD (b) and modified DOWN dynamic schematic with inverter by [9] (c).

Reset path of typical tri-state PFD depicted in Fig. 4 has been eliminated in this high speed dynamic PFD by rerouting the PFD input connections to the next flip-flop. The input of one flip-flop plays a role to generate reset signal for the other flip-flop. Basic operation of this design is to push UP signal to level high when CLKREF is leading while the reset path pulls the other flip-flop to be grounded. The same condition applies to the second scenario in which DOWN is at logic high when CLKVCO leads the CLKREF and pull the other flip-flop to be grounded. The circuit by Thakore *et al.* [9] has been utilized with the smallest device sizes possibly drawn in 0.18 µm process to obtain a high speed phase frequency detector as depicted in Fig. 5. To

solve misleading issue of this design in 0.18 µm CMOS process; (1) a modification is proposed as marked in the red circle (2) perform connection from inverter output of the first stage (UP flip-flop) to drive NAND input of the second stage (DOWN flip-flop).

IV. Results And Discussion

Post layout simulations were accomplished in 0.18 µm CMOS process technology with 1.2 V and 1.8 V power supply by using Mentor Graphics (DA-IC) EDA tool. The width and length of the transistors were fixed as W/L_{PMOS} = 0.5 µm/0.18 µm and W/L_{NMOS} = 0.5 µm/0.18 µm. The simulation output waveforms as shown in Fig. 6(a)–Fig. 6(c), and completely fulfilled all PFD basic functionalities.

The small spikes at dead zone found around 76 mV peak-to-peak high and top and bottom peak are as low as 30 mV which is close to 0 V and formed approximately zero pulse width. Total power dissipation of this modified dynamic PFD achieved only 59 pW exhibiting the lowest among the rest of the designs implemented earlier.

Figure 6(b) and Fig. 6(c) show the expected waveforms when the CLKREF leads CLKVCO for 3 ns and vice versa. Simple modification implemented into the design has successfully detect both input signal rising and falling edges. Moreover, lower power supply is desired in achieving a low power design. From simulation result, lower power supply 1.2 V alleviated rise time delay of UP and DOWN pulses when CLKREF signal leads or lags the CLKVCO compared to the simulation result of 1.8 V power supply. From these findings we can deduce the most effective and simplest approach to reduce power dissipation in CMOS design; (1) by reducing the supply voltage due to the quadratic dependence of the power dissipation on the supply voltage (2) by minimizing the size of transistors in both width and gate length.

In this work, all of the PFD conditions (leads, lags or match CLKREF and CLKVCO inputs) are met when tested with different input frequencies. The simulation output waveforms of 50 MHz to 4 GHz input frequencies are overlaid respectively as depicted in Fig. 7. The output exhibits this modified high speed dynamic PFD maintained its circuit performance operated under low power supply range (1.2 V). The output wave patterns remain consistent regardless the speed of input frequencies introduced.

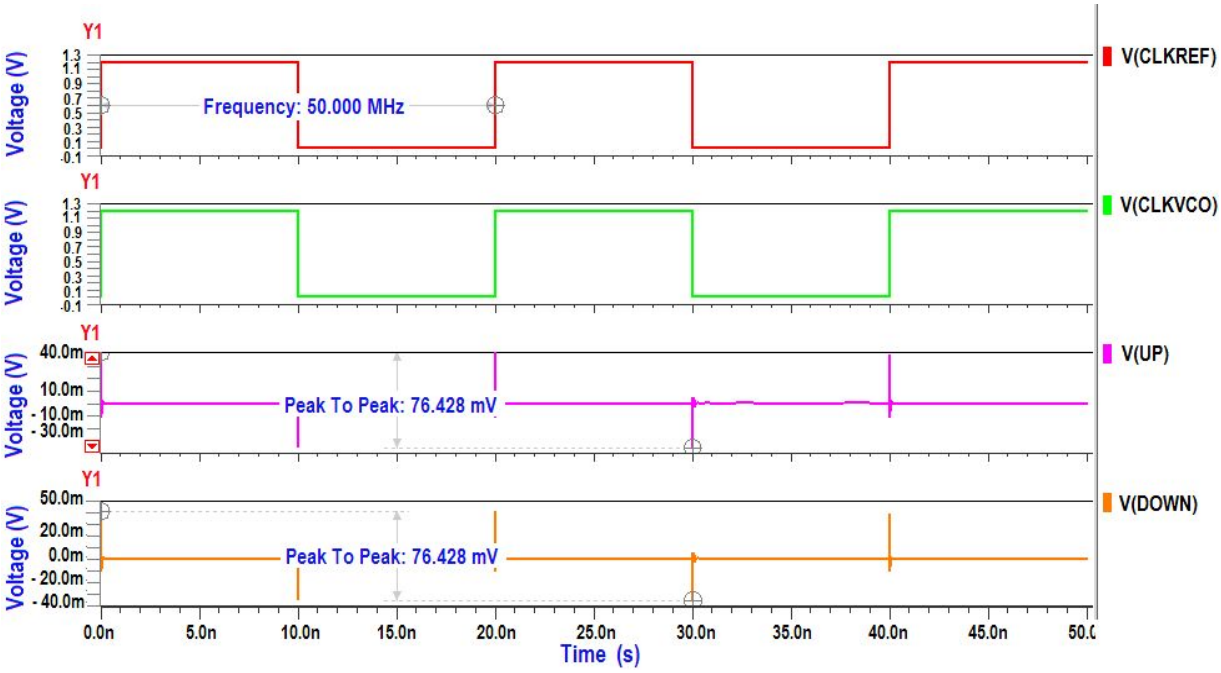
This design has the smallest dead zone of 2 ps considering the rise time and fall time of the CLKREF and CLKVCO input signals in the simulation are fixed at 1 ps. Hence, the penalty of having approximately to zero dead zone size would be insignificant to the PLL. The smallest phase difference detected defines the best sensitivity of the design. Undetected phase difference defines as dead zone which any transitions of input frequencies will not be seen by the PFD.

Low frequency circuit design operation usually has high capability to detect the smallest phase differences when operates at low frequency (50 MHz). The sensitivity of this high speed dynamic PFD remained high when processing 4 GHz of feedback input frequencies.

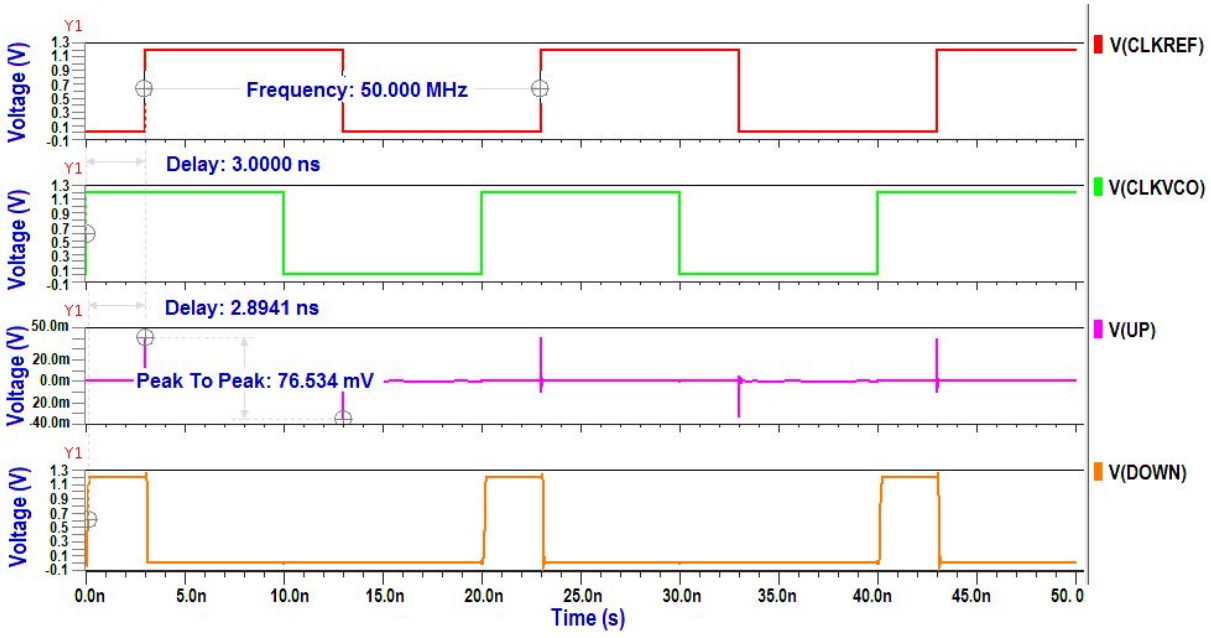
The layout active area of this work is drawn in 101 µm^2 shown in Fig. 8. Parallel critical signals are spaced out more than its minimum spacing to avoid cross-talk, apposite p-taps and n-taps are placed to avoid massive latch-up between devices and practice short signal routings to minimize the RC effects.

In this work we found that the stability of the design in 0.18 µm process technology gives more flexibility for the researcher to design according to the application needs. Moreover, custom circuit design of the dynamic flip-flop has contributed to the low power operation and a compact active area.

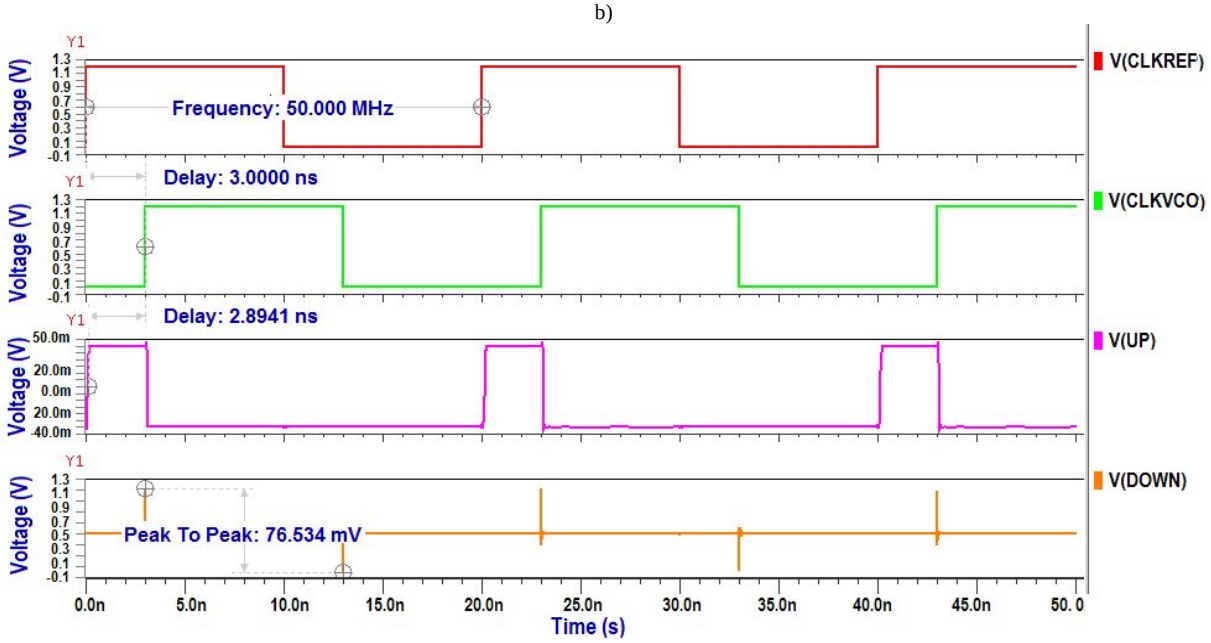
Learnt that conventional tri-state PFD has weaknesses of large power dissipations and delay variation due to current driving capabilities of the transistors frequently have issue to operate at low supply core voltage VDD. This problem has resolved in this high speed dynamic PFD as it satisfies the demand of digital circuit design and befitting a modern operating system running on a multi-gigahertz.



a)



b)



c)

Fig. 6. Modified high speed dynamic PFD output waves for all three conditions.

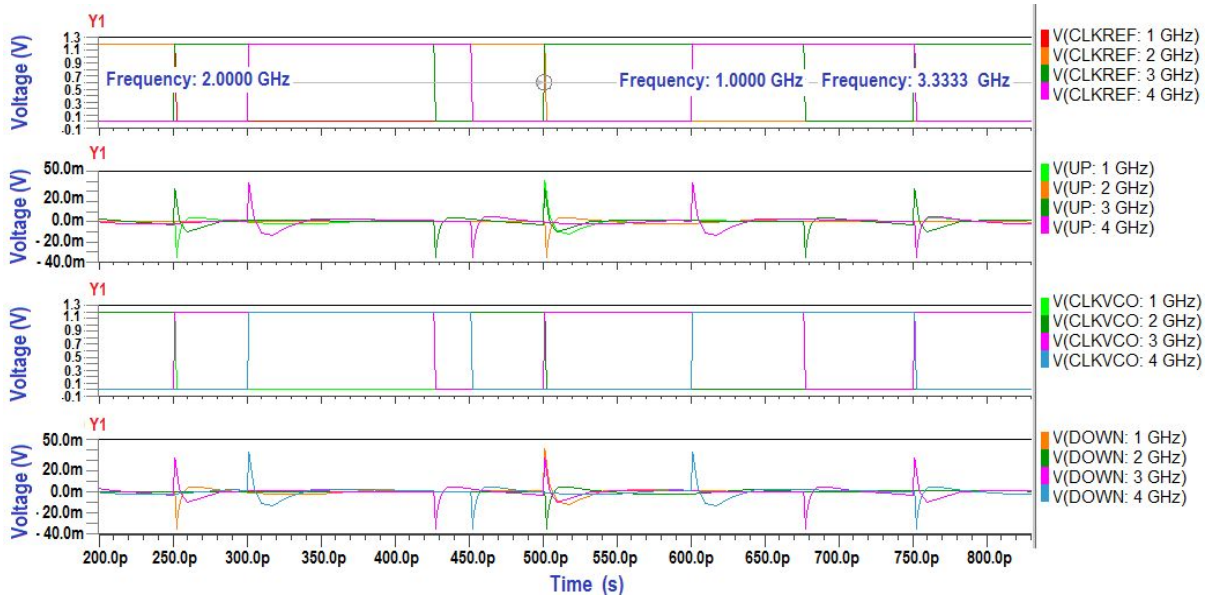


Fig. 7. Modified high speed dynamic PFD operates at matched inputs (locked) in the range of 1 GHz – 4 GHz.

TABLE I. PERFORMANCE COMPARISONS WITH PUBLISHED WORKS.

Ref.	CMOS Process	Power Supply (V)	Total Power Dissipation (W)	Reference Frequency (MHz)	Dead Zone (ps)	Transistor Counts	Layout Area (μm²)
[2]	0.18 μm	1.8	6.6 μ	50	0	12	N/A
[8]	0.18 μm	1.8	-	10 - 25	120	24	N/A
[9]	0.18 μm	1.2	870 p	50 - 100	2	18	N/A
[13]	0.18 μm	1.0	3 m	50	0	24	N/A
[15]	0.18 μm	1.8	1.56 m	50	-	22	N/A
[14]	65 nm	1.08	8.8 m	50	1	-	N/A
This work	0.18 μm	1.8	118 p	50	0	18	101
		1.2	59 p				

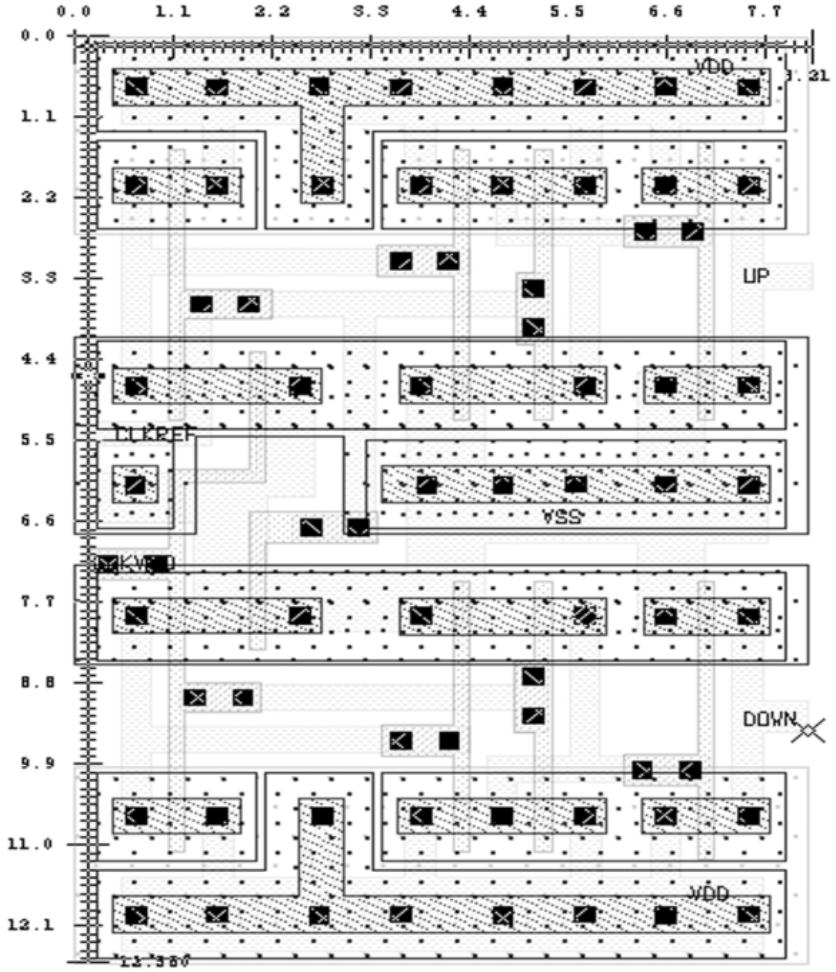


Fig. 8. Modified high speed PFD layout design.

Table I compares the simulated performance of this work high speed dynamic PFD to previous architectures. The PFD designed by Fan *et al.* [13] is the best choice for a device with low power operation however power dissipation of 3 mWatt are relatively high for a digital circuit for 0.18 μm process. It also consumed huge area on chip due to the error amplifier circuitry utilized in the charge pump. Hsu *et al.* [14] has developed deep-submicron device sizes. In this work it exhibits power dissipation has been traded-off with smaller device sizes. Other research works designed by using 0.18 μm process including Soh *et al.* [8] and Chen *et al.* [15] operated under 1.8 V power supply, indicate that it both need higher input power supply compare to 1.2 V used in this work. Thakore *et al.* [9] presented PFD operates under 1.2 V power supply however it has 820 pWatt power dissipation which is higher compare to this work due to the effect of big transistor sizes. Ismail *et al.* [2] developed a PFD with less number of transistors count, however it has limitation in detecting the input phase difference as the detection is works at inputs falling edge only.

V. CONCLUSIONS

A simple dynamic phase frequency detector (PFD) with low input power supply of 1.2 V presented. This design maintained the circuit stability when operate at both low and very high frequency. The dead zone of undetected input frequencies phase difference of this design has been eliminated. The peak-to-peak spikes are as low as 76 mV which is insignificant to PLL overall performance. The design is simulated with 0.18 μm CMOS process and drawn in a compact layout with active area of 101 μm². Total power dissipation is 59 pW which is lower than other typical

PFDs that gives the designers better options in developing high speed PLL devices.

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