# Recent Developments in Inverter Topologies for Direct Torque Controlled Induction Motors

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***Abstract*—Direct torque control (DTC), an industrial standard for applications requiring high dynamic performance in induction motors, has reached its performance limits owing to the high torque ripple and acoustic noise generated by traditional two-level inverters. This comprehensive review examines the technological evolution of power converter topologies developed to extend the performance limits of DTC, from classic multilevel structures, such as neutral point clamping and cascaded H-bridge, to recently developed reduced-switching-count and asymmetric hybrid topologies. The study also details the integration of matrix converters, which increase power density, and open-ended winding (OEW) architectures, which enable voltage optimization, with DTC. The article compares existing topologies in terms of cost, efficiency, and harmonic performance and provides critical projections on how silicon carbide (SiC)/gallium nitride (GaN)-based wide bandgap semiconductors and fault-tolerant designs will transform future electric drive systems, thereby offering a strategic roadmap for researchers and design engineers.**

***Index Terms*—Direct torque control; Induction motor; Inverter topology; Matrix converter; Multilevel inverter; Wide-bandgap semiconductor.**

## I. INTRODUCTION

Induction motors (IM) are essential components of industrial production systems and recently accelerating electric vehicle (EV) technology owing to their robust construction, low cost, ease of maintenance, and resistance to harsh operating conditions. In particular, in applications requiring variable speed and torque, such as pumps, fans, compressors, and traction systems, the performance of these machines is directly dependent on the topology of the power electronics converter used and the control strategy applied [1], [2]. Direct torque control (DTC), developed by Takahashi and Noguchi in the mid-1980s, stands out compared to field-oriented control (FOC) due to its structure that does not require coordinate transformations and pulse width modulation (PWM) blocks, its fast dynamic torque response, and its robustness against parameter change [3]. However, the classic DTC scheme, which has become an industrial standard, struggles to meet the requirements of modern high-performance drivers when implemented with traditional two-level voltage-sourced inverters (2L-VSIs) because of internal structural limitations.

The most significant disadvantages of the classic two-level inverter and hysteresis-based DTC combination are high torque and current ripple observed at low speeds and in the steady state, the variable switching frequency, and the high total harmonic distortion (THD) in the generated output voltage [4]. Additionally, particularly in medium-voltage drives and new-generation EV battery systems that are transitioning to the 800 V level, the high dv/dt stress applied by two-level structures to motor terminals threatens motor winding insulation, causes bearing currents, and causes serious electromagnetic interference (EMI) problems [5], [6]. These issues cannot be fully overcome simply by improving the control algorithm (e.g., by adding artificial neural networks or model predictive control); they necessitate a fundamental change in the hardware infrastructure, namely the inverter topology. In this context, multi-level inverters (MLIs) provide an ideal hardware platform for DTC applications because they naturally reduce harmonic content by synthesizing the output voltage in a staircase pattern, divide the voltage stress on the switching elements, and deliver high power quality at lower switching frequencies [7], [8].

A review of the current literature reveals that in addition to classic MLI topologies such as neutral point clamped (NPC), cascaded H-bridge (CHB), T-type, and flying capacitor (FC) aim to improve the performance of the DTC method, matrix converters (MC) that do not require a DC bus capacitor, and cost-focused reduced switch count (RSC) topologies are also being intensively researched [9]. For example, three-level and higher topologies provide the DTC algorithm with a much richer voltage vector space, enabling more precise compensation for torque and flux errors and thus minimizing fluctuations [10], [11].

The primary objective of this study is to provide a comprehensive classification of the inverter topologies employed in DTC-based induction motor drives by critically comparing their impacts on torque ripple, harmonic performance, cost, and control complexity, ranging from classical structures to advanced multilevel and hybrid architectures.

This compilation study is based on a systematic literature review aimed at comprehensively analyzing current research,

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technological developments, and future trends in the field of MLI topologies for IM drives. To ensure access to the most authoritative academic publications, a systematic search protocol was implemented across the most reputable databases in power and industrial electronics: IEEE Xplore, Web of Science, Scopus, ScienceDirect, and Springer. In addition to these primary academic indexes, Google Scholar was utilized to broaden the search scope, examine relevant grey literature, and perform cross-verification of the findings.

These platforms were selected because of their extensive coverage of high-impact journals and peer-reviewed conference proceedings. The search query utilized a combination of Boolean operators (AND, OR) and keywords, including: *"Direct Torque Control"*, *"Multilevel Inverter"*, *"Matrix Converter"*, *and "Induction Motor"*. The search timeframe was strictly set from 2010 to 2026 to capture both the foundational developments and the most recent breakthroughs in wide-bandgap (WBG) semiconductors and AI-enhanced control algorithms.

The selection process was strategically designed to capture the most impactful and technically relevant advancements in the field. The inclusion criteria were as follows:

– Studies focusing primarily on IM, as these represent the most prevalent machines in modern industrial DTC applications;

– Research published in high-impact journals and highly-cited review articles that provide a foundational synthesis of the field;

– Recent publications from 2010 to 2026, with a particular emphasis on the 2021–2026 period to incorporate the latest trends in semiconductors and advanced control methods.

The literature synthesis was executed through a rigorous multistage screening framework to ensure the highest technical relevance and scientific integrity. Initially, a broad search across leading academic databases identified a pool of approximately 900 publications. In the second stage, focused filtration was applied, targeting studies specifically aligned with the IM architecture, advanced DTC strategies, and the investigated multilevel/matrix inverter topologies. This phase narrowed the scope to 180 high-potential studies, which underwent a comprehensive full-text evaluation.

Finally, based on the robustness of their empirical validation and contribution to the current state-of-the-art, 127 landmark publications were selected for inclusion in this review. By prioritizing high-impact journals and seminal review articles, this methodology ensures that comparative analysis is anchored in the most authoritative and up-to-date evidence available in the power electronics field.

The remainder of this paper is organized as follows. Section II establishes the theoretical foundation by focusing on the operation of inverters within DTC-controlled induction motor drives. Section III provides a detailed examination of MLI topologies and their impact on DTC performance. Section IV introduces new-generation inverter architectures and their specific DTC applications, followed by Section V, which analyzes matrix converter-based DTC strategies known for eliminating DC-link capacitors. Section VI presents a comparative evaluation of the discussed topologies, identifying their respective advantages and limitations. In Section VII, a comprehensive performance assessment is conducted in terms of cost-effectiveness, efficiency, and harmonic distortion while exploring how wide-bandgap (SiC/GaN) semiconductors and fault-tolerant designs are reshaping the future of electric drives. Section VIII discusses the integration of these high-performance drives into Industry 4.0 frameworks, highlighting the role of IoT-based monitoring and digital twin technologies. Finally, Section IX concludes the study by offering strategic insights and directions for future research in the field.

## II. INVERTER REQUIREMENTS FOR IM DTC

The DTC principle is fundamentally based on controlling the motor's stator flux vector and electromagnetic torque directly through the inverter's switching states without any coordinate transformation or current regulator [12]. In this structure, the stator flux magnitude and the torque error are digitized via hysteresis bands and combined with the sector information of the stator flux vector to select the optimal voltage vector from a look-up table (LUT) [13]. The primary objective of the hysteresis controllers used in the classic DTC scheme (two-level for flux and three-level for torque) is to produce the fastest dynamic response by minimizing dependence on motor parameters [14]. The traditional DTC block scheme is shown in Fig. 1.

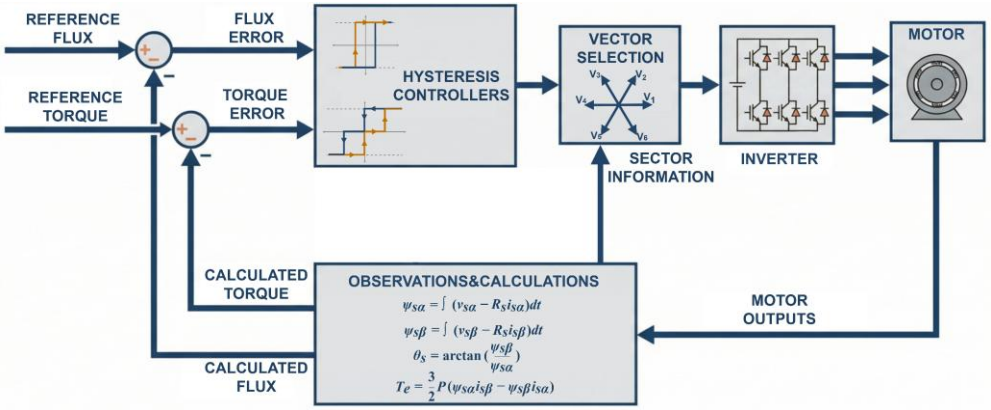


Fig. 1. Hysteresis-based DTC system architecture and fundamental control equations.

However, the success of this control strategy is directly related to the resolution of the voltage vectors that the inverter can provide and the flexibility with which it can use the DC bus voltage [15]. Therefore, the mathematical demands of the DTC algorithm create three critical requirements for inverter hardware: an increased voltage vector count, efficient DC bus

utilization, and limitation of common-mode voltage (CMV).

Classic two-level inverters can provide only eight voltage vectors in the space vector plane, with six active vectors and two zero vectors; this causes the stator flux path to deviate from its ideal circular form and exhibit a hexagonal structure, resulting in increased torque ripple [16]. The primary feature expected of an inverter to improve DTC performance is the ability to generate a greater number of voltage vectors with different amplitudes (large, medium, and small) in the space vector plane. MLI topologies overcome this limitation by offering a greater number of switching combinations; for example, 27 in a three-level structure and significantly more in a five-level structure [17]. This increase in the number of vectors allows the plane containing the stator flux vector to be divided into 12 or 24 sectors instead of the conventional six sectors, thereby enabling torque and flux errors to be compensated with smaller and more precise voltage steps [11], [16]. In particular, at low speeds and under transient conditions, the "medium" and "small" amplitude vectors provided by the inverter are critical to preventing drops in stator flux (flux droop) and smoothing the torque response [18].

The second critical aspect expected from an inverter design is the effective use of the DC bus voltage and the balancing of capacitor voltages. In applications where the DC source is a battery or fuel cell, such as electric vehicles and renewable energy systems, the inverter must minimize switching losses and maintain a low harmonic content when transferring the DC bus voltage (Vdc) to the motor terminals [19]. In MLI structures, such as NPC or T-type, the potential shift of the DC bus midpoint (neutral point unbalance) can cause disturbances in output voltage and excessive voltage stress on semiconductors, thereby compromising the stability of the DTC [20]. Therefore, an inverter driven by the DTC algorithm is expected to have a topology that also accounts for the effects of the selected switching states (redundant states) on the charging or discharging of the DC bus capacitors [21].

Finally, one of the most important features expected from inverters in modern drive systems is the management of CMV, which causes damage to motor bearings and EMI. Owing to the nature of DTC, its hysteresis-free and asynchronous switching structure tends to generate high-frequency CMV components at the inverter output [22]. Although reducing CMV in traditional two-level inverters typically requires passive filters, MLI topologies offer the flexibility to select vector combinations that produce zero CMV or limit CMV amplitude to low levels, such as Vdc/6. In this context, an ideal DTC inverter should possess switching capabilities that ensure not only torque production, but also the motor insulation life and electromagnetic compatibility of the system. The topologies developed to meet these requirements differ in terms of structural complexity and cost.

## III. Classic Multi-Level Inverter Topologies

Classic MLI topologies, developed to meet hardware requirements such as the increased number of voltage vectors expected from the inverter and DC bus usage flexibility in the control of induction motors using DTC, and which have become industrial standards, include diode-clamped, flying capacitor, and cascaded H-bridge structures. This section examines the structural characteristics of these topologies, their integration with the DTC algorithm, and, in particular, the dynamics of balancing the neutral point and capacitor voltages, based on fundamental and current studies in the literature.

### *A. Diode-Clamped Inverters*

The NPC inverter, introduced to the literature by Nabae, Takahashi, and Akagi in 1981 [23], is the most commonly used topology in medium-voltage industrial drives. A three-level NPC (3L-NPC) structure divides the DC bus by two series capacitors and uses clamping diodes to create +Vdc/2, 0, and −Vdc/2 voltage levels at phase output [24]. This structure enables the space vector plane to be divided into 12 sectors instead of six in the DTC strategy, allowing for more precise control of the torque and flux errors. Furthermore, T-type inverters, which are derivatives of NPCs, are gaining popularity in electric vehicle applications because they offer lower transmission losses than the NPCs, particularly at medium switching frequencies and partial loads [25]. The NPC inverter topology is illustrated in Fig. 2.

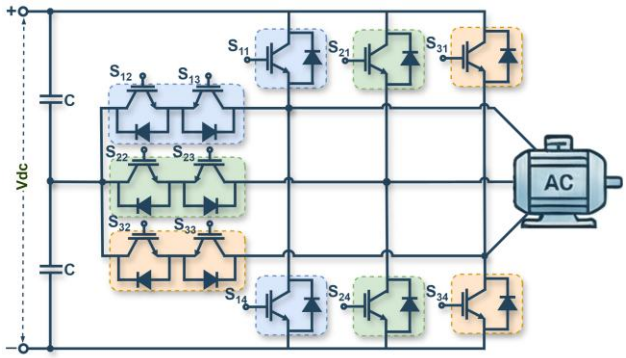


Fig. 2. Circuit diagram of the three-phase, three-level locked-in diode (NPC) inverter topology.

Although this structure provides an excellent platform for reducing harmonic distortion and dv/dt stress at the motor terminals, maintaining equal capacitor voltages in hysteresis-based control methods, such as DTC, is challenging. Under ideal conditions, the voltage across each capacitor should be Vdc/2; however, the non-zero average current flowing to the inverter's neutral point causes one capacitor to overcharge, while the other discharges [26]. This imbalance causes errors in DTC torque and flux estimation by distorting the amplitudes of the output voltage vectors, increasing the voltage stress on the semiconductors, and generating low-order harmonics in the output current [27]. The T-type inverter topology is illustrated in Fig. 3.

The methods developed to solve this problem are integrated into the switching table logic of the DTC. The redundant state selection method is the most common approach. In this method, when the DTC algorithm selects a "small vector" based on torque and flux error, it applies the switching combination that will provide balance considering the instantaneous voltage difference of the DC bus capacitors and the direction of the phase current [28]. For example, the authors in [16] demonstrated that they successfully balanced the NP voltage using redundant small vectors in a twelve-sector DTC structure. A similar approach applies to T-type inverters; the authors in [25] optimized efficiency while

controlling the NP potential in a T-type structure using a modified modulation technique. Furthermore, the use of virtual space vectors allows the creation of a synthetic vector that cancels the neutral current by combining three vectors in specific ratios to eliminate low-frequency fluctuations caused by medium vectors [29].

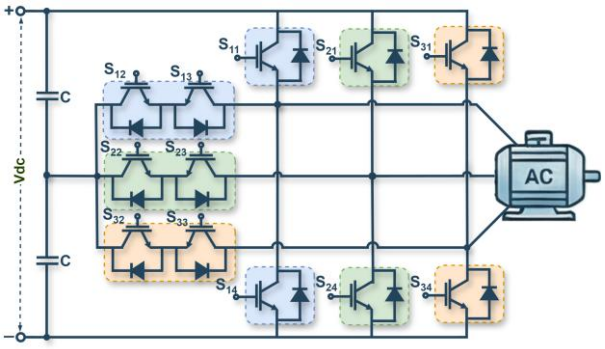


Fig. 3. Three-level T-type neutral point clamped inverter configuration.

### B. Flying Capacitor Inverters

The flying capacitor (FC) inverter topology uses series-connected "floating" capacitors integrated into the phase legs to provide multilevel voltage synthesis. This structure eliminates the clamping diodes in the NPC topology while offering a modular architecture that increases system reliability and fault tolerance [6]. The most critical feature of the FC topology for DTC applications is that it has multiple switching combinations (redundant switching states) that can produce the same output voltage level. This redundancy not only allows the DTC algorithm to control the electromagnetic torque and stator flux, but also provides an additional degree of freedom that enables the charging or discharging of flying capacitors depending on the selected switching state and the direction of the phase current [30], [31]. The flying capacitor inverter topology is shown in Fig. 4.

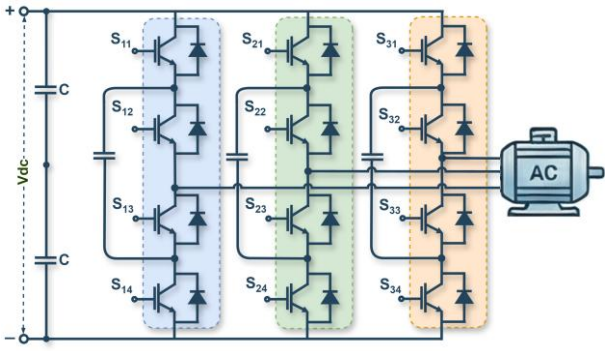


Fig. 4. Circuit diagram of three-phase, three-level flying capacitor (FC) inverter topology.

Balancing capacitor voltages in FC inverters is critical for system stability and the quality of the generated voltage THD. Although modulation techniques, such as phase-shifted pulse-width modulation (PS-PWM), are known to provide "natural balancing" in the literature, this process is slow and may be insufficient during dynamic torque changes [32], [33]. In methods requiring a fast dynamic response, such as DTC, "active balancing" is mandatory. In classic DTC schemes, this is achieved by expanding the look-up tables to select the appropriate backup switching state based on the sign of the capacitor voltage error [34]. However, in recent studies, model predictive control (MPC)-based DTC approaches have emerged as alternatives to these complex logical selections. For example, in [35], optimized capacitor voltages, torque, and current within a single cost function were developed in a predictive torque control (PTC) scheme for a four-level FC inverter. This approach succeeded in reducing torque fluctuations by 17.9 % compared to classical methods while maintaining capacitor voltages at their nominal values.

The effect of capacitor voltage balancing dynamics on the DTC is bidirectional. A well-balanced FC system provides a high bandwidth and low dv/dt stress in torque and flux controls; however, in the event of an imbalance, the output voltage levels are disrupted, resulting in low-frequency harmonics in motor currents and increased torque ripple [27], [36]. In particular, maintaining the capacitor charge balance is difficult at low speeds and during motor startup, which can lead to disturbances in the stator flux trajectory. To overcome this problem, a strategy was proposed to reduce computational load using a sequential predictive current control method while maintaining capacitor balance and reducing CMV in [37]. Therefore, the success of an FC-based DTC drive is directly dependent on the speed and accuracy with which the capacitor balancing algorithm operates compared to the mechanical time constants of the motor.

### C. Cascade H-Bridge

CHB converters have a modular structure created by connecting identical H-bridge cells in series, utilizing low-voltage power semiconductors, thereby enabling safe access to medium- and high-voltage levels [5], [6]. The most distinctive feature of this topology is that each H-bridge cell requires independent and electrically isolated DC power sources. In industrial induction motor drives, this requirement is typically met using phase-shifting multi winding transformers, which minimize harmonics on the grid side (e.g., with 36-pulse or 54-pulse rectifiers) while creating an isolated DC bus for each cell [38]. In EV applications, the fact that the battery pack naturally consists of multiple cells transforms the isolated source requirement of the CHB topology from a disadvantage into an advantage that can be integrated with the battery management system (BMS) and provides fault tolerance [39], [40]. The CHB inverter topology is illustrated in Fig. 5.

The integration of the CHB topology with the DTC method offers superior precision in torque and flux control, particularly due to the significant increase in the number of voltage vectors generated. For example, a 7-level CHB converter can provide hundreds of active vector combinations compared to the eight voltage vectors offered by a classic two-level converter, allowing the DTC algorithm to take much smaller and more precise voltage steps within the hysteresis bands [41]. However, this increases the complexity of the look-up tables that enable the selection of the optimal vector. To overcome this challenge, in [42], an ANN-based DTC scheme was developed for CHB-fed systems instead of a classical look-up table, and it was demonstrated that this method minimizes torque ripple by learning the complex switching logic. Furthermore, the modularity of the CHB structure allows for fault-tolerant operation by bypassing a cell when a fault occurs in that cell, thereby enabling the

driver to continue operating. This feature, combined with the fast dynamic response of DTC, provides high reliability for critical industrial processes [43].

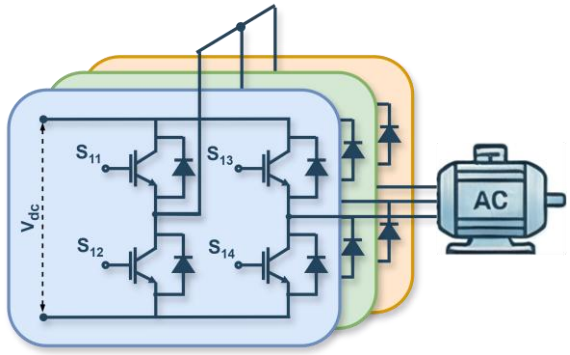


Fig. 5. Three-phase, three-level cascaded H-bridge (CHB) inverter topology.

Another critical factor affecting the performance of CHB inverters in DTC applications is the ripple in isolated DC bus voltages. The authors in [44] analyzed the direct effect of the DC bus capacitor value on the rectifier output and the resulting voltage ripple on motor torque ripple and speed stability in induction motors driven by a 5-level CHB. The study revealed that while the DTC algorithm is robust against changes in DC bus voltage, excessive ripple distorts the stator flux trajectory and reduces performance at low speeds. Additionally, the CHB topology offers flexibility in reducing CMV owing to the presence of isolated sources; motor bearing currents and EMI issues can be suppressed at the source with appropriate switching strategies [45]. Consequently, CHB-based DTC drives strike a balance between hardware cost (transformer or multiple-source requirements) and performance (low THD, high efficiency, and modularity), making them a dominant technology, particularly in high-power IM applications.

## IV. Next-Generation and Reduced Switch Count Topologies

In the industrial automation and EV sectors, component optimization in inverter topologies has become a critical design parameter for achieving power density and efficiency targets. In traditional MLI structures (particularly CHB and NPC), increasing the number of voltage levels at the output voltage results in a quadratic or linear increase in the number of switches; this requires complex PWM techniques, expanded cooling volumes, and increased costs [46], [47]. Developed to overcome this bottleneck, RSC topologies aim to produce higher-quality (higher-level) output voltages with fewer active switches by utilizing hybrid modules and smart switching matrices. These new generation structures not only reduce hardware costs but also increase system reliability and provide a more compact hardware infrastructure for advanced control methods, such as DTC [48].

### *A. Reduced-Switch Count MLI Structures*

The fundamental philosophy of a reduced-switch topology is to minimize the number of switches in the current path by using series-parallel conversions or "cross-switched" techniques in voltage-level conversion. This approach reduces transmission losses while improving the harmonic spectrum. For example, in [49], a 17-level output voltage with a minimum number of switches was achieved in a newly developed high-efficiency MLI topology using an asymmetric source configuration and an optimized switching matrix. The authors demonstrated through simulation and experimental studies that this structure improved power quality and reduced switching losses compared to classical topologies. Similarly, in [50], a five-level inverter design was developed, demonstrating how a reduced number of switches increased power conversion efficiency; the authors particularly emphasized the cost-effectiveness of these structures in medium-voltage applications. Furthermore, in [51], a new nine-level inverter composed of cascade modules was proposed for water pumping systems, and it was demonstrated that this structure reduced the number of devices compared to traditional topologies while decreasing the voltage stress on the motor owing to its high-level output.

In the case of IM drives, RSC topologies play a strategic role in improving DTC performance. The authors in [52] proposed a new MLI topology with a reduced number of switches for IMs and integrated this structure with the DTC technique. The authors reported that the proposed topology significantly reduced torque ripple and decreased motor THD, despite using fewer components than the classic NPC structure. For low-power ranges, the author in [9] designed a low-cost DTC driver using a four-switch inverter instead of a classic six-switch structure; it was demonstrated that this structure provides sufficient dynamic performance in cost-sensitive applications (e.g., household appliances or small pumps). Additionally, the authors in [53] increased the efficiency of an IM and minimized the THD of the system in solar-powered water pumping systems by using a 17-level reduced-switch symmetric MLI topology.

### *B. Asymmetric Inverters*

One of the most effective ways to maximize the number of levels is to use different magnitudes of DC source voltages at the inverter input (asymmetrical). In a symmetric structure, N sources yield 2N + 1 levels; when the source voltages are selected in a binary (binary - Vdc, 2Vdc, 4Vdc) or ternary (trinary - Vdc, 3Vdc, 9Vdc) series, the number of levels increases exponentially [54]. The authors in [55] proposed a new method to calculate DC sources in extended multilevel converters and mathematically modelled that asymmetric structures produce voltage waveforms with a much higher resolution than symmetric structures with the same number of switches. This high resolution enables the narrowing of the hysteresis bands used in the DTC and increases the torque control accuracy. The three-phase asymmetrical inverter topology is illustrated in Fig. 6.

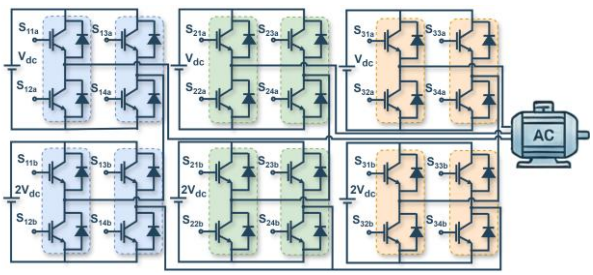


Fig. 6. Circuit diagram and phase modules of an asymmetric cascade H-bridge (ACHB) inverter.

On the application side, the authors in [54] designed an

asymmetric MLI with reduced components and low voltage stress, achieving a 21-level output and validating the use of this structure in solar energy systems. For motor drivers, the authors in [56] in an IM driver powered by a five-level asymmetric inverter used a fractional-order PID controller and the Meerkat optimization algorithm to successfully reduce both total harmonic distortion and common-mode voltage simultaneously. Asymmetric structures offer a natural advantage in the management of electric vehicle battery packs, in which battery cells can have different states of charge, and in motor driving [8].

### *C. Switched-Capacitor Structures*

The requirement for traditional MLIs to have multiple isolated DC sources is a major limitation, especially in applications where only a single DC source is available (e.g., an EV battery or a single PV array). Switched-capacitor (SC) topologies are innovative structures that can boost the DC bus voltage by switching capacitors in series/parallel and exhibit a "self-balancing" feature for capacitor voltages. These topologies can provide the high voltage required by the motor from a single low-voltage source without the need for an additional DC-DC boost converter.

The authors in [57] proposed a new three-phase, switched-capacitor-based, common-ground MLI topology for electric vehicle applications. This structure minimizes leakage currents while maintaining a capacitor charge balance without using any sensors. Similarly, the authors in [58] developed a self-balancing SC inverter with 17 levels and quadruple boost capability, thereby minimizing the number of components while maximizing the voltage gain. The authors in [59] proposed a nine-level active NPC (ANPC) boost-type inverter with reduced component stress, emphasizing that this structure increases reliability in industrial drives. For open-ended winding motor drives, the authors in [60] combined SC-based structures with model predictive torque control (MPTC) using synthetic voltage vectors, minimizing flux and torque ripple. The authors in [61] analyzed the capacitor balancing capabilities of nine- and 13-level advanced SC inverters and demonstrated that voltage stability is maintained during dynamic load changes (e.g., motor acceleration).

## V. MATRIX CONVERTER TOPOLOGIES

For aviation and modern EV applications, where power density is critical, topologies that eliminate energy storage elements, also known as "all-silicon solutions", combined with DTC's fast dynamic structure maximize the system's power density. Additionally, structures that increase the voltage level by changing the motor winding configuration are emerging as a powerful alternative in the literature.

### *A. Matrix Converters (MC)*

Matrix converters are a series of bidirectional switch structures that directly convert the input AC voltage into the desired amplitude and frequency of the output AC voltage, allow bidirectional power flow, and do not contain a DC bus capacitor. The elimination of bulky passive components (large capacitors and choke coils) enables matrix converter (MC)-based drives to achieve approximately 30 % volume savings compared to conventional methods and increase system reliability. Furthermore, sinusoidal input/output currents, unity input power factor, and natural regenerative braking capability make this topology attractive for IM drives. The main challenge in integrating MC with DTC is that classical DTC requires a fixed DC voltage source [62]–[65].

To overcome this challenge, the indirect matrix converter (IMC) structure has been introduced in the literature. The IMC separates the topology into virtual rectifier and virtual inverter stages, thus creating a "virtual DC bus" for the DTC.

The authors in [66] describe this approach, first theorized in [67] and topologically developed in [68], in which the matrix converter control algorithm is virtually divided into two stages:

1. A virtual rectifier r" stage that maintains sinusoidal grid currents;
2. A virtual inverter r" stage that supplies the motor [69].

Although there is no physical DC capacitor, the control algorithm defines a virtual VPN voltage by forming a positive envelope from instantaneous input line voltages [70]. Thus, a classic VSI-based DTC can be operated through this virtual voltage as if it were a fixed DC bus. A DTC based on an SVM and fuzzy logic was developed for IMC-fed IM drives, demonstrating that this structure can dampen torque fluctuations without a DC bus capacitor. The three-phase direct matrix converter topology is shown in Fig. 7.

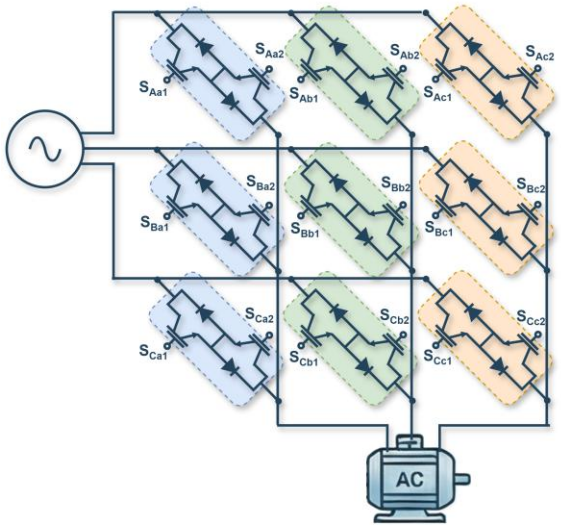


Fig. 7. Direct matrix converter (DMC) configuration based on a bidirectional switch matrix.

Furthermore, the authors in [71] proposed a model-predictive DTC for three-phase-to-five-phase direct matrix converters and demonstrated that it reduced the common-mode voltage while maintaining the input power factor at unity.

To overcome another limitation of matrix converters, namely, exceeding the maximum voltage transfer ratio (0.866), the author in [72] proposed a DTC modification using rotating vectors and theoretically demonstrated that this could extend the linear modulation region. The three-phase indirect matrix converter topology is shown in Fig. 8.

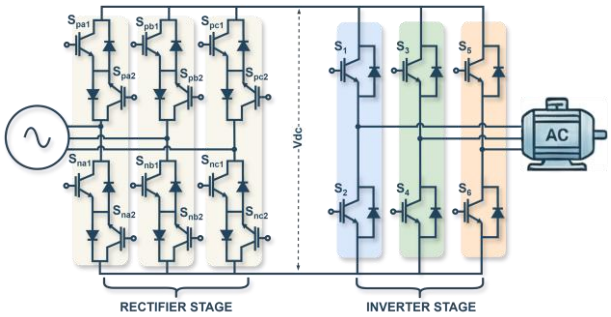


Fig. 8. Circuit configuration of an indirect matrix converter (IMC) with a cascaded structure.

### *A. Dual Inverter Open-Ended Winding (OEW) Structures*

In high-power induction motor drives, another approach that provides hardware flexibility is to open the star point of the motor (open-end winding) and supply both winding ends with two separate standard inverters, rather than using a single multilevel inverter [73], [74]. This topology increases the effective voltage applied to the motor windings (voltage boosting), thereby enabling the motor to reach its nominal speed and torque values with a lower DC bus voltage. In this structure, a three-level voltage characteristic can be obtained on the motor windings using two standard two-level inverters, which enables the motor to reach its nominal speed with lower DC bus voltages by providing "effective voltage boosting" [75].

Integration of the OEW structure with the DTC increases the number of voltage vectors that can be generated in the space vector plane in proportion to the number of levels of the inverters used. For example, when two two-level inverters are used, the characteristics of a three-level inverter are obtained at the winding terminals, and the harmonic content decreases significantly [33]. In [42], an improved duty cycle DTC algorithm supported by artificial neural networks (ANN) was proposed for open-wound induction motors. This study demonstrated that the complex switching combinations introduced by the dual-inverter structure were optimized using ANN, thereby minimizing the torque error. Similarly, the authors in [76] presented a dual-inverter control strategy for electric vehicle applications and reported that this structure increased motor performance by utilizing the battery voltage more efficiently.

One of the most critical issues in dual-inverter systems is the use of isolated DC sources or zero-sequence currents that arise when a single source is used. The authors in [75] proposed a seven-level hybrid dual-inverter scheme that reduced the number of switches while increasing the linear modulation range and mitigated this problem through asymmetric source usage. Additionally, the authors in [77] presented a multilevel solution that minimized the number of components in six-phase or dual-motor systems by using a dual-output nine-switch converter topology.

## VI. COMPARATIVE ANALYSIS OF TOPOLOGIES

Selecting the most suitable inverter topology for industrial IM drives is typically a multidimensional optimization problem that involves power quality, system cost, efficiency, and control complexity. Although traditional 2L-VSI remains the most cost-effective option due to its low component count and the simplest DTC, it remains the most cost-effective option. However, it is inadequate for medium- and high-power applications due to high dv/dt stress and limited harmonic performance. In contrast, three-level NPC and FC topologies significantly reduce motor current harmonics and increase efficiency, despite an increased number of switches and passive component requirements; however, this necessitates increasing the number of sectors in the DTC to 12 or more and complicates the look-up tables. A detailed comparison of the topologies is presented in Table I.

The power electronics industry is undergoing a new phase of transformation driven by revolutionary innovations in materials science and the digitalization brought about by Industry 4.0. In this context, the remainder of this section outlines three key trends that will shape the future of IM drives.

Current literature suggests that the disruptive impact of wide-bandgap (WBG) semiconductors is reshaping topology selection, enabling fault-tolerant architectures essential for autonomous systems, and facilitating the development of integrated motor drivers that maximize power density.

The switching speed and thermal limits of traditional silicon (Si) IGBTs are the primary bottlenecks that limit the sampling frequency and control bandwidth in DTC applications. The commercial maturity of silicon carbide (SiC) and gallium nitride (GaN)-based devices necessitates a paradigm shift in inverter topologies. SiC MOSFETs and GaN HEMTs allow for switching frequencies 10 times higher (100 kHz+) and higher operating temperatures than their Si counterparts, thereby reducing the size of passive filter elements and increasing the power density of the system.

However, the ultra-fast voltage changes rates (dv/dt) provided by WBG devices threaten motor winding insulation and increase bearing currents. This creates an interesting dilemma in topology selection: while it is possible to achieve high efficiency with a classic two-level inverter using SiC, three-level topologies are becoming more attractive for managing dv/dt stress.

TABLE I. COMPARISON OF INVERTER TOPOLOGIES USED IN DIRECT TORQUE CONTROL.

| Topology | Level Classification | Total Number of Active Keys | THD Performance | Torque Ripple Reduction | Efficiency Metrics | Application Complexity | References |
|---|---|---|---|---|---|---|---|
| Neutral Point Clamped (NPC) | Multilevel (3, 4, 5, 6, 7, 11-level) | A three-level structure requires four active switches per phase (12 in total); a five-level structure requires a total of 24 switches. | Low harmonic distortion; levels typically range from 1.35 % to 14.25 % depending on the control strategy. | The use of SVM in conjunction with a three-level NPC inverter resulted in a clear improvement of 62.4 % to 66.8 % in torque ripple compared to traditional systems. | Very high efficiency values ranging from 98.2 % to 99.4 % have been achieved using SiC MOSFETs and active NPC (ANPC) structures. | High; requires clamping diodes and complex capacitor voltage-balancing algorithms to prevent the neutral point potential shift. | [2], [15], [16], [17], [69], [78], [79], [80], [81], [82], [83] |

| Topology | Level Classification | Total Number of Active Keys | THD Performance | Torque Ripple Reduction | Efficiency Metrics | Application Complexity | References |
|---|---|---|---|---|---|---|---|
| Cascaded H-Bridge (CHB) | Multilevel (Scalable from 5 to 121-level) | It depends on the number of levels; a five-level, three-phase system requires 24 switches, while an 11-level system requires 20 switches per phase. | Very low (between 0.73 % and 4.61 %); as the number of levels increases (e.g., 23 levels), THD drops to levels between 2.0 % and 3.5 %. | As the number of levels increases in the CHB architecture and with filter capacitor optimization 65 % - 75 % reduction. | High; efficiency values ranging from 92 % to 98.3 % have been reported with low switching losses. | High component count and multiple independent isolated DC sources or transformers are required for a high, modular, and scalable structure. | [41], [44], [46], [50], [53], [78], [81], [84], [85], [86] |
| Flying Capacitor (FC) | Multilevel (3, 4, 5, 7, 9, 10-level) | A three-level, three-phase system requires 12 switches and three capacitors; a five-level configuration requires a total of 24 switches. | Between 1.35 % and 15.0 %; the lowest distortion level of 1.6 % was achieved in a nine-level interleaved structure. | The use of an MPC system has resulted in a clear 7.7 %–10.85 % improvement in torque ripple compared to traditional predictive methods. | Efficiency values ranging from 95 % to 98.6 % have been reported, depending on the number of layers and the GaN-based structure. | High; requires a large number of bulky capacitors and a complex control for real-time voltage balancing and precharging. | [6], [78], [81], [87], [88], [89], [90], [91] |
| Asymmetric | Multilevel (Asymmetric ratios, 5 to 169-level). | 12 keys are sufficient for a 25-level output, and 10–12 keys are sufficient for a 31-level output. | Very good (between 0.04 % and 14.25 %); THD levels of 4.8 % were achieved in a 25-stage SCMLI configuration and 0.11 % in a 169-stage cascade configuration. | The use of MFPCC and DTC has resulted in an improvement of more than 60 %–70 % in torque ripple. | High efficiency ranging from 93.99 % to 99.0 %; transmission losses have been minimized through a reduced number of switches. | Moderate to very high; requires unequal DC source magnitudes (binary/trinary) and complex source management algorithms. | [46], [84], [92], [93], [94], [95], [96] |
| Direct Matrix Converter (DMC) | Single-stage/ Multilevel equivalents | It requires nine bidirectional switches (for a total of 18 active IGBTs/MOSFETs) for a 3×3 matrix configuration. | Medium (between 1.35 % and 15.0 %); with the use of a filter, the THD values of the input current can be reduced to below 5 %. | Torque ripple has been reduced by 40 % to 60 % using Model-Free Predictive Control (MFPC) and DTC. | High (95 %–98 %); compact and efficient due to the absence of a DC bus capacitor; system volume has been reduced by 30 % to 50 %. | Very high; requires bidirectional switches (e.g., nine for a three-phase) and complex commutation strategies to avoid short circuits. | [62], [63], [64], [69], [97], [98], [99] |
| Indirect Matrix Converter (IMC) | Dual-stage (Virtual DC-link) | The standard configuration uses 18 active keys, the sparse model uses 15, and the ultra-sparse model uses 9–12. | 1.35 % to 10.5 %; Output THD levels can be maintained below 5 % in compliance with IEEE standards using SVPWM techniques. | With FL-DTC and PCC, torque ripple has been reduced by 43 % to 67.75 % compared to conventional inverters. | High (95 %–98 %); low losses are achieved by eliminating the intermediate-circuit capacitor. | High; separates the rectifier and inverter stages, allowing standard six-pack modules, but requiring synchronized control. | [60], [62], [63], [66], [70], [99] |

The authors in [100] proposed a GaN-based three-level active NPC (3L-ANPC) topology for the 800 V DC bus voltage in electric vehicle traction systems; they demonstrated that this structure reduces voltage stress on the motor and eliminates the need for filtering compared to two-level SiC solutions.

Furthermore, hybrid topologies are emerging for cost optimization. The authors in [101] proposed a hybrid structure for a three-level ANPC inverter, using GaN or SiC for high-frequency switched internal switches and inexpensive Si-IGBT for low-frequency switched external switches, reporting that this combination achieved over 99 % efficiency. Therefore, the future trend is shifting towards topological hybridization that balances cost and performance, rather than "all-SiC" solutions.

The ultimate limit to reducing the volume and weight of IM drives is reached with "integrated drives" (IMD) or "integrated modular motor drives" (IMMD), where the motor and inverter are physically combined into a single housing [102]. Eliminating the long, braided motor cables found in traditional systems solves EMI problems at the source and enables the use of common cooling systems.

The biggest obstacle to this integration is the negative impact of high temperatures and vibrations generated by the motor on power electronics. However, the development of high-temperature-resistant WBG; SiC/GaN devices and the use of low-profile matrix or ceramic capacitor DC-link topologies have overcome these obstacles. The authors in [103] examined integrated driver designs for electric vehicles and noted that immersed motor method drive structures, in which the motor windings have a segmented structure and each segment is driven by a small, modular GaN inverter, increase torque density. When combined with the multi-phase and modular control capabilities of DTC, these structures offer both high fault tolerance and unparalleled power density. A comprehensive comparison of the evaluated inverter topologies is presented in Fig. 9, highlighting the trade-offs between performance and complexity.

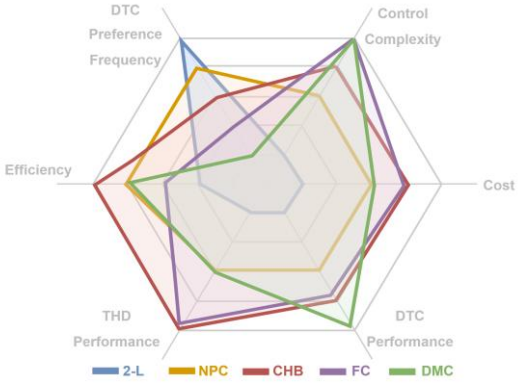


Fig. 9. Comparison of inverter topologies.

## VII. EMERGING INVERTER TOPOLOGIES AND ADVANCED CONTROL STRATEGIES

Traditional VSI and conventional DTC algorithms, which have been studied to date in high-performance drive systems for induction motors, may be inadequate in recent industrial applications that demand strict efficiency and power quality standards. On the hardware front, the commercial maturity of WBG semiconductors such as SiC and GaN has made reduced switch count asymmetric MLI and, in particular, current-source inverters (CSI) into attractive alternatives once again for induction motor drive systems [104], [105]. These next-generation WBG-based topologies reduce the system's size while operating at high frequencies, mitigate dangerous dv/dt stress and bearing currents at motor terminals, and minimize EMI by providing sinusoidal output [106].

However, fully harnessing the immense potential of these advanced hardware architectures depends on overcoming the drawbacks associated with conventional DTC, such as high torque ripple and variable switching frequencies. In this context, the field of control engineering is increasingly adopting artificial intelligence and prediction-based intelligent control strategies such as sliding mode control (SMC), FL, ANN, and finite control set model predictive control (FCS-MPC) [107]–[109]. Advanced control algorithms process the increased voltage vector diversity provided by next-generation inverters with the highest resolution, thus tolerating uncertainties in motor parameters, dynamically eliminating torque and flux fluctuations, and, when combined with sensorless techniques such as model reference adaptive systems, maximizing the system's fault tolerance and reliability.

### *A. Emerging Inverter Topologies*

Fully unlocking the dynamic performance potential of DTC is possible only when these control algorithms are supported by modern hardware architectures. This section focuses on modern power electronics architectures and emerging inverter topologies, going beyond classic two-level (2L-VSI) structures.

*Reduced-Device-Count Multilevel Inverters:* MLIs directly enhance the performance of DTCs by offering lower THD compared to conventional two-level inverters in induction motor drives and by reducing motor insulation stress. However, in standard NPC or CHB configurations, as the target output voltage level increases, the number of power switches and isolated DC power supplies increases exponentially, thus increasing system costs and control complexity [106]. To reduce the high cost associated with a large number of switches in these standard structures, reduced-device-count (RDC) MLI topologies have gained prominence in the literature. These next-generation topologies can generate output voltages of 7, 9, 11, and even higher levels while using significantly fewer semiconductors, owing to asymmetric resource utilization and cross-connected module designs [93], [110]. The use of RDC-MLI structures to control induction motors via DTC naturally dampens high dv/dt ratios, which trigger motor insulation stress, by providing low THD values, thus extending the motor's electrical lifespan without increasing hardware complexity.

*Impedance-Source and Quasi-Z-Source Inverters - qZSI*: Another fundamental hardware limitation encountered in motor drive systems is that conventional VSI configurations can operate only as buck converters, and a short circuit (shoot-through) involving switches on the same leg can destroy the system. Impedance-source and, in particular, quasi-Z-source inverters (qZSI), developed to overcome this physical limitation, can provide the capability for single-stage voltage boost by safely allowing a "shoot-through" condition through their passive impedance network [111]. These topologies provide the optimal voltage vectors required to satisfy the instantaneous torque demands of the motor in DTC drives, while eliminating the need for an additional DC-DC boost module. Additionally, qZSI configurations exhibit high immunity to DC-link voltage fluctuations because of the continuous current draw on the input side and reduced voltage stress on the capacitors. These features make them indispensable for induction motor drivers integrated with renewable energy sources, such as solar or wind, which have variable energy profiles.

*Wide Bandgap Based Inverters:* Achieving the targeted power density and efficiency in advanced inverter topologies has been made possible by replacing traditional silicon (Si)-based switches with WBG semiconductors such as SiC and GaN. WBG-based inverters can operate seamlessly at ultra-high switching frequencies (100 kHz and above) due to their high critical electric field strength, superior electron mobility, and thermal conductivity [104], [112]. In DTC drives for induction motors, this ultra-high-frequency operating capability dramatically reduces the size of the system's filtering components, coils, and cooling blocks, thus optimizing the overall physical footprint of the equipment [105]. Concurrently, due to the extremely low conduction and switching losses offered by GaN and SiC devices, modern inverter systems are achieving efficiency levels of up to 99 %, thus redefining the boundaries of modern power electronics in both industrial drives and aerospace and electric vehicle applications [28].

### *B. Advanced Control Strategies for Modern Induction Motor Drives*

To fully leverage the high-resolution and flexible voltage vectors offered by the RDC-MLI and WBG hardware architectures examined in the previous section, modern software-based intelligence that goes beyond the classical DTC algorithms is required [113]. In this context, advanced control strategies that fundamentally transform the dynamic performance and energy management of induction motor drives can be addressed as follows.

*Model Predictive Control (MPC)*: In parallel with hardware advancements in conventional drive systems, software-based MPC, and in particular, the FCS-MPC algorithms, offer a revolutionary approach to induction motor control [108]. Unlike traditional DTC and FOC methods, FCS-MPC predicts future behavior based on the discrete-time dynamic model of the motor and inverter without using any PWM and directly generates the optimal switching signal [114]. The greatest strength of this strategy lies in its ability to simultaneously optimize multi-variable constraints, such as electromagnetic torque, stator flux, switching losses, and current limits, through a single cost function [108]. Thus,

while providing an ultra-fast dynamic response, the system minimizes current and torque ripple by effectively evaluating complex switching states and increasing the voltage vectors offered by multilevel inverters [113].

*Sensorless Control and Observer Techniques:* Sensorless control techniques, which eliminate the need for mechanical speed and position sensors, have become an integral part of modern drives to enhance the reliability of advanced control algorithms in industrial settings, reduce hardware costs, and minimize the risk of failure in harsh environments [107]. The issue of sensitivity to changes in stator resistance, particularly at low speeds, in conventional DTC systems is addressed using advanced estimation algorithms, such as the MRAS, sliding mode observers (SMO), and the extended Kalman filter (EKF) [109]. While MRAS algorithms estimate speed and flux by comparing references and adaptive motor models, the EKF provides optimal stochastic filtering against non-deterministic noise, and the SMO offers high robustness against parameter changes. Precise monitoring of motor parameters at low speeds and estimation of rotor position using hybrid observer structures supported by high-frequency signal injection compensate for the system's thermal stress, thereby maximizing the controller's error tolerance [104].

*Artificial Intelligence and Machine Learning Integration:* The final step in maximizing the dynamic performance of an induction motor and creating seamless synergy with advanced MLI hardware is the integration of artificial intelligence and deplaning. In traditional DTC systems, hysteresis comparators and fixed switching tables, which cause high-torque fluctuations, have been replaced by intelligent controllers based on FL and ANN. While FL dynamically evaluates torque and flux errors using linguistic rules to make optimal decisions, the neural network learns the motor's nonlinear dynamics to select the optimal voltage vector with high precision and instantly compensates for changes in electrical parameters [109]. Furthermore, to ensure system continuity, machine learning algorithms, such as CNNs, are used to diagnose open-circuit and short-circuit faults in multilevel inverters and detect sensor failures, thereby enabling predictive maintenance based on real-time data and ensuring the system's overall reliability [47]. To provide a comprehensive overview, the performance trade-offs and quantitative characteristics of next-generation inverter topologies are summarized in Table II. This comparison highlights the shift from traditional two-level structures to more complex, high-efficiency architectures.

TABLE II. PERFORMANCE TRADE-OFFS AND QUANTITATIVE ANALYSIS OF NEXT-GENERATION INVERTERS.

| Inverter Topology | Estimated System Efficiency (%) | Active Component Volume Savings | (THD) Levels | Complexity of Capacitor Balancing | Electromagnetic Interference (EMI) and dv/dt Stress | Industrial Investment Cost | References |
|---|---|---|---|---|---|---|---|
| Classic Two-Stage VSI | 90 %–98.5 % (lower with standard Si-IGBTs, higher with SiC-VFDs) | 0 % (reference baseline, no design savings) | 35 %–80.17 % (without filter); 4.52 %–9.52 % (with PWM/filter) | Low (no complexity, single DC-link capacitor) | Highest (sharp switching transitions, dv/dt stress exceeding 10 V/ns, and high EMI) | Lowest (cost-effective due to standard silicone components and simple construction) | [45], [104], [105], [110], [112], [115], [116], [117], [118], [119], [120] |
| Classic Multilevel H-Bridge (CHB-MLI) | 97 %–98.30 % (using low-voltage stress switches and fundamental frequency switching) | Low (requires a large number of isolated DC power supplies, drivers, and bulky transformers) | 2.80 %–4.92 % (may drop as low as 4.36% for 35-year terms) | Medium-High (separate isolated DC power supply and capacitor management for each cell/bridge) | Low (step-down type output and reduced common-mode voltage) | Moderate to Very High (varies depending on the number of components and isolated sources) | [47], [93], [105], [106], [110], [115], [121], [122], [123], [124], [125] |
| Wide Bandgap Current-Source Inverter (WBG-CSI) | 97.8 %–99 % (50 % reduction in switching losses with SiC/GaN) | 30 %–55 % reduction in volume and weight (by removing the DC-link capacitor) | 3 %–7.33 % (Low, sinusoidal output current) | None (uses inductive storage; no DC bus capacitor) | Low dv/dt and EMI (quasi-sinusoidal output); however, a specialized filter design may be required for high-speed switching | High (due to the cost of WBG semiconductors and monolithic bidirectional switches) | [47], [104], [105], [112], [115], [116], [117], [121] |
| RDC Asymmetric MLI | 94.87 %–96 % higher yield potential compared to VSI) | 40 %–70 % savings on switches, 62.22 % reduction in capacitors | 1.09%–8.37 % (depending on the number of levels and the filter) | Very High (due to asymmetric sources and complex switching sequences) | Very Low (minimal step and low dv/dt due to high voltage levels) | Low to Medium (fewer hardware components, but complex control software) | [93], [105], [106], [110], [115], [121], [122], [123], [126] |

As illustrated in Table II, the WBG-CSI demonstrated a superior efficiency profile, reaching up to 99 %, while simultaneously achieving a 30 %–55 % reduction in active component volume by eliminating bulky DC-link capacitors. This suggests that WBG-CSIs are highly suitable for high-power-density applications, in which spatial constraints are critical.

Regarding power quality, the RDC Asymmetric MLI topology exhibits the most promising harmonic performance, with THD levels dropping as low as 1.09 %. As shown in Table II, this topology significantly mitigates dv/dt stress and EMI compared to the classic two-stage VSI, which suffers from high switching transitions (>10 V/ns), potentially leading to premature motor insulation failure.

There is a critical trade-off between hardware simplicity and control intelligence. Although RDC Asymmetric MLIs offer substantial hardware savings (up to a 70 % reduction in switches), they impose a very high capacitor balancing complexity, as detailed in the table. Conversely, the classic VSI remains the most cost-effective solution for standard industrial investments, despite its lower efficiency and higher filter requirements.

## VIII. COMPARATIVE DISCUSSION: INDUSTRY 4.0 AND FUTURE TRENDS

When evaluated within the framework of Industry 4.0 standards, the capability for fault-tolerant operation has become one of the most critical research areas for modern induction motor drives. Although the increasing number of switches in multilevel inverters theoretically raises the likelihood of hardware failures, the integration of modern machine learning and deep learning algorithms, particularly convolutional neural networks (CNNs), into the system transforms this situation into a significant advantage [47].

Advanced AI algorithms and digital twin technologies can detect and isolate critical faults, such as open circuits or short circuits, within milliseconds by analyzing anomalies in sensor data in real time

Following this rapid detection, MLI topologies with redundant power cells and fault-tolerant control algorithms kick in, bypassing the faulty module and ensuring the motor continues to operate seamlessly without compromising its nominal speed and torque values.

Although a single switch failure in traditional drives causes the entire system to shut down, modern MLI-DTC systems equipped with intelligent diagnostics and reconfiguration algorithms eliminate the costs associated with unplanned downtime in industrial production lines.

Another critical area in which the synergy between hardware and software is reshaping industry standards is the reduction of EMI and common-mode voltage (CMV). The ultra-high switching frequencies and extremely high dv/dt rates (exceeding 10 V/s) offered by WBG semiconductors, such as SiC and GaN, cause insulation stress in the stator windings of traditional drivers [105], [117].

This situation causes discharge currents in the bearings of electric motors and leads to severe mechanical wear known as “fluting”.

The ability of multilevel inverters to naturally reduce the dv/dt stress by dividing the voltage steps, when combined with advanced software strategies, resolves these mechanical and electrical problems algorithmically.

Modified PWM techniques, such as active zero-pulse-width modulation (AZPWM) and near-zero-pulse-width modulation (NSPWM), based on “reduced common-mode voltage (RCMV)”, have been developed in the literature; these methods suppress CMV during the design phase without the need for bulky and costly passive filters.

Additionally, staggered switching strategies developed to minimize dangerous peak CM currents caused by very small duty cycles reduce motor bearing currents by up to 50 %, thereby extending motor life and facilitating compliance with electromagnetic emission standards [127].

## IX. CONCLUSIONS

This comprehensive study provides a systematic review of inverter topologies and control strategies specifically designed to reduce torque ripple, improve dynamic response, and increase energy efficiency in IM drives, revealing that there is no “single best” inverter structure in the literature, but rather a trade-off matrix determined by application requirements. Although traditional two-level inverters maintain their dominance in standard applications due to their low cost and control simplicity, they are insufficient for hardware-based solutions to the high torque ripple and variable switching frequency issues inherent in DTC. Classic multilevel topologies, such as the NPC and CHB, optimize motor performance at medium and high voltage levels by narrowing the torque and flux hysteresis bands due to the rich voltage vector space they offer. However, this performance increase comes at the cost of increased semiconductor count, more complex DC bus-balancing algorithms, and volumetric growth.

Analysis of power electronics trends for the next decade reveals that cost and reliability pressures are driving researchers toward RSC and “hybrid” topologies. Studies conducted between 2020 and 2026, in particular, have shown that asymmetric and switched-capacitor structures, which produce higher voltage levels (7, 9, 13 levels, etc.) using fewer active switches, are the strongest candidates to replace classical topologies. These new-generation topologies reduce hardware costs while providing the precise voltage vectors required by the DTC; however, this increases the complexity of the control algorithm. This complexity can be managed through the integration of artificial intelligence-based strategies, such as ANN and MPC. Furthermore, the proliferation of WBG semiconductors, such as SiC and GaN, increases the power density of DC-busless structures such as matrix converters, strengthening the applicability of DTC, especially in space-constrained applications such as electric vehicles and aviation.

Consequently, the future of IM DTC lies in integrated systems in which hardware-side reduced-component hybrid topologies and software-side AI-supported adaptive controllers work in a synchronized manner.

## CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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