Performance Analysis of a Secondary-Side Resonance 1 MHz GaN-based Active-Clamp Flyback DC-DC Converter in CCM

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***Abstract*—Traditional active-clamp flyback (ACF) DC-DC converters operate in discontinuous current mode (DCM) and continuous current mode (CCM). In high-frequency traditional CCM-ACF, zero-voltage switching (ZVS) of main switch is unrealised particularly under light load, necessitating complex control strategies to transition between CCM and DCM depending on the load. In contrast, the secondary-side resonance CCM-ACF topology alters the primary current waveform, affecting the energy stored in the leakage inductance when the active-clamp switch is off, simultaneously reducing the primary rms current, thereby lowering conduction losses and improving overall efficiency. This study presents a comparative performance analysis between high-frequency traditional and secondary-side resonance CCM-ACF. A 60 W 1 MHz gallium nitride (GaN)-based model of both topologies is simulated and analysed using MATLAB Simscape. The results indicate that the secondary-side resonance CCM-ACF achieves ZVS of main switch even under light load with a low output voltage ripple and a better transient response at low output voltage. Finally, a peak efficiency of 93.99 %, which marks a 0.56 % improvement compared to traditional topology, is achieved.**

***Index Terms*—Active-clamp flyback; Continuous current mode; DC-DC power converters; Gallium nitride; Secondary-side resonance.**

I. INTRODUCTION

DC-DC converters are widely used, covering a wide spectrum of applications from residential lighting, motor drives, renewable energy systems to electric vehicle industries [1]–[8]. One of the well-known topologies for DC-DC converters is the traditional flyback DC-DC converter. Despite its simple structure, it is well known for excessive switching stress due to resonance between the parasitic capacitances of semiconductor switches and transformer leakage inductance, which contributes to significant power losses [9]. Numerous enhanced topologies have been proposed to overcome the challenges. With the introduction of high-electron-mobility-transistor (HEMT) gallium nitride (GaN) transistors, flyback DC-DC converters can be achieved with high switching frequency and improved efficiency [10]–[13].

However, the high switching frequency with hard-switching increases switching losses, thus motivating the implementation of soft-switching flyback DC-DC converters. The two-switch DC-DC flyback converters could offer higher efficiency compared to traditional flyback, but come with a higher cost, where two power switches and two clamping diodes are required [14], [15]. On the other hand, active-clamp flyback (ACF) topology is effective for converters up to 100 W and is commonly used to achieve soft-switching at high switching frequencies [16], [17]. In ACF, the leakage inductance energy is absorbed by the clamp capacitor, which reduces the voltage overshoot when the main switch is turned off, lowering the voltage stress and switching losses of the main switch. The absorbed energy is then recycled, improving overall efficiency. A new switching method to achieve soft switching in ACF allows full recycling of leakage inductance energy [13]. With a switching frequency of 65 kHz, high efficiency is achieved under both heavy and light load conditions. In [11] and [16], MHz range GaN-based ACF was presented to analyse zero-voltage switching (ZVS) losses caused by inductor current drops during the switching transient, which is influenced by discharging of the capacitance of the secondary-side diode junction.

The traditional ACF can operate in discontinuous current mode (DCM) and continuous current mode (CCM). These

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modes are almost similar except that CCM requires a higher magnetising inductance. DCM experiences higher current stress, higher primary and secondary-side peak currents, resulting in higher conduction and switching loss [18], [19]. In CCM, the magnetising inductance current does not drop to zero, enabling continuous energy transfer, stable output voltage, and a smaller capacitor is sufficient to manage the output ripple [20]. The ZVS energy stored in the leakage inductance decreases with load; therefore, in a high-frequency CCM-ACF designs, the ZVS of the main switch becomes unrealisable, particularly at light load [21]. As a result, some ACF designs transition between CCM and DCM based on load.

In addition to DCM and CCM, the traditional ACF relies on the resonance between transformer leakage inductance and the primary-side clamp capacitor. This results in higher conduction loss due to increased primary rms current [11]–[13], [16], [17]. In secondary-side resonance ACF, leakage inductance resonates with both the clamp capacitor and the additional secondary-side resonance capacitor [21], [22]. The previously proposed secondary-side resonance ACF is implemented up to 600 kHz switching frequency with complex control due to the use of an active switch as the secondary-side rectifier. A MHz range secondary-side ACF was introduced as part of solar street-lighting LED drivers [23]. However, a comparative analysis of ZVS performance, output voltage ripple, transient response, and efficiency between traditional and secondary-side resonance CCM-ACF was not included.

Only a limited available study has been conducted on the MHz frequency of secondary-side resonance CCM-ACF converters. Therefore, their performance remains an ongoing topic of discussion. This manuscript presents a performance analysis of a GaN-based 1 MHz, 60 W secondary-side resonance CCM-ACF converter. A comparison with traditional CCM-ACF is simulated through the MATLAB Simscape environment. The focus of this manuscript is as follows.

– ZVS realisation of the main switch in high-frequency CCM-ACF particularly under light load.

– Comparison of switching stress, output voltage ripple, transient response, and efficiency between traditional vs. secondary-side resonance CCM-ACF.

To further explain this manuscript, the operating principle of traditional and secondary-side CCM-ACF is discussed in Section II and III, respectively. In Section IV, the design consideration of secondary-side CCM-ACF is presented and the results are discussed in Section V. Section VI concludes this manuscript.

II. TRADITIONAL CCM-ACF

The traditional CCM-ACF circuit scheme is shown in Fig. 1. On the primary side, the clamp capacitor C_{clamp} absorbs the leakage inductance energy to effectively reduce voltage overshoot when the main switch Q_1 is turned off. An RC snubber is installed on the secondary side to manage the voltage spike of the secondary-side rectifier diode D_1 during turn-off. The key waveforms of the high-frequency traditional CCM-ACF show that the magnetising inductance current i_{LM} does not fall to zero, indicating a CCM operation as seen in Fig. 2. V_{gs_Q1} and V_{gs_Q2} are the gate signals of main switch Q_1 and active-clamp switch Q_2, respectively. VC_{clamp} is the voltage across the clamp capacitor and V_{ds_Q1} is the voltage between drain and source of Q_1. i_{LM}, and i_{LK} are the magnetising and leakage inductance current, respectively. V_D is the voltage through D_1 and I_D is the current through D_1.

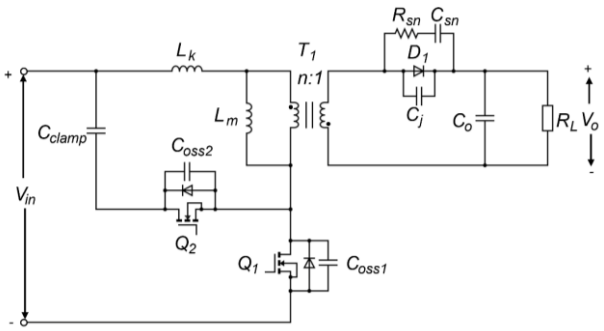


Fig. 1. Circuit scheme of traditional CCM-ACF with diode rectifier and snubber circuit on the secondary side.

In Fig. 1, V_{in} is the input voltage, V_o is the output voltage, Q_1 is the main switch, Q_2 is the active-clamp switch, L_k is the transformer leakage inductance, L_m is the transformer magnetising inductor, C_{clamp} is the clamp capacitor, C_{oss1}, C_{oss2} is the GaN's switches output capacitor, C_j is the rectifier diode junction capacitor, D_1 is the rectifier diode, R_{sn} is the secondary-side snubber resistor, C_{sn} is the secondary-side snubber capacitor, C_o is the output capacitor, and n is the transformer ratio.

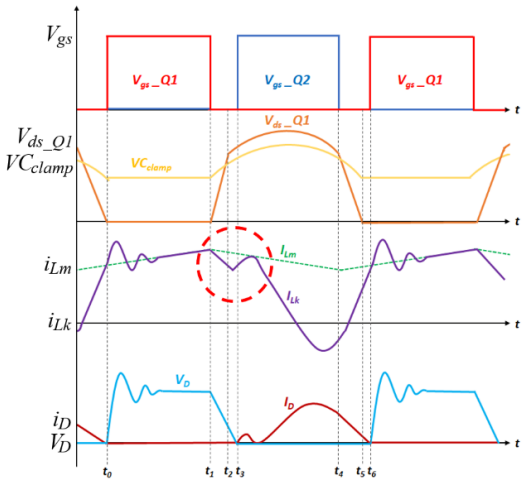


Fig. 2. Key waveforms of high-frequency traditional CCM-ACF.

– Mode 1 [t_0-t_1]

At $t = t_0$, Q_1 is turned ON and Q_2 is turned OFF. L_m and L_k are charged by V_{in} to store energy. As a result, i_{LM} and i_{Lk} increase linearly. D_1 is reverse biased; thus, the transformer is not conducting, and no energy is transferred from the primary- to the secondary-side of the transformer. The voltage across D_1 could spike and dampen by the snubber circuit on the secondary side. This mode ends at $t = t_1$, where Q_1 is turned OFF.

– Mode 2 [t_1-t_3]

In this interval, the dead time of [t_1-t_3] provides the condition for Q_2 to realise ZVS. When Q_1 is turned OFF at $t = t_1$, the primary current takes the path of the resonant circuit, which involves L_m, L_k, and C_{oss1}. C_{oss1} is charged from $0V$ to $V_{in} + nV_o$ by i_{Lk}, whilst C_{oss2} is discharged by i_{Lk}. Once C_{oss2} is fully discharged at $t = t_2$, the body diode of Q_2

conducts, causing zero voltage across Q_2. The ZVS of Q_2 could be realised if the gate signal arrives within [t_2-t_3]. Referring to Fig. 2, i_{Lk} experiences an immediate current drop after Q_1 off. This mode ends at t = t_3 where Q_2 is turned ON.

– Mode 3 [t_3-t_4]

At t = t_3, Q_2 and D_1 turned ON. The energy stored in L_m is transferred to the output and the leakage inductance L_k resonates with C_{clamp}. During this interval, i_{Lk} oscillates and could approach i_{LM} before moving towards its peak negative value, as depicted in Fig. 2. The oscillation occurs due to a small C_{clamp}. It causes irregular oscillation of the rectifier diode current I_D, thus could forcing a false trigger of D_1. This mode ends at t = t_4 where $Q2$ is turned OFF.

– Mode 4 [t_4-t_6]

In this interval, the dead time of [t_4-t_6] provides the condition for Q_1 to realise ZVS. When Q_2 is turned OFF at t = t_4, C_{oss2} is charged by i_{Lk} while C_{oss1} is discharged by i_{Lk}. In CCM, the magnetisation current i_{LM} is always positive, thus only the leakage inductance current i_{Lk} is used to release the output capacitor energy and to assist the ZVS of Q_1. Once C_{oss1} is fully discharged at t = t_5, the body diode of Q_1 conducts, resulting in zero voltage across Q_1. The ZVS of Q_1 can be realised if the gate signal arrives within t_5-t_6. This mode ends at t = t_6, where Q_1 is turned ON.

III. SECONDARY-SIDE RESONANCE CCM-ACF

The secondary-side resonance CCM-ACF circuit scheme is depicted in Fig. 3. The components are similar to those in traditional CCM-ACF; however, a small difference could be spotted where the secondary-side resonance capacitor C_{sr} and the output inductor L_o are the additional elements on the secondary side. Figure 4 depicts the key waveforms of high-frequency secondary-side resonance CCM-ACF. The magnetising inductance current i_{LM} does not fall to zero, indicating a CCM operation.

– Mode 1 [t_0-t_1]

In this interval, the operation is similar to Mode 1 of traditional CCM-ACF. This mode ends at t = t_1 where Q_1 is turned OFF.

– Mode 2 [t_1-t_3]

In this interval, the working principle is almost similar to that in traditional CCM-ACF. Referring to Figs. 2 and 4, it is observed in both topologies that i_{Lk} experiences an immediate current drop when Q_1 is off. The magnitude of the current drop is influenced by the total parasitic capacitance, which determines the initial condition of the resonance process, affecting the i_{Lk} rms value. The current drop during this interval is also similar if both topologies have similar parasitic capacitances.

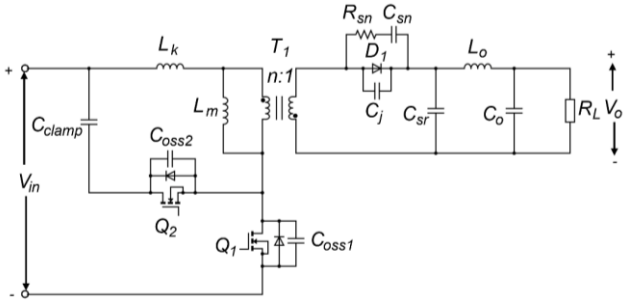


Fig. 3. Circuit scheme of secondary-side resonance CCM-ACF with diode rectifier, snubber circuit and secondary-side resonance capacitor.

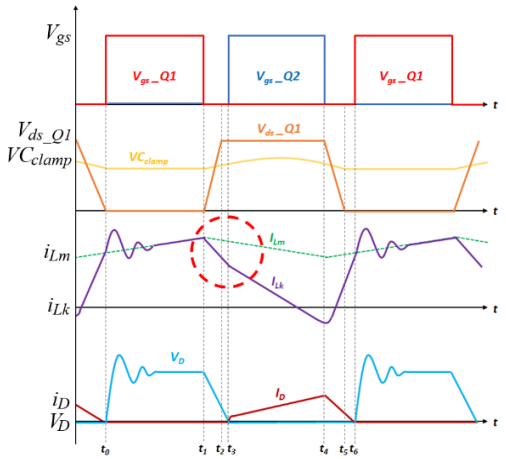


Fig. 4. Key waveforms of high-frequency secondary-side resonance CCM-ACF.

The mathematical equation during this interval is discussed in [21]. Suppose the interval [t_1-t_3] is short and L_m>>L_k, thus the average of magnetising current $i_{Lm.avg}$ is equal to

$$i_{Lm.avg} = \frac{P_o}{\eta V_{in}} + \frac{I_o}{n}, \tag{1}$$

where P_o is output power, η is converter's efficiency, I_o is the output current. The peak and valley values of I_{Lm} can be calculated as:

$$i_{Lm.max} = i_{Lm.avg} + \frac{V_{in} d}{2 f_s L_m}, \tag{2}$$

$$i_{Lm.min} = i_{Lm.avg} - \frac{V_{in} d}{2 f_s L_m}, \tag{3}$$

where d is the duty cycle and f_s is the switching frequency. This mode ends at t = t_3 where Q_2 is turned ON.

– Mode 3 [t_3-t_4]

At t = t_3, Q_2 and D_1 is turned ON. The energy stored in L_m is transferred to the output, and the leakage inductance L_k is resonating with C_{clamp} and C_{sr}, thus the resonance waveform is related to these components value. During this interval, the waveform between both topologies is different. In secondary-side resonance CCM-ACF, i_{Lk} is resonating away towards its peak negative value as depicted in the key waveform in Fig. 4. The simplified circuit during this interval is shown in Fig. 5, where L_o and L_m, which are the output inductor and magnetising inductor shown in Fig. 3, respectively, are represented as a constant current source I_o and a time-variation current source $i_{Lm}(t)$.

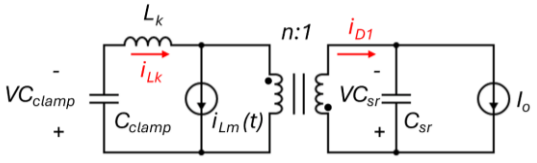


Fig. 5. Simplify circuit in Mode 3 [t_3-t_4].

If $i_{Lk.t3}$, $i_{Lm.max}$ are the current of the leakage inductance and the magnetising inductor, respectively, whilst $V_{Cclamp.t3}$ and $V_{Csr.t3}$ are the voltage across the clamp and the secondary-side resonance capacitor, respectively, during the starting point of the interval [t_3-t_4], the leakage inductance current can be

calculated [24]:

$$i_{Lm}(t) \cong i_{Lm.max} - \frac{nV_o}{L_m}t, \tag{4}$$

$$i_{Lk}(t) = \frac{n^2}{L_k C_{sr} \omega_r^2}\left(\alpha\ sin(\omega_r t) + \beta\ cos(\omega_r t) + \gamma(t)\right), \tag{5}$$

$$\alpha = \left(n.VC_{sr.t3} - VC_{clamp.t3}\right)\frac{C_{sr}\omega_r}{n^2} + \frac{nV_o}{L_m\omega_r}, \tag{6}$$

$$\beta = i_{Lk.t3}\frac{L_k C_{sr}\omega_r^2}{n^2} - i_{Lm.max} + \frac{I_o}{n^2}, \tag{7}$$

$$\gamma(t) = i_{Lm.max} - \frac{I_o}{n} - \frac{nV_o t}{L_m}, \tag{8}$$

$$\omega_r = \sqrt{\frac{1}{L_k C_{eq}}}. \tag{9}$$

The slope of (6) shows that if ($n.VC_{sr.t3}$) is larger than ($VC_{clamp.t3}$), $I_{Lk}(t)$ slope is positive, as traditional ACF current waveform, as shown in Fig. 2. If ($n.VC_{sr.t3}$) is smaller than ($VC_{clamp.t3}$), then $I_{Lk}(t)$ slope is negative, as the secondary-side resonance ACF, as shown in Fig. 4. $\boldsymbol{C_{eq}}$, which is the total equivalent capacitance during this interval, can be calculated as [21]

$$C_{eq} = \frac{C_{clamp}\left(C_{sr}/n^2\right)}{C_{clamp} + \left(C_{sr}/n^2\right)}. \tag{10}$$

This mode ends at t = t_4 where $\boldsymbol{Q_2}$ is turned OFF.

– Mode 4 [t_4-t_6]

Active-clamp switch $\boldsymbol{Q_2}$ is turned OFF at t = t_4. The simplified circuit during this interval is shown in Fig. 6 where $\boldsymbol{C_{sw}}$ is the total capacitance of the switching point, which includes $\boldsymbol{C_{oss1}}$, $\boldsymbol{C_{oss2}}$, $\boldsymbol{C_j}$, and all other parasitic capacitances. $\boldsymbol{C_{oss2}}$ is charged by $\boldsymbol{i_{Lk}}$, whilst $\boldsymbol{C_{oss1}}$ is discharged by $\boldsymbol{i_{Lk}}$. Due to the magnetisation current $\boldsymbol{i_{Lm}}$ being always positive, only the leakage inductance current $\boldsymbol{i_{Lk}}$ is used to release the output capacitor's energy and to realise the ZVS of $\boldsymbol{Q_1}$. Ideally, to achieve ZVS, the energy stored in the leakage inductance should be greater than the energy stored in the output capacitor of $\boldsymbol{Q_1}$

$$L_k i^2_{Lk.t4} > C_{oss1}\left(V_{in} + nV_o\right)^2. \tag{11}$$

Thus, the peak negative value of $\boldsymbol{i_{Lk}}$ when $\boldsymbol{Q_2}$ is turned off at t = t_4 is important as it could determine the ZVS of $\boldsymbol{Q_1}$, especially during light load, because it impacts the energy stored in the leakage inductance.

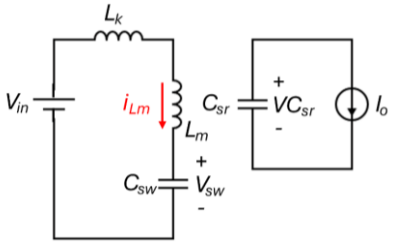


Fig. 6. Simplify circuit in Mode 4 [t_4-t_6].

Referring to [24],

$$i_{Lk.t4} = \frac{-V_{in} - VC_{clamp.t3}\ cos(\omega_z T_d)}{\sqrt{\frac{L_m + L_k}{C_{sw}}}sin(\omega_z T_d)}, \tag{12}$$

$$\omega_z = \frac{1}{\sqrt{(L_m + L_k)C_{sw}}}, \tag{13}$$

where $\boldsymbol{T_d}$ is the dead time duration of [t_4-t_6], which can be controlled by the controller. Once $\boldsymbol{C_{oss1}}$ is fully discharged at t = t_5, the body diode of $\boldsymbol{Q_1}$ conducts, causing zero voltage across $\boldsymbol{Q_1}$. The ZVS of $\boldsymbol{Q_1}$ could be realised if the gate signal arrives within t_5-t_6. Furthermore, the zero-current switching (ZCS) of $\boldsymbol{D_1}$ occurs when $\boldsymbol{i_{Lk}}$ touches $\boldsymbol{i_{Lm}}$ where the resonance between $\boldsymbol{L_k}$ and $\boldsymbol{C_{sr}}$ ends at t_6. This mode ends at t = t_6, where $\boldsymbol{Q_1}$ is turned ON.

The equivalent circuits corresponding to Mode 1 to 4 are as depicted in Fig. 7.

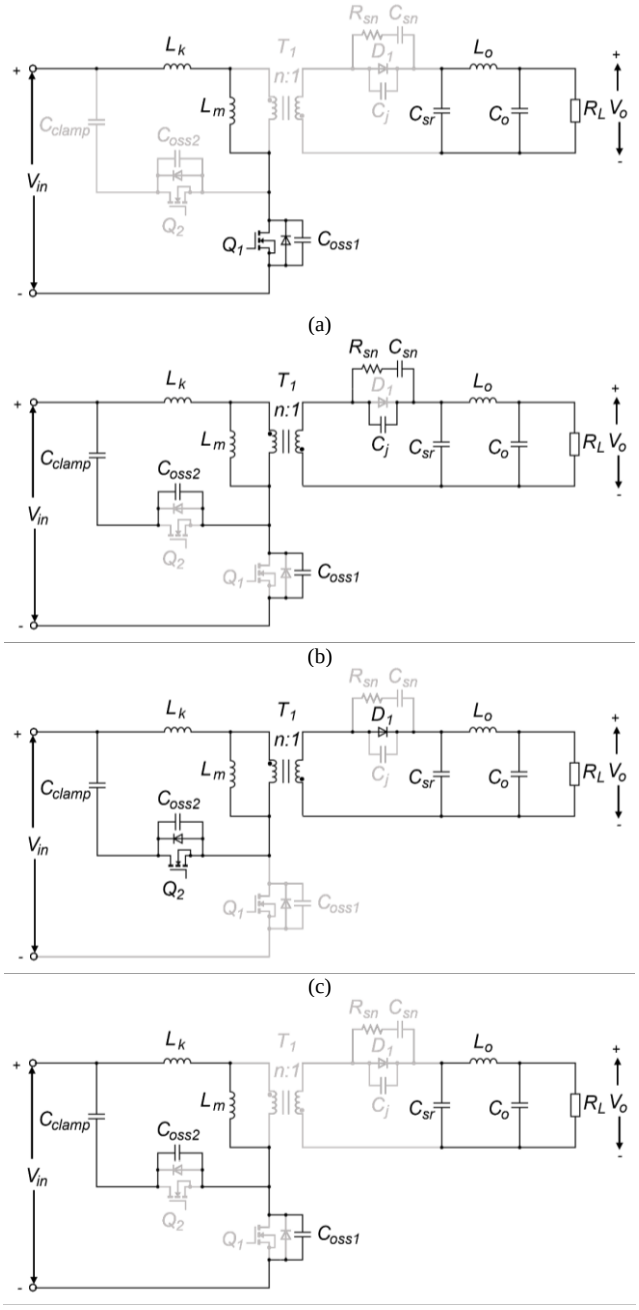


Fig. 7. Equivalent circuits of each operating mode: (a) Mode 1 [t_0-t_1]; (b) Mode 2 [t_1-t_3]; (c) Mode 3 [t_3-t_4]; (d) Mode 4 [t_4-t_6].

IV. DESIGN CONSIDERATIONS

A. Transformer Turn Ratio and Selected Duty Cycle

It is important to determine the minimum input voltage $V_{in(min)}$ and the maximum output power $P_{o(max)}$, as these define the worst operating conditions of the converter. Since there are similarities, the parameters of all components are designed based on the traditional CCM-ACF as shown in Fig. 1, and the requirements for secondary-side resonance are then added. The key to the CCM-ACF converter is the flyback transformer T_1. The transformer turn ratio n is determined based on [25]:

$$\frac{N_p}{N_s} = n = \frac{V_{in(min)}\ d_{max}}{\left[\left(V_o + V_D\right)\ \left(1 - d_{max}\right)\right]}, \tag{14}$$

$$d = \frac{n\ \left(V_o + V_D\right)}{V_{in} + \left[n\ \left(V_o + V_D\right)\right]}, \tag{15}$$

where $V_{in(min)}$ is the minimum input voltage, d_{max} is the maximum duty cycle, V_o is the output voltage, and V_D is the forward voltage of the secondary rectifier diode D_1. As seen in (15), the output voltage changes by regulating the duty cycle. A low duty cycle is unhealthy for the operation of the secondary-side rectifier diode D_1, whilst a high duty cycle will cause higher conduction loss. Therefore, an appropriate range of duty cycle and transformer turn ratio needs to be considered. In this manuscript, the transformer turn ratio n is selected as 2 and the operating duty cycle is limited between 0.2 and 0.5.

B. Primary and Secondary Inductance

The minimum value of the primary inductance is calculated on the basis of [25]

$$L_{p(min)} > \frac{{V_{in(min)}}^2\ {d_{max}}^2\ \eta}{2\ f_{sw}\ P_{o(min)}}, \tag{16}$$

where η is the estimated efficiency and $P_{o(min)}$ is generally 20 %–30 % of $P_{o(max)}$. Instead of a customisation, a flexible flyback transformer made by Wurth Electronics is selected in this manuscript. Through its flexibility features, the transformer winding arrangement can be varied to achieve the desired *turn ratio* n, the primary inductance L_P, and the secondary inductance L_S [26]. The selected winding arrangement with parallel connection on the secondary side, as shown in Fig. 8, could further reduce secondary voltage spikes [27].

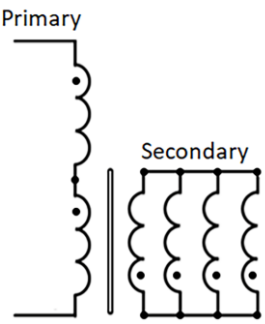


Fig. 8. Selected flyback transformer winding arrangement with parallel connection on the secondary side.

The primary peak current I_{P_peak}, when the minimum input voltage $V_{in(min)}$ supplied, is calculated based on [25]

$$I_{p\_peak} = \frac{I_{o(max)}}{\left(1 - d_{max}\right)\ n} + \frac{V_{in(min)}\ d_{max}}{2\,L_p\ f_{sw}}. \tag{17}$$

C. Clamp Capacitor

The current in the transformer does not circulate in the secondary and primary at the same time due to the imperfect coupling where leakage inductance exists. When the main switch Q_1 is turned off, the leakage inductance energy cannot be be transferred dirtectly to the secondary side and the only path for the leakage inductance current to circulate is through C_{Coss1}. This causes the drain-source voltage of the main switch V_{ds_Q1} to spike and oscillate, exposing the main switch to excessive switching stress and power dissipation. The maximum V_{ds_Q1} is calculated on the basis of [25]

$$V_{ds(max)} = V_{in(min)} + \left[n\left(V_o + V_D\right)\right]. \tag{18}$$

To reduce the effect of voltage spike and oscillation, a clamp capacitor C_{clamp} is added as it is able to store additional energy and recycle back to the source. The minimum clamp capacitor C_{clamp} can be calculated based on [28]

$$C_{clamp} > 10\ \frac{\left(1 - d_{min}\right)^2}{L_m\ \left(2\pi\, f_{sw}\right)^2}, \tag{19}$$

where L_m is the magnetising inductance.

D. Secondary-Side Rectifier Diode, RC Snubber, Resonance Capacitor, Output Inductor and Output Capacitor

The reverse voltage $V_{D(rv)}$ and forward current I_D of the rectifier diode D_1 can be calculated based on [25]:

$$I_D = \frac{I_{o(max)}}{1 - d_{max}}, \tag{20}$$

$$V_{D(rv)} = V_o + \left(\frac{V_{in(max)}}{n}\right), \tag{21}$$

$$R_{sn} = 2\pi\, f_{ring} L_k. \tag{22}$$

During rectifier diode D_1 turn-off, V_D will also spike with a high frequency of oscillation. A protection circuit on the secondary side, as in [29] and [30], are examples of RC snubber used to effectively damp out the ringing. In [31], the steps to determine the snubber resistor R_{sn} and the capacitor C_{sn} were detailed, where L_k is the leakage inductance, while f_{ring} is the frequency of the oscillation of voltage across D_1 without a snubber circuit

$$C_{sn} > \frac{1}{2\pi\, f_{ring} R_{sn}}. \tag{23}$$

In the secondary-side resonance CCM-ACF, L_k resonates with both C_{clamp} and C_{sr}. When the C_{clamp} is large enough, traditional CCM-ACF becomes a secondary-side resonance. Based on the value obtained in (19), C_{clamp} is then increased

so that VC_{clamp} reaches almost constant, as depicted in Fig. 4. The voltage is to be considered constant when its ripple is maintained within a range of 5 % to 10 % of the nominal value [13]. A smaller secondary-side resonance capacitor C_{sr} is then added, where $C_{clamp} >> C_{sr}/n^2$, purposely so that C_{sr} dominates the resonance with the leakage inductance L_k [21]. An output filter is added to suppress the ripple in the output voltage. Based on previous research and considerations, the values of C_{Clamp}, C_{sr}, and L_o are selected as 1 µF, 1 µF, and 1 µH, respectively. To determine the output capacitor C_o, it is related to the output voltage ripple ΔV_o and the switching frequency f_{sw} as in [25]

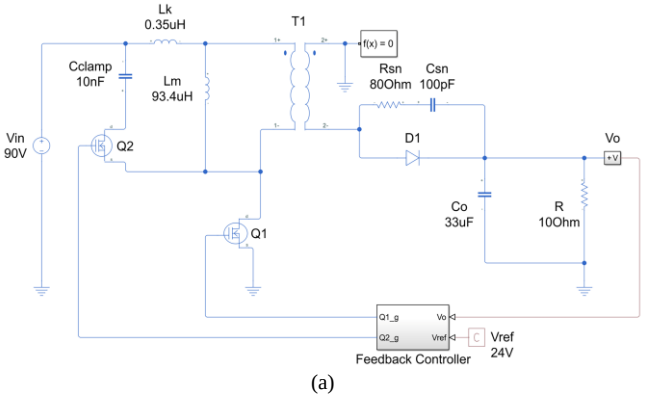
$$C_o > \frac{I_{o(max)}\, d_{max}}{\Delta V_o\, f_{sw}}. \tag{24}$$

V. Results and Discussion

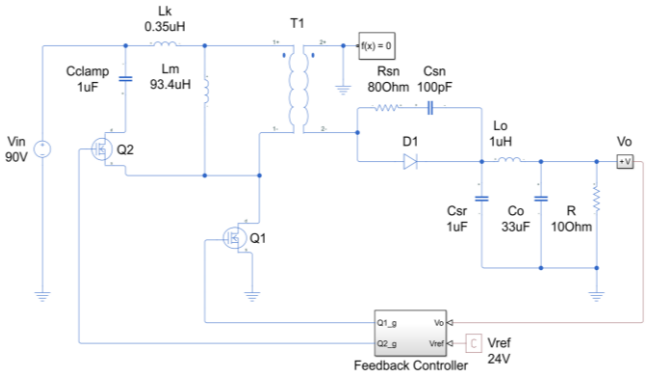
To compare the ZVS realisation of the main switch, switching stress, output voltage ripple, transient response, and efficiency, a simulation through MATLAB Simscape environment has been performed. Both circuits were composed of similar components and power ratings. Table I list down the parameters, whilst Fig. 9 shows the models of traditional and secondary-side resonance CCM-ACF composed in MATLAB Simscape for simulation verification of the converter. The selected transformer is WE-FLEX 749197341 by Wurth Electronics, main and active-clamp switches are 650 V SuperGaN TP65H150G4PS by Transphorm, and the secondary rectifier diode is a 300 V 15 A Hyperfast Rectifier by Vishay Semiconductors. It is worth noting that C_{oss1} and C_{oss2} were not visible on both models, as they are defined under the properties of both GaN switches, as shown in Fig. 9(c).

TABLE I. PARAMETERS USED FOR SIMULATION VERIFICATION.

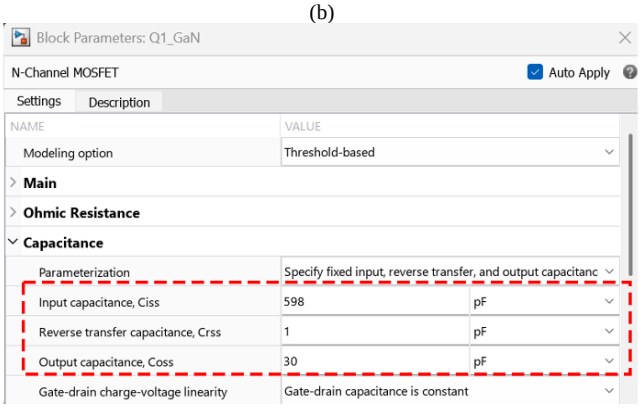
Parameter	Value
Input Voltage, V_{in}	90 V–100 V
Output Voltage, V_o	18 V–24 V
Switching Frequency, f_{sw}	1 MHz
Rated Power, P_o	60 W
Transformer magnetising inductor, L_m	93.4 µH
Transformer turn ratio, $n:1$	2:1
GaN's switches output capacitor, C_{oss1} & C_{oss2}	30 pF
Clamp Capacitor, C_{clamp}	1 µF
Secondary-side resonance capacitor, C_{sr}	1 µF
Secondary-side snubber resistor, R_{sn}	80 Ω
Secondary-side snubber capacitor, C_{sn}	100 pF
Output capacitor, C_o	33 µF
Output inductor, L_o	1 µH



(a)



(b)



(c)

Fig. 9. Model of ACF composed in MATLAB Simscape for simulation verification: (a) Traditional CCM-ACF; (b) Secondary-side resonance CCM-ACF; (c) Properties window of GaN switch.

Figures 10–13 show the simulated waveforms of the main switch gate signal V_{gs_Q1} and the voltage between the drain and source V_{ds_Q1}, with $V_{in(min)}$ = 90 V and output power P_o = 30 W. The ZVS of traditional CCM-ACF is unrealised, where V_{ds_Q1} does not fall to zero before the gate signal arrived, as depicted in Fig. 10. Traditional CCM-ACF starts to demonstrate ZVS realisation once the output power is 40 W, as depicted in Fig. 11. In contrast, the ZVS of the secondary-side resonance is realised under a light load of output power P_o = 30 W, as depicted in Figs. 12 and 13. This is due to the resonance that occurs between [t_3-t_4], as depicted in Fig. 2, and Fig. 4 differs between both topologies and caused changes in the leakage inductance current waveform. These changes cause a different peak negative value of leakage inductance current when the active-clamp switch Q_2 is OFF at t_4, as depicted in Fig. 14. This affects the energy stored in the leakage inductance required to fully discharge the energy stored on the output capacitor of Q_1.

The switching stress is related to the peak voltage that it must maintain. Figure 15 shows the comparison of the voltage and rms current stress on the main switch Q_1, the active-clamp switch Q_2, and the secondary rectifier diode D_1, respectively. It can be observed that the main switch Q_1 of traditional CCM-ACF suffers a higher voltage stress compared to its counterpart, and its rms current is noticeably high at low output power. Meanwhile, the active-clamp switch Q_2 of secondary-side resonance CCM-ACF has to sustain higher voltage stress, but it comes with lower rms current compared to its counterpart. This will help to reduce the conduction power loss of Q_2. However, for the secondary rectifier diode, both voltage and rms current of the secondary-side resonance CCM-ACF are slightly higher compared to that of its counterpart.

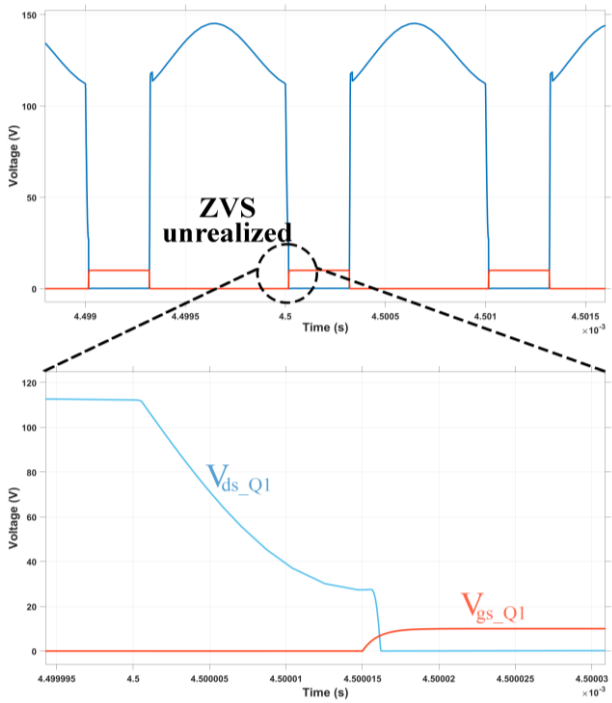


Fig. 10. ZVS of the main switch Q_1 for traditional CCM-ACF at output power P_o = 30 W.

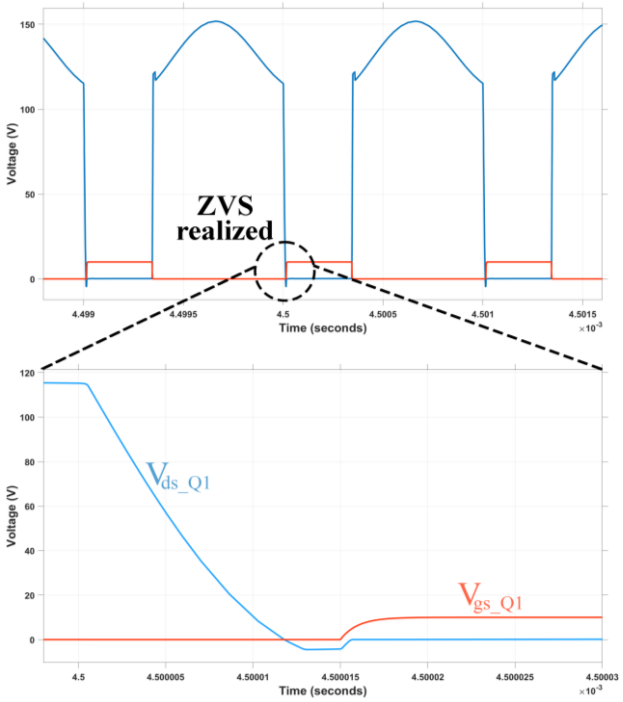


Fig. 11. ZVS of the main switch Q_1 for traditional CCM-ACF at output power P_o = 40 W.

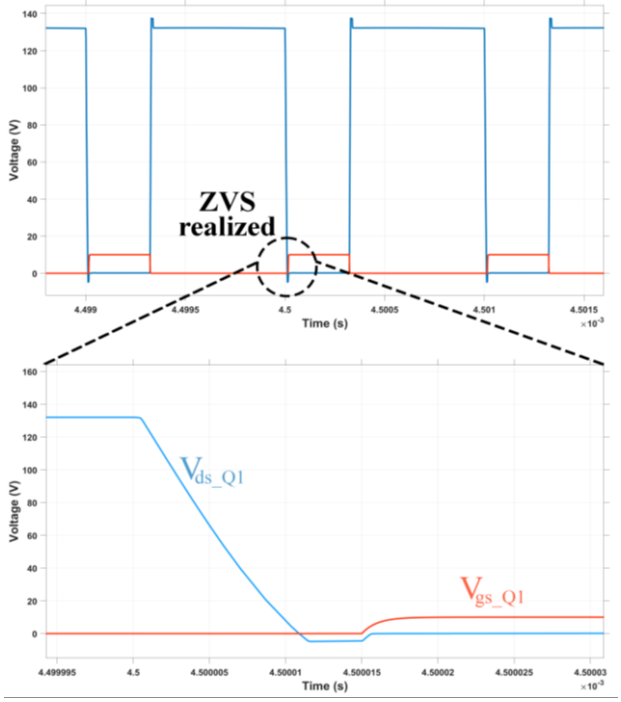


Fig. 12. ZVS of the main switch Q_1 for secondary-side CCM-ACF at output power P_o = 30 W.

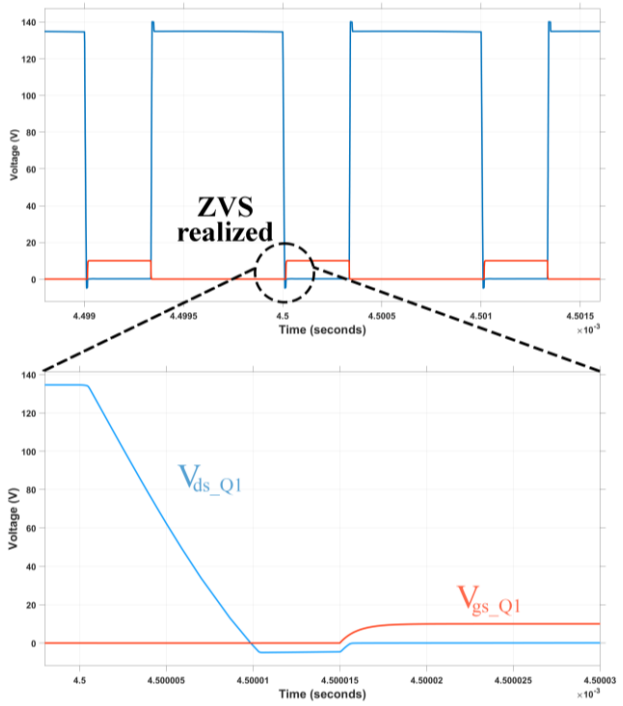


Fig. 13. ZVS of the main switch Q_1 for secondary-side CCM-ACF at output power P_o = 40 W.

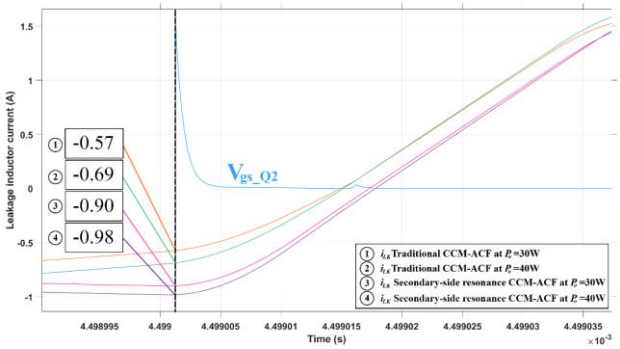
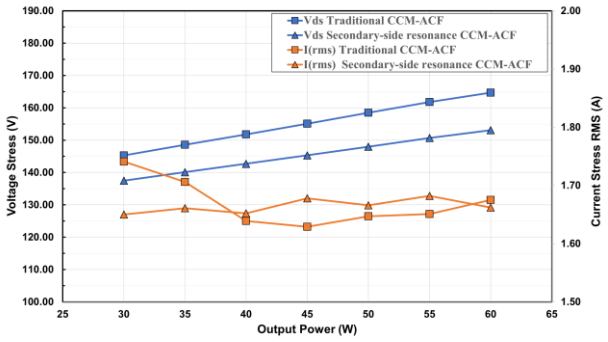
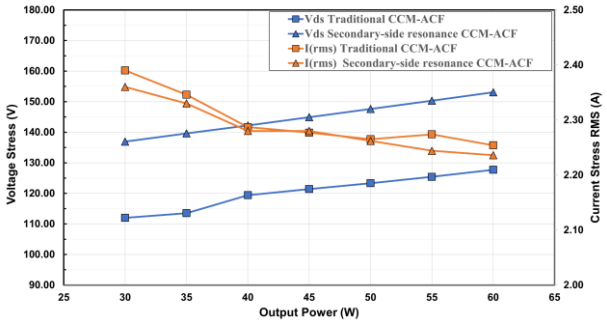


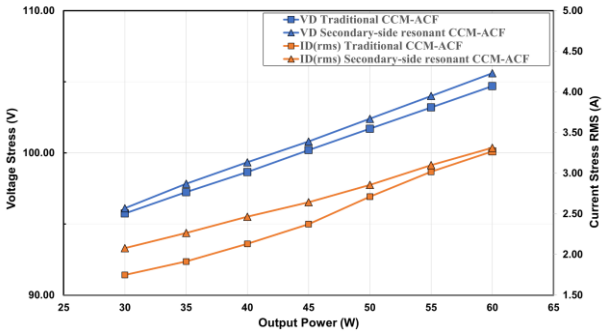
Fig. 14. Peak value of i_{lk} when Q_2 OFF for both traditional and secondary-side CCM-ACF under light load.



(a)



(b)



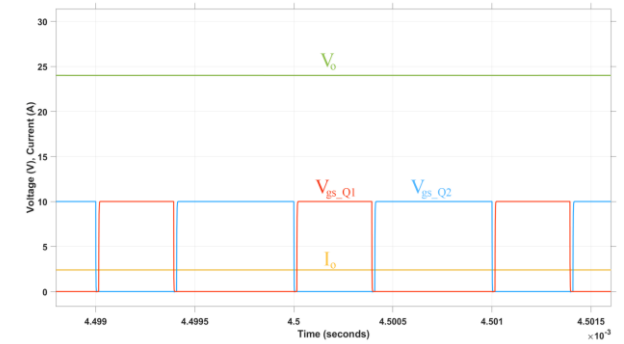
(c)

Fig. 15. Peak voltage and rms current of main switch Q_1, active-clamp switch Q_2 and secondary rectifier diode D_1: (a) Q_1 switching stress; (b) Q_2 switching stress; (c) diode D_1 switching stress.

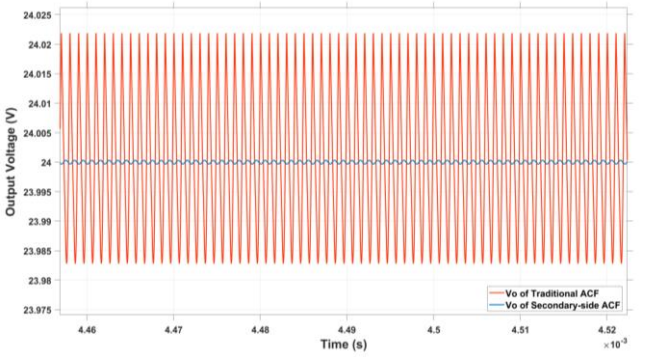
Figure 16(a) shows the output voltage V_o and the output current I_o with respect to the switching signal of the main switch V_{gs_Q1} and active-clamp switch V_{gs_Q2} at $V_{in(min)}$ = 90 V and output voltage V_o = 24 V. It is observed that the output voltage and current are stable throughout the converter operation. With the help of a simple output filter, the ripple in the output voltage of secondary-side resonance CCM-ACF is remarkably lower than that of its counterpart, as depicted in Fig. 16(b). This will become an advantage of a more stable and less noise from the converter to the load, especially if the load is sensitive to voltage variation and noise interference. To verify the performance of the transient response, a stepped output voltage is measured, as depicted in Fig. 17. This is achieved by changing the reference voltage V_{ref} through a PS Step instead of a constant function in MATLAB-Simscape. The duty cycle of both switches is then controlled to achieve the desired output voltage. With the input voltage of 90 V, the output voltage is stepped from 0 V to 18 V at t = 0 s. The transient response of secondary-side resonance is much better, where the settling time taken is 0.84 ms, which is 31 % faster compared to traditional CCM-ACF. At t = 2.5 ms, the output voltage is stepped further from 18 V to 24 V, the output voltage of the secondary-side resonance CCM-ACF oscillates with a higher peak value and requires 31 % longer settling times compared to traditional CCM-ACF.

The efficiency of secondary-side resonance CCM-ACF is always slightly higher compared to traditional CCM-ACF, as depicted in Fig. 18. Due to lower rms current, the conduction loss of the active-clamp switch Q_2 is reduced, as depicted in Fig. 19. This contributes to an increase of efficiency up to 93.99 %, which is equal to 0.56 % improvement. An investigation is conducted to investigate the relationship between $(C_{sr}/n^2)/C_{clamp}$ and efficiency. This is to justify the selection of C_{sr}. The value of the clamp capacitor C_{clamp} is fixed at 1 µF so that VC_{clamp} is constant while the value of the secondary-side resonance capacitor C_{sr} is varied. Figure 20 shows the relation between different ratios of reflected C_{sr} and C_{clamp} to the efficiency of the converter. It is observed that the efficiency does not change much when the ratio is increased from 0.2 to 0.3, and the efficiency stays constant once the ratio is increased further. The highest efficiency occurs when the ratio is small, which means that a small value of C_{sr} is selected. However, due to this, the output voltage ripple worsens. Thus, consideration must be taken to achieve the best efficiency with acceptable output voltage ripple. Based on the simulation, the selected ratio is 0.25, where C_{clamp} and C_{sr} are both 1 µF, respectively.

A comparison between the proposed topology and previous literature is summarized in Table II. It can be validated that the efficiency of the MHz frequency of the active-clamp flyback DC-DC converter operating in CCM can be improved through secondary-side resonance topology.



(a)



(b)

Fig. 16. Waveform of the output voltage and current: (a) Waveform of the output voltage and current waveform relative to the switching of $Q1$ and $Q2$; (b) Comparison of the ripple of the output voltage with $V_{in(min)}$ = 90 V and V_o = 24 V.

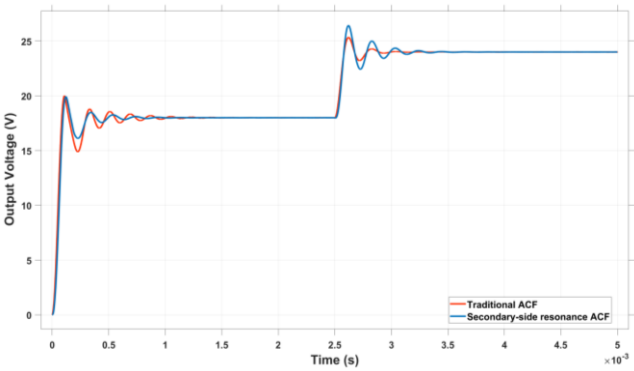


Fig. 17. Output voltage transient when the output voltage is stepped from 0 V to 18 V at t = 0 ms and 18 V–24 V at t = 2.5 ms.

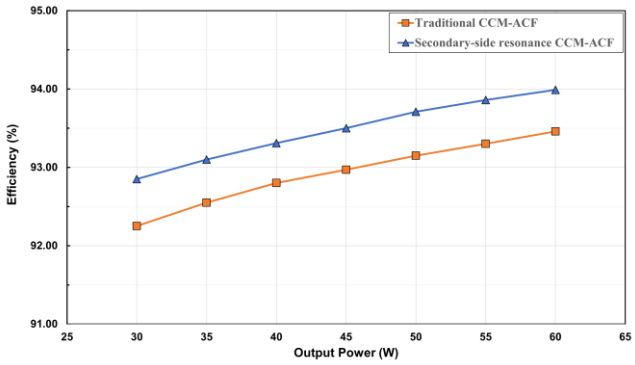


Fig. 18. Comparison of efficiency between output power of 30 W–60 W with $V_{in(min)}$ = 90 V.

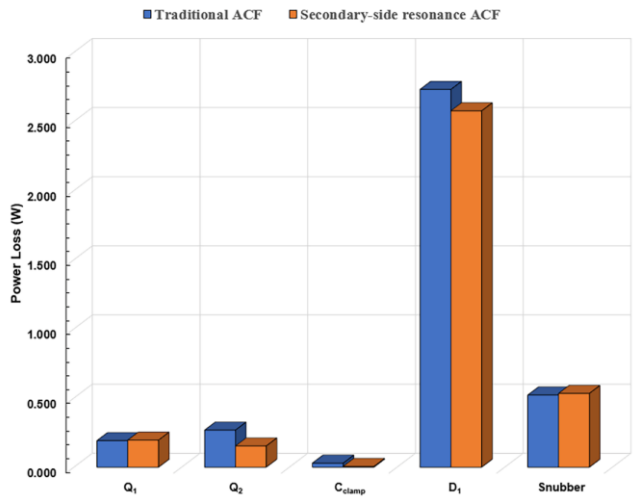


Fig. 19. Comparison of power losses with $V_{in(min)}$ = 90 V and output power of 60 W.

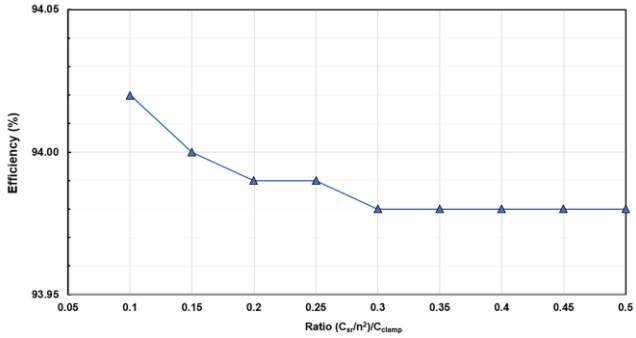


Fig. 20. Relationship between ratio of $(C_{sr}/n^2)/C_{clamp}$ and the efficiency of the converter.

TABLE II. PERFORMANCE COMPARISON WITH OTHER WORKS.

Symbol	[10]	[11]	[16]	[22]	This Work
Topology	PSR & SSR-ACF	PSR	PSR	SSR	SSR
Operation Mode	DCM	CCM	DCM	DCM	CCM
Switching Frequency (MHz)	0.6	1	0.5	0.6	1
Synchronous Rectifier	Yes	No	Yes	Yes	No
Output Power (W)	65	300	200	65	60
Peak efficiency (%)	93.2	93	93.2	92.8	93.99

VI. CONCLUSIONS

This manuscript presents a comparative performance analysis between traditional and secondary-side resonance CCM-ACF. Both topologies were simulated in MATLAB Simscape to evaluate ZVS realisation of the main switch, switching stress, output voltage ripple, transient response, and efficiency. Simulation results show that the secondary-side resonance CCM-ACF can realise ZVS of the main switch even under light load, with significantly lower output voltage ripple and improved transient response. Although the active-clamp switch experiences higher voltage stress, it benefits from a lower rms current. Maximum efficiency of 93.99 % is achieved, marking a 0.56 % improvement. Varying the ratio of $(C_{sr}/n^2)/C_{clamp}$ indicates that reducing C_{sr} improves efficiency but worsens the output voltage ripple. The operation principle and design consideration of the high-frequency secondary-side resonance CCM-ACF are also discussed. These findings aim to guide power designers in selecting power switch ratings and secondary-side resonance capacitor values during the early stage of the design of the ACF DC-DC converter.

CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

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