Furtherance of Multilevel Inverter and Evolution of a Packed Inverter Unit for Dynamic Loads

Premkumar R[1,2,*], Vimala Juliet A[2], Vijayaraja L[3]
[1]*Department of Electronics and Instrumentation Engineering, Sri Sairam Engineering College, Chennai, 600044, India*
[2]*Department of Electronics and Instrumentation Engineering, SRM Institute of Science and Technology, Kattankulathur, Chennai, 603203, India*
[3]*Department of Electrical and Electronics Engineering, Sri Sairam Institute of Technology, Chennai, 600044, India*
[*]*premkumar.rajavel@gmail.com, vimalaja@srmist.edu.in; vijayarajal.eee@gmail.com*

***Abstract*—Multilevel inverters (MLIs) provide a solution for high-power applications due to the production of a high-quality output voltage with low harmonic distortion. This technology is gaining popularity in the power industry for applications such as renewable energy systems, motor drives, and electric vehicles. MLIs are categorised on the basis of the number of levels in their output waveform. This article includes a discussion of two, three, and higher-level inverters with respect to design aspects and their application in the power industry, contributing to the development of sustainable and efficient systems. In addition, a packed inverter unit (PIU) with 11 IGBT switches and three uneven DC voltages is used to generate 11 voltage steps. From the suggested axioms, the amplitude of the DC sources is chosen to generate larger voltage steps with the fewest possible circuit components. Additionally, an 11-level inverter is simulated for fixed and variable R/RL loads. A comparison analysis of the circuit components between the developed circuit and existing MLIs is carried out. Finally, 11-level inverters are evaluated in real time for constant, fluctuating R/RL loads, and various performance metrics are noticed.**

***Index Terms*—Asymmetric DC sources; Packed inverter; Power drivers; Pulse width modulation; Total harmonics reduction.**

I. INTRODUCTION

With the evolution and growth of power electronics devices, namely the increase in switching speed, the ability to conduct higher currents and withstand large voltage values when blocked, as well as the existence of controllers with greater capacity and processing speed such as the field programmable gate array (FPGA) and the digital signal processor (DSP), it became possible to implement the multilevel converter (MLC). Multilevel conversion (MLC) finds place in renewable energy grid, such as photovoltaic energy, wind energy, fuel cells, and electric traction applications. The MLC fixes the voltage levels at which the different alternating voltage levels at the output are generated through the correct commutation of the switches. Thus, the MLC has advantages and disadvantages over two-level converters, especially for medium- and high-power applications. The concept of using multiple voltage levels to convert electrical energy was patented by Massachusetts Institute of Technology (MIT) researcher R. H. Baker, more than thirty years ago [1], [2].

The MLCs have been compared to conventional two-level converters in medium, large power and medium, high voltage applications, which demonstrates reduction of electromagnetic interference levels, possibility of obtaining higher levels of power, switching frequency higher than that of a conventional converter, and low switching losses, reduction of harmonic content. Also some of the disadvantages include a greater number of switches, which increases as you have more voltage levels at the output of the converter, thus increasing the implementation cost, modulation strategies are more complex, and the continuous side of the converter has different voltage levels that can be obtained by independent continuous sources or by capacitors. The disadvantages presented have been increasingly reduced over time due to the evolution of electronic devices that over time have increased their power and switching frequency, with increasingly reduced prices. Regardingelectronic device control, there arecurrently several solutions, such as DSPs and FPGAs, which are faster signal processors and have great calculation capacity, thus facilitating MLC control. In this paper, we discussthe following topics:

1. Type of multilevel inverter (MLI);
2. New multilevel inverter design (packed inverter).

The research aims to contribute a novel MLI topology with reduced circuit components while maintaining performance. This includes the following:

- Reducing the number of switches and sources for a simpler design;
- Ensuring lower harmonic distortion and stable voltages;
- Testing the proposed topology under real-time conditions.
- The development of this new topology addresses the complexity and cost challenges faced by conventional MLIs, making it a promising advancement in power electronic converters.

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II. MULTILEVEL TOPOLOGIES (ML)

Multilevel inverters (MLIs) are power electronic devices that convert DC power to AC power at a higher voltage level than conventional two-level inverters. MLIs use a series of power switches and capacitors to generate multiple voltage levels in the output waveform. This allows for lower harmonic distortion and a smoother output waveform compared to traditional two-level inverters. There are several types of MLI, which can be classified according to the topology or the number of voltage levels. Currently, there are different topologies of MLCs. Among all existing topologies, there are three that have prevailed in the market, the most developed with a greater number of applications.

The topologies studied here are:

– Converter with diodes fixed to the neutral point (neutral point clamped (NPC) or diode clamped converter (DCC));
– Floating capacitor converter (flying capacitor converter); Conventional cascaded converter (cascaded full bridge converter);
– However, other topologies are emerging, such as:
  – Multi point clamped converter (MPC); Hybrid asymmetric converter;
  – Diode/Capacitor-clamped converter.

A. Diode-Clamped MLI (DCMLI) or Neutral Point Clamped (NPC) Inverter

The concept of an MLC using diodes fixed to the neutral point was introduced with the proposal of a three-level converter, which was later called a converter with diodes fixed to the neutral point (NPC). Figure 1 shows a three-level converter.

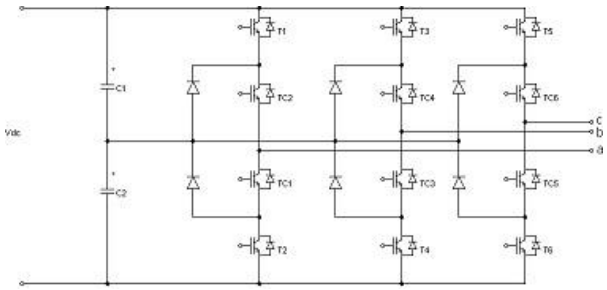


Fig. 1. NPC three-level converter.

The referenced voltage levels are obtained by a set of switch states; these states are presented in Table I, and the voltage waveforms are illustrated in Fig. 2.

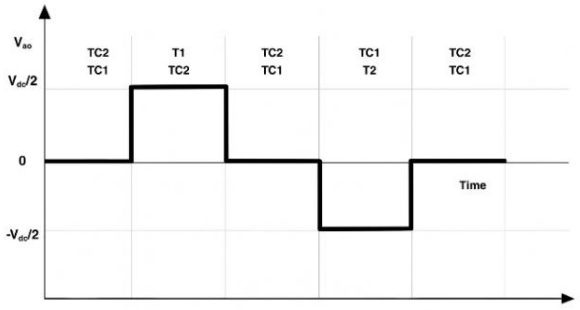


Fig. 2. V_{ao} output voltage for the three-level converter shown in Fig. 1.

In this topology, it is necessary to pay attention to the inverse voltage drop across the diodes, since when switches T1-T2-T3-T4 are on, the voltage drop that diode D3 has to withstand is equal to $3V_{dc}/4$, as can be seen in Fig. 2. One way to solve this problem is to insert diodes in series, thus dividing the voltage supported by them. However, this solution significantly increases the number of semiconductors used, which leads to an increase in the complexity of the structure. The same situation is verified in diode D4 when switches TC1-TC2-TC3-TC4 are on.

TABLE I. SWITCHING SEQUENCE TO OBTAIN THE THREE VOLTAGE LEVELS.

Connected Switches	**V_{ao}**
T1-TC2	$V_{dc}/2$
TC2-TC1	0
T2-TC1	$-V_{dc}/2$

The advantages of this topology are:

– Each switch must block a voltage equal to $V_{dc}/(n-1)$ for n voltage levels;
– The number of capacitors used in this topology is lower compared to other ML topologies, thus reducing implementation costs;
– The change between voltage levels is carried out only by activating one of the switches, reducing losses and interference;

The disadvantages presented by this topology are the following:

– In topologies with more than three levels, the diodes do not block the same voltage levels, making it necessary to add diodes in series, which increases the cost and complexity of the project;
– The voltage at the capacitor terminals must remain stable and balanced, which leads to an increase in the complexity of the converter control algorithm;
– The clamping diodes have to be fast recovery since they switch at the switching frequency.

After analysing the advantages and disadvantages of this topology, it is verified that this topology presents all the advantages of the MLC and that the disadvantages only become significant when the NOL is greater than 3. Therefore, for applications with 3 voltage levels, the converter with diodes fixed to the neutral point is a good choice.

B. Flying Capacitor MLI (FCMLI)

This type of inverter uses capacitors that "fly" between different voltage levels to generate the output waveform. The number of capacitors determines the number of voltage levels. FCMLIs are used in applications where low harmonic distortion and high efficiency are required.

This topology is one of the most recent, being introduced in the 1990s [1], [3]. Figure 3 shows a three-level floating capacitor converter. The three-level floating capacitor topology, like the NPC topology, can have the following values at the V_{ao}, V_{bo}, and V_{co} outputs: $V_{dc}/2$, 0 and $-V_{dc}/2$. Switch pairs T1-TC1, T2-TC2 are complementary; the same logic applies to the other two branches. The V_o values are obtained by different states that are represented in Table II. Although the output waveform is similar to that of the NPC topology, the switching is different, since there is a redundant state, i.e., there are two states in which an equal voltage is obtained, as shown in Fig. 4.

The floating capacitor C3 is charged when switches T1

and T2 are on and discharged when switches TC1 and TC2 are on. This is only valid when the positive reference of the converter current is considered the current that enters it [1]; if the load supplies the converter current, this situation is reversed. The charging of capacitor C3 can be controlled by selecting the combination of active switches at zero voltage level. Converters with floating capacitors have greater flexibility to control switches, which allows better control of energy flow compared to MLC with diodes fixed at the neutral point [1].

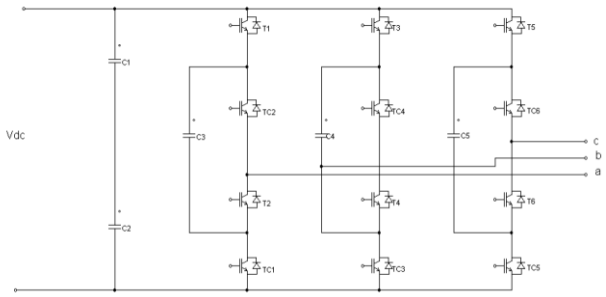


Fig. 3. Three-level converter of the flying capacitor.

TABLE II. SWITCHING SEQUENCE TO OBTAIN THE THREE VOLTAGE LEVELS.

Connected Switches	V_{ao}
T1-T2	0
T1-TC2	$V_{dc}/2$
TC1-TC2	0
T2-TC1	$-V_{dc}/2$

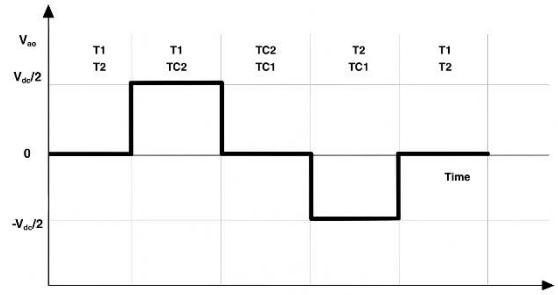


Fig. 4. V_{an} output voltage for the three-level converter.

C. Cascaded H-Bridge MLI (CHBMLI)

This type of inverter uses a series of H-bridge modules to generate multiple voltage levels. Each H-bridge module can be switched independently to create different voltage levels. CHBMLIs are commonly used in renewable energy sources (RES), motor drives, and power quality improvement (Fig. 5).

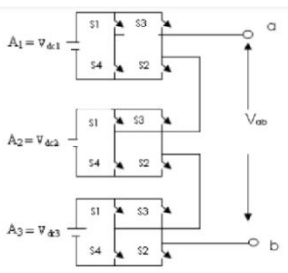


Fig. 5. Cascaded H-bridge MLI.

– Stacked MLI: This type of inverter uses multiple series two-level inverters to generate multiple voltage levels. Stacked MLIs are commonly used in low to medium voltage applications, such as motor drives and RES.

– Asymmetric MLI: This type of inverter uses different voltage levels on the positive and negative sides of the output waveform to reduce the number of switches and increase efficiency. Asymmetric MLIs are commonly used in low voltage applications, such as motor drives and grid-tied solar inverters.

– Hybrid MLI: This type of inverter combines two or more of the above types of MLI to achieve higher voltage levels and lower harmonic distortion. Hybrid MLIs are commonly used in high-power applications, such as RESs and motor drives.

The selection of the type of MLI depends on the specific application requirements, such as voltage level, harmonic distortion, efficiency, and cost.

1. Stacked MLI

Figure 6 systematically shows an arm of a converter with different numbers of levels, where the continuous side has a set of capacitors in series and the converter arm consists of a series of switches, with different voltage levels at the output forming a ladder voltage waveform. A two-level converter has V_o with two levels, while the three-level converter has V_o with three levels, and successively the n-level converter has n levels of V_o [1]. Considering that n is the NOL per branch in a three-φ converter, the voltage between phases will have k levels, which can be calculated using the following equation

$$k = 2n - 1. \tag{1}$$

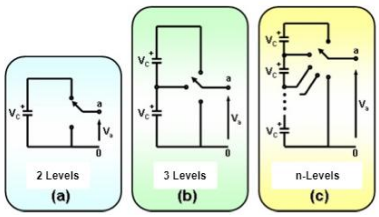


Fig. 6. (a) Arm of a converter with two levels; b) Arm of a converter with three levels; c) Arm of a converter with n levels.

The number of voltage levels (p) that exist in a converter is calculated using the following expression

$$p = 2k - 1. \tag{2}$$

Thus, for a three-level converter, the phase-to-phase voltage will have five levels and phase-to-neutral voltage will have nine levels.

2. Asymmetric MLI

In the topology known as asymmetric MLC (Fig. 7), it is possible to work with different voltage levels between cells or modules [4].

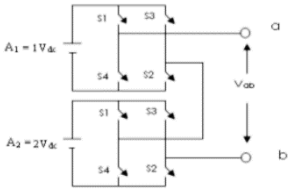


Fig. 7. Asymmetric MLI.

3. Hybrid Converter

In Fig. 8, two modules of this MLC are shown, one of them with a voltage level equal to V_{dc} and the other with a voltage level equal to V_{dc}/n. MLCs have isolated DC sources, all of which have identical voltages. One way to increase the voltage without having to add any components is to have asymmetric DC sources, i.e., with different voltage levels [5]. If the converter in Fig. 8 had different DC sources, e.g., $2V_{dc}$ and V_{dc}, the output voltage would have seven levels. The use of asymmetric DC sources causes the use of different switches on each bridge to block different voltage levels.

Furthermore, various topologies are designed to generate multiple voltage levels; the circuits presented in [6], [7] describe neutral point clamped inverter with 11 and six switches that produce seven voltage levels. The proposed circuit follows predictive control technique, distributed maximum power point tracking (DMPPT) control, and artificial neural network method, respectively, to achieve the lower harmonics of 5.54 % and 2.35 %. This work gives immense study about the MLI method to follow and used in prescribed applications.

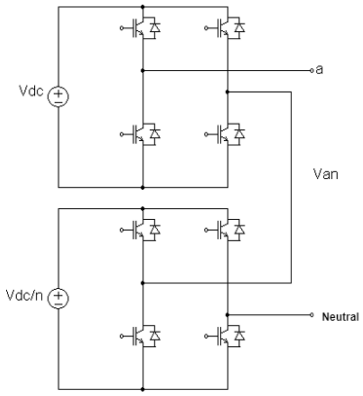


Fig. 8. Arm of an MLC with asymmetric hybrid modules [8].

In [9], the proposed method generates seven voltage levels in the response with 12 switches per phase, and a distributed MPPT control scheme is used. The presented module is the modular cascaded H-bridge multilevel inverter producing a lower harmonics of 4.2 %. The presented method in [10] requires more switches compared to other methods and observes THD of 3.3 %, looks less compared to the other methods discussed here. A new MLI voltage level boost [11] is presented with ten numbers of switches with more voltage levels in the output, 15 levels of output generated using the distributed maximum power point tracking method, and produces the THD of 5.54 %.

In [12], a symmetric cascaded half-bridge inverter is proposed to generate fifteen levels of output with multicarrier pulse width modulation technique. The configuration presented in [13], [14] uses more switches to achieve more level of output using modified hybrid multicarrier pulse width modulation. In [15], the H-bridge MLI is proposed with seventeen more switches and produces nine output levels that follow the selective harmonic elimination (SHE) PWM method, which requires more switches relatively to obtain levels.

In [16], dual-mode interleaved MLI and improved H-bridge MLI follow pulse width modulation method requires ten and five numbers of switches, respectively, to produce six levels of voltage in the output. The configuration explained in [17], [18] uses the phase disposition - carrier pulse width modulation (PD-CPWM) technique to generate 15 output levels using a cascaded H-bridge sub-MLI and five levels of output using micro MLI that utilise the seven and five number of switches, respectively. In [19], the switched capacitor multilevel inverter is proposed with eight number of active switches that generates seven voltage levels, follows swarm optimisation technique. The various types of topologies in MLI [20], [21] are designed using a large number of switches with fewer voltage levels using the pulse width modulation method. The inverter CHB and T type inverter method [22], [23] achieves minimum voltage levels that follow the sinusoidal carrier pulse width modulation and presents the THD of 2.01 %. In [24], the grid-connected method is analysed to design the switched capacitor multilevel inverter having 16 switches to generate 41 levels of voltage in the output.

The main topologies of the electronic power converters of ML and the main characteristics of each topology are presented in Table III, as well as the various modulation methods. The definition of the existence of a better topology and a modulation method cannot be concluded, because of the richness of the differences presented in each of the topologies.

The implementation of a certain MLC topology must be done observing the main characteristics of the application to which the converter will be submitted (Table IV); then, one must choose which modulation method is most appropriate for the topology in question.

TABLE III. RECENT MLI'S - OVERVIEW.

Ref.	Method	N_{level}	N_{Switch}	N_{Source}	$N_{Capacitor}$	N_{Diode}	Advantages	Limitations
[25]	Flying Capacitor MLI	17	12	2	2 per phase	4	V/F and d-q control	Low voltage inverter
[26]	Proton Exchange Membrane Fuel Cell	5	5	3	0	5	Simple circuit	Complexity in voltage balancing
[27]	Switched-DC-source sub-module MLI	13	10	3	0	0	Switching loss is comparatively low	Four voltage source
[28]	Single-Stage Switched-Capacitor MLI	9	12	2	4	2	Control technique is simple	Extra circuit components required
[29]	Neutral Point Clamp Inverter	9	16	1	8	14	Usage of sources is less	The utilisation of the DC bus voltage. It can only utilise up to 50 % of the DC bus
[30]	Cascaded Multilevel Inverter	7	24	3	6	6	Low THD	More number of switches
[31]	Modified Cascaded Multilevel Inverter	7	6	2	2	6	Low THD	Requirement of diode is high

Ref.	Method	N_{level}	N_{Switch}	N_{Source}	$N_{Capacitor}$	N_{Diode}	Advantages	Limitations
[8]	Asymmetric Cascaded Half-Bridge Inverter	7	6	3	0	6	Switching loss is low comparatively	Only for medium power applications
[32]	Improved H-bridge MLI	5	6	2	4	2	Low efficiency	Extra circuit components required
[33]	9L4x Inverter	9	10	1	3	2	Less switch loss	Voltage stress more
[34]	Packed E Cell	9	7	1	2	0	Grid connected	Fault tolerant

TABLE IV. MLI'S & ITS APPLICATIONS.

Ref.	Method	N_{level}	Applications
[35]	Single Phase Modified MLI	13	PV Applications
[36]	Reduced MLI	6	Grid Tied Applications
[37]	Quadruple Boost MLI	9	High Voltage Applications
[38]	ANPC Converter	5	Capacitor Balancing Voltage Applications
[39]	PD PWM MLI	9	Power Quality boosting
[40]	Neutral Point Clamped	2	Traction Applications
[41]	Hybrid Cascaded MLI	6	Fuel cells
[42]	Tri-State H-bridge MLI	485	PV/Fuel Cell Applications
[43]	Switched capacitor MLI	7	High frequency AC power distribution

Cost limitations, control complexity, operating flexibility, V_o level, and any other limitation that may make the application unfeasible must be considered when choosing the topology. From the above discussions, it is inferred that designing a multilevel inverter without complexity is a challenging task. Therefore, it is decided to develop a novel topology of a multilevel inverter with reduced circuit components, and the same is to be tested in real time.

III. DEVELOPMENT OF PACKED INVERTER UNIT

The structure of the proposed topology is of H-bridge type, which is chosen for its easy control and simple design. The H-bridge inverters conventionally consist of four switches and they are to be controlled by a controller circuit with nearest control techniques. Also, while using multiple independent DC sources for DC supply, the H-bridge topology is better suited when compared with the diode clamped topology and flying capacitor topology.

This H-bridge topology also requires no diodes, capacitors, or other added power electronic devices other than the switches. This will ultimately reduce the losses and the cost of the entire device. The configuration shown in Fig. 9 uses three separate DC sources (V1, V2, V3) and ten switches (S1–S10), where S1–S4 forms an H-bridge around the load resistor (R1) and S5–S10 controls the connection of each DC source to the main H-bridge through intermediate nodes. By combining sources, it can generate five positive voltage levels, and through H-bridge the shown configuration is able to produce 11 levels.

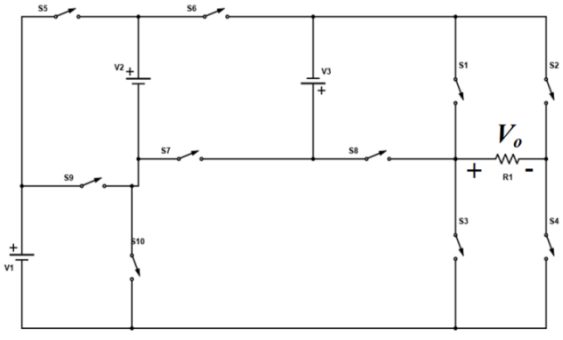


Fig. 9. Proposed packed inverter unit (PIU).

A. Definition of the Magnitude of Voltage Sources

1. *Method 1*: For V1 = V2 = V3 = V_{dc}

$$N_l = 2(3u)+1, \tag{3}$$

$$V_o = 3uV_{dc}volt. \tag{4}$$

2. *Method 2*: V1 = V_{dc}, V2 = $2V_{dc}$, V3 = $4V_{dc}$

$$N_l = 2(6u)-1, \tag{5}$$

$$V_o = \left(6^u\right)V_{dc}volt. \tag{6}$$

3. *Method 3*: V1 = V_{dc}, V2 = $2V_{dc}$, V3 = $3V_{dc}$

$$N_l = 2(4u)+1, \tag{7}$$

$$V_o = \left(4^u\right)V_{dc}volt, \tag{8}$$

where N_l and V_o arethe number of voltage levels and the maximum voltage generation across the load.

For all the above methods ((3)–(8)) to obtain the magnitude of the voltage sources, the circuit parameters such as the quantity of switches, drivers, "on" state switches, variety of DC sources, and DC sources are the same, and the following are given below:

$$N_{switch} = 10u, \tag{9}$$

$$N_{drivers} = 10u, \tag{10}$$

$$N_{on} = 4u, \tag{11}$$

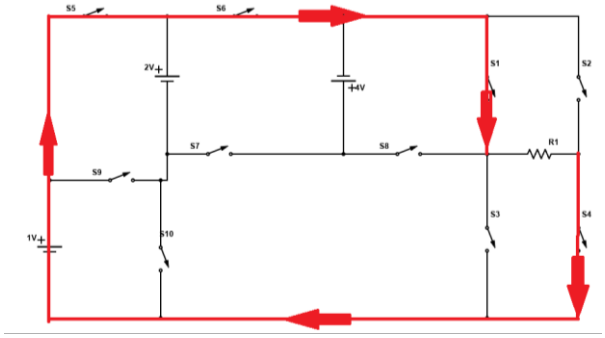
$$N_{variety} = 3u, \tag{12}$$

$$N_{source} = 3u. \tag{13}$$

The 11-level modes of operation for the proposed configuration shown in Fig. 9 and the switching sequences for each voltage level are given in Table V. Additionally, Table V shows that the notation "0" indicates that the switches are in the OFF state, while the notation "1" indicates that they are in the ON state. Thus, the maximum voltage obtained at the output is +5 V using PIU. The different voltage level generation is shown in Fig. 10.

TABLE V. SWITCHING STATE OF PROPOSED PIU.

V_{DC}	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
0 V	0	0	0	1	0	0	1	1	0	1
1 V	1	0	0	1	1	1	0	0	0	0
2 V	1	0	0	1	0	1	0	0	0	1
3 V	1	0	0	1	0	1	0	0	1	0
4 V	0	1	1	0	0	0	1	0	0	1
5 V	0	0	0	1	1	1	0	1	0	0
-1 V	0	1	1	0	1	1	0	0	0	0
-2 V	0	1	1	0	0	1	0	0	0	1
-3 V	0	1	1	0	0	1	0	0	1	0
-4 V	1	0	0	1	0	0	1	0	0	1
-5 V	1	0	0	1	1	0	1	0	0	0



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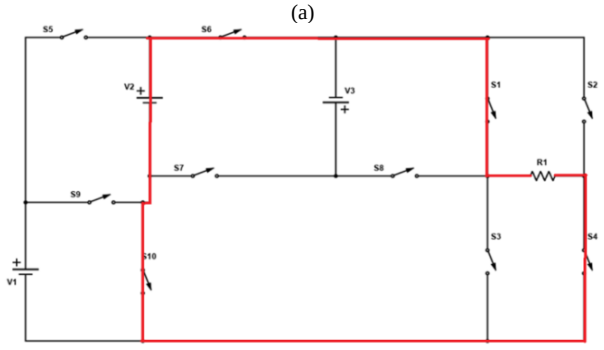

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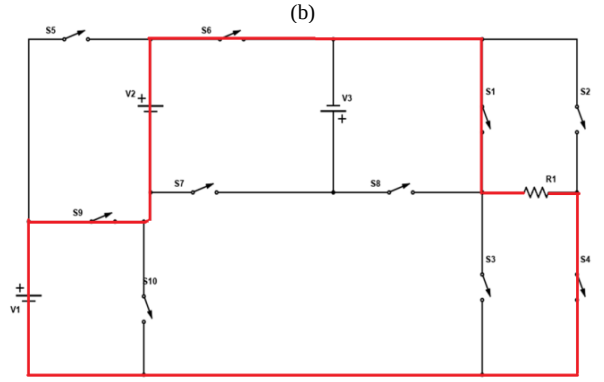

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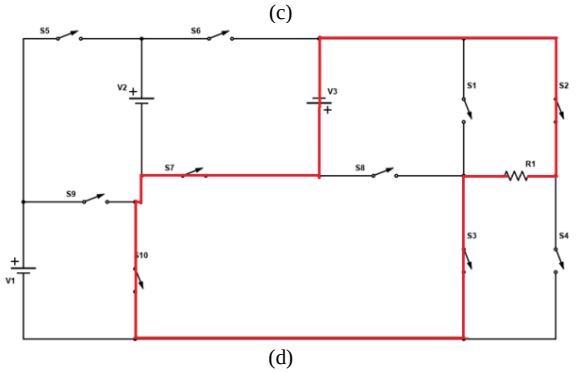

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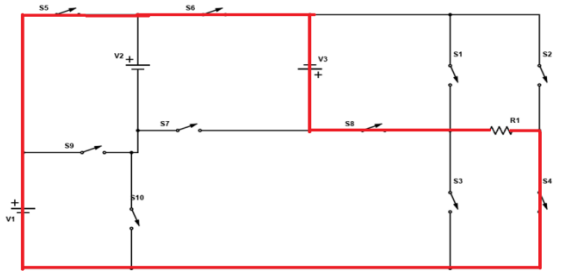

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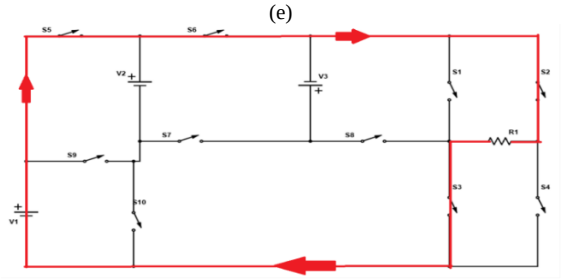

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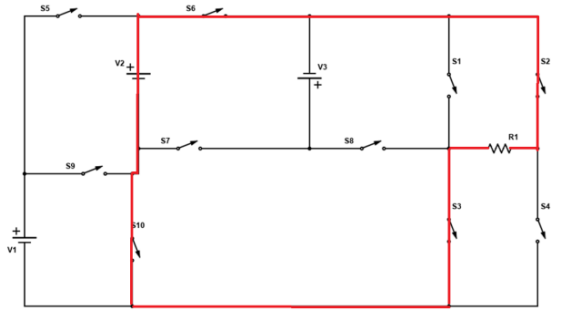

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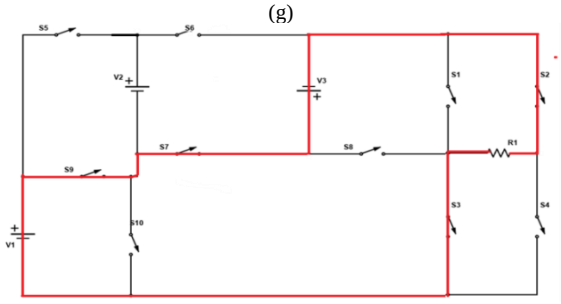

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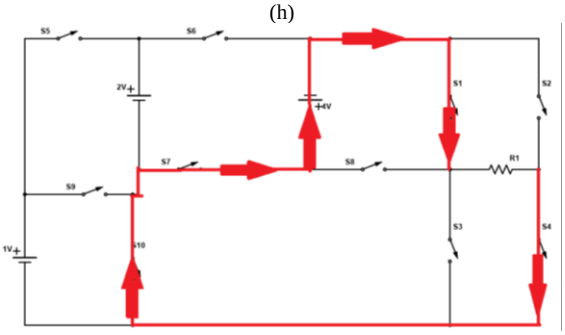
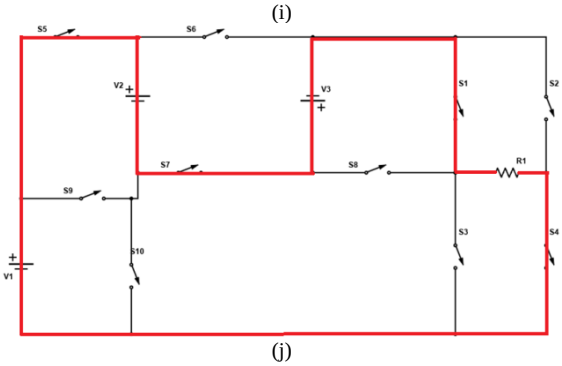


(i)



(j)

Fig. 10. (a) Mode 2 (1 V); (b) Mode 3 (2 V); (c) Mode 4 (3 V); (d) Mode 5 (4 V); (e) Mode 6 (5 V); (f) Mode 7 (-1 V); (g) Mode 8 (-2 V); (h) Mode 3 (-3 V); (i) Mode 10 (-4 V); (j) Mode 10 (-5 V).

B. Analytical Design Comparison of PIU with Other Works

The comparative study suggested by the inverterwith alternative topologies is shown in this section. Many factors have been compared, including the number of switches (N_{SW}), DC sources (N_S), output voltage levels (N_L), the number of "ON" switches ($N_{on,sw}$), and the variety of DC sources (N_V). Examination of the works in [44]–[49] reveals that the suggested inverter is shown in Figs. 11–15 with different design parameters for a multilayer inverter.

To produce the desired number of voltage steps at the output, the number of switches, driver circuits, and DC voltage sources utilised in the suggested inverter (T3) is compared with the invented MLI described in [44]–[49]. Also examined are the parameters related to these MLI circuits, as well as the number of "ON" state switches.

The comparison between the number of switches in the referenced circuit and the number of voltage steps created by the referenced MLIs is displayed in Fig. 11. Comparing T3 of the PIU with other mentioned MLIs, it is evident that fewer switches are needed. As a result, the inverter is smaller. By plotting the number of DC sources against T3 in Fig. 12, it can be seen that the suggested MLI uses the fewest DC sources compared to the others. As a result, the cost of the inverter is reduced.

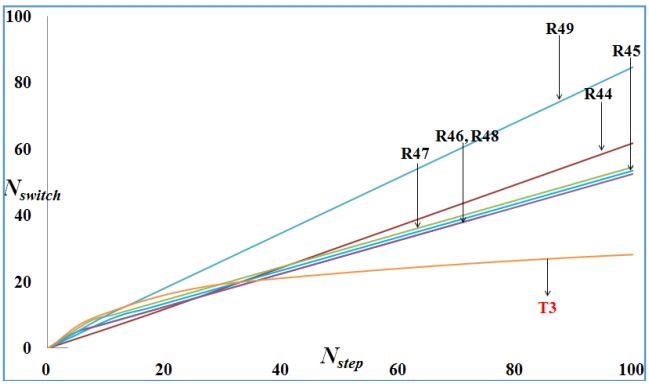


Fig. 11. N_{step} vs. N_{switch}.

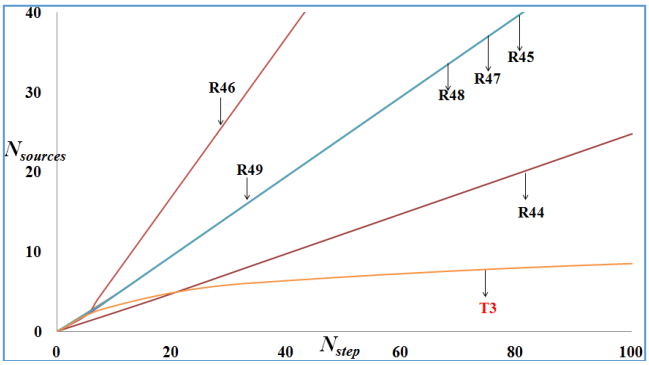


Fig. 12. N_{step} vs. $N_{sources}$.

In the comparison between N_{step} and N_{driver}, as shown in Fig. 13, the suggested inverter unit T3 uses fewer driver circuits than the others. The N_{step} vs. N_{on} state switches is displayed in Fig. 14. Compared to other PIUs, the proposed PIU has fewer "ON" state switches. This reduces the complexity of the control of the inverter. For the proposed MLI along with other referred MLIs, N_{step} vs. $N_{variety}$ is drawn. It is evident from Fig. 15 that the suggested MLI has fewer DC source varieties than the others. As a result, the cost of the inverter is reduced. It follows that the T3 design is superior to the other MLIs mentioned based on all the comparative graphs.

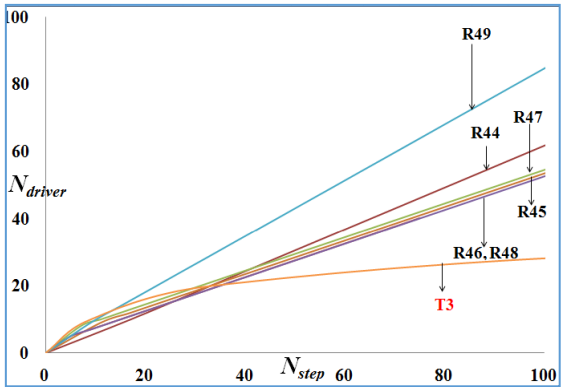


Fig. 13. N_{step} vs. N_{driver}.

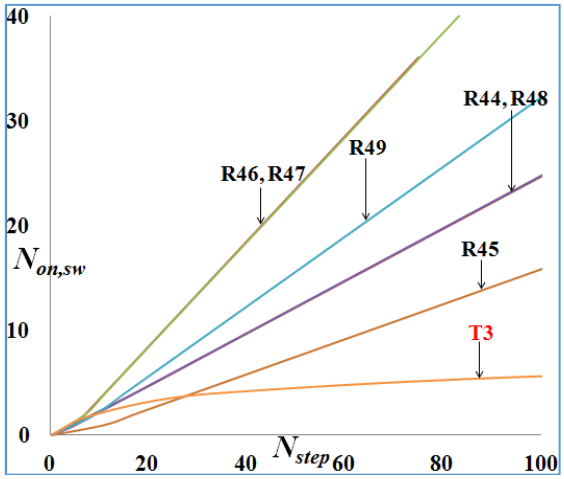


Fig. 14. N_{step} vs. N_{on}.

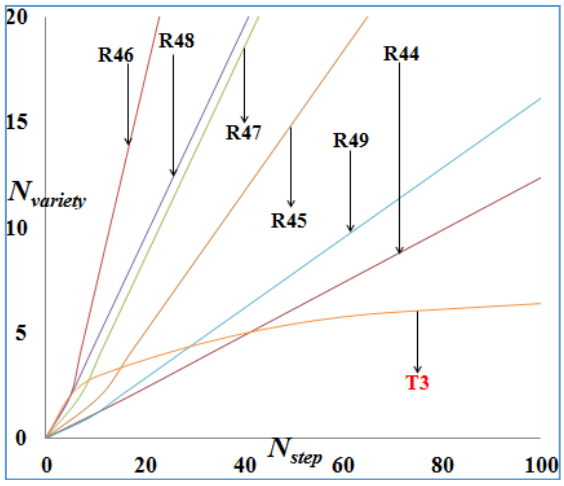


Fig. 15. N_{step} vs. $N_{variety}$.

From the analysis of Figs. 11–15, the following inferences are made: the proposed inverter uses fewer switching devices to achieve higher voltage levels, leading to a more compact and cost-effective design, also the requirement of fewer isolated DC sources indicated the reduced source dependency leading to simplified power management. Furthermore, the number of driver circuits required is significantly lower, and the "ON" state of the switches at any given time is minimised in the proposed design, reducing power losses, thermal stress, and control complexity.

IV. SIMULATION OF 11-LEVEL MLI

A. Control Technique

The theory and operation principle of pulse width modulation technique used for generating pulses for the switches of the inverter is performed using a simple technique called fundamental frequency method. This technique consists of four stages, a reference sine wave signal, comparators, logic circuits, and drive circuits to make suitable pulses for the switches, as shown in Fig. 16.

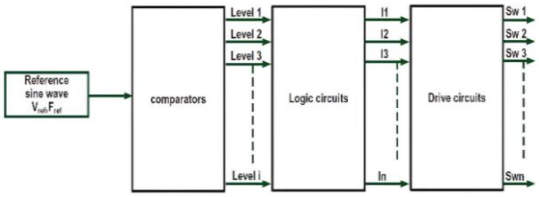
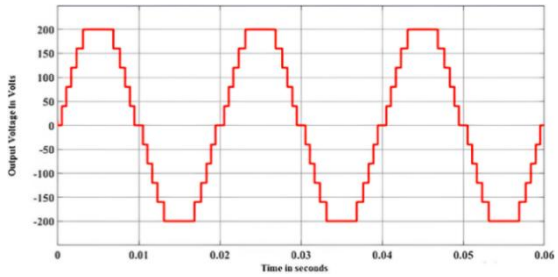


Fig. 16. Stages of the switching pulse scheme.

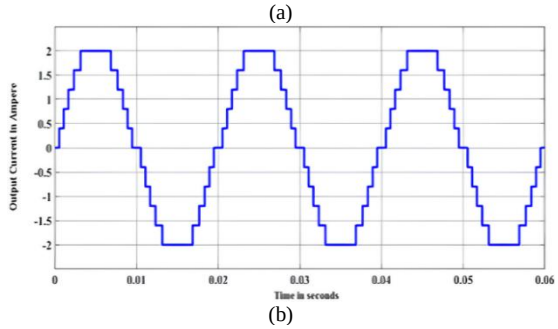
B. Simulation Results of 11-Level PIU

The MATLAB/SIMULINK environment is used to design and run the circuit simulation shown in Fig. 17. Figure 17(a) depicts the 11-level MLI output voltage waveform for R = 100 Ω load. The peak voltage is found to be ±200 V. Further, total harmonic distortion (THD) is calculated using fast Fourier transform (FFT) analysis and is depicted as 8.92 % shown in Fig. 17(d).

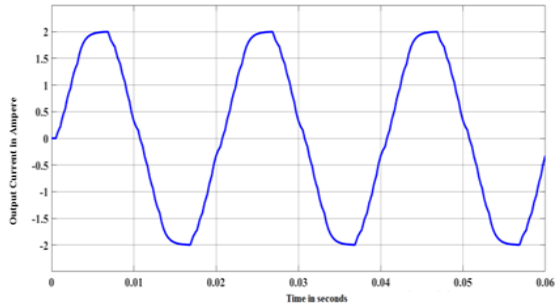
Furthermore, the circuit is implemented for the reactance load, with R = 100 Ω, L = 50 mH. The output voltage and output current are depicted in Fig. 17(a) and 17(b), and the THD for the load voltage is 4.82 % as shown in Fig. 17(e) and Fig. 17(f).



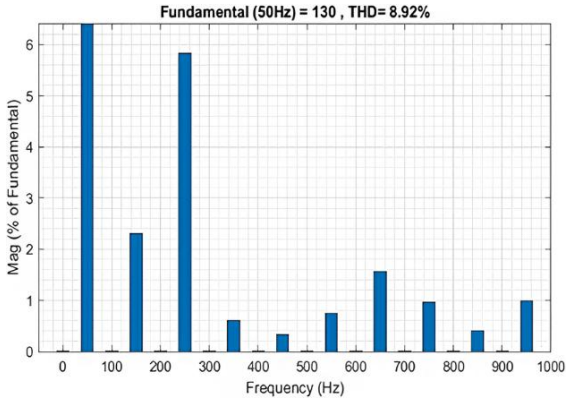
(a)



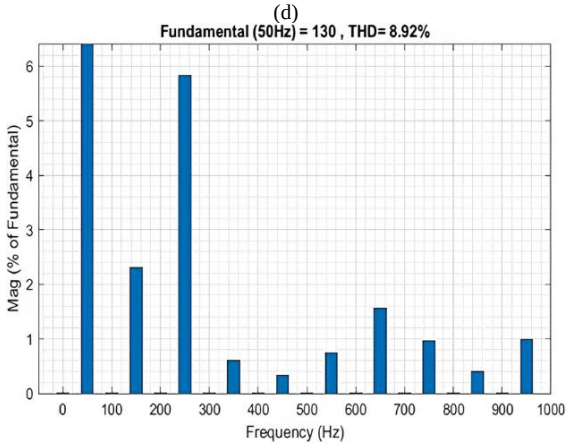
(b)



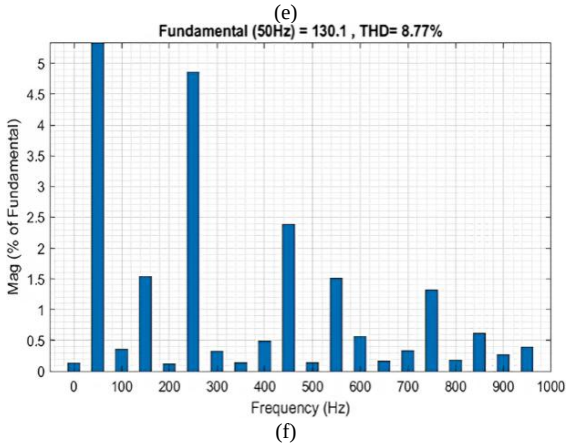
(c)



(d)



(e)



(f)

Fig. 17. (a) R and RL voltage output; (b) Output current for R load; (c) Output current for RL load; (d) Voltage and current THD for R load; (e) RL voltage THD; (f) Current RL THD.

C. Inverter Efficiency and Power Loss Calculation, Mean Lifetime

The loss of the power switch conduction and switching constitutes a total loss. The conduction losses for the switches can be calculated using (14)

$$P_{cl} = \left[V_{sw} + R_{sw} i^{\beta}(t)\right] i(t), \tag{14}$$

where V_{sw} and R_{sw} are the voltage drop across and the total resistance of IGBT. Taking into account the number of IGBTs (N_{IGBT}) for a particular conduction interval, the total conduction loss is given as in (15)

$$P_{clt} = \frac{1}{2\pi}\int_0^{2\pi}\left[N_{IGBT}(t) P_{tcl,IGBT}(t)\, dt\right]. \tag{15}$$

The switching loss [50] is obtained from the energy (E_{on} and E_{off}) used by the switches, as given in

$$P_{slt} = f\frac{1}{2\pi}\sum_{i=1}^{N_{IGBT}}\left[E_{ON}+E_{OFF}\right]=\frac{1}{6}V_{sw}\left(IT_{off}+I'T_{on}\right). \quad (16)$$

The total power losses (P_{plt}) and the efficiency are obtained as:

$$P_{plt} = P_{clt} + P_{slt}, \quad (17)$$

$$\eta = \frac{P_o}{P_o + P_{plt}}, \quad (18)$$

where the output power (P_o) is obtained from $V_{rms} * I_{rms}$. Taking into account the above equations, the efficiency is calculated η = 95.64 %.

The failure rate [51] for the system can be obtained by adding the failure rate of all components

$$\lambda_{CONVERTER} = \left(2\times\lambda_{MOSFET}\right)+\left(\lambda_{C_1}+\lambda_{C_2}\right)+\left(\lambda_{L_1}+\lambda_{L_2}\right)= = 0.74624\, failures/10^5 h. \quad (19)$$

Therefore, the mean time of power converter to failure is found as 134005 hours from the below expression

$$MTTF = \frac{1}{\lambda_{CONVERTER}}\, hours. \quad (20)$$

The THD is computed using the standard definition

$$\text{THD} = \frac{\sqrt{V_2^2+V_3^2+V_4^2+...+V_n^2}}{V_1}\times 100\%, \quad (21)$$

where V_1 is the root mean square (RMS) value of the fundamental frequency component, and V_2, V_3 are the RMS values of the harmonic components obtained from the Fourier transform of the inverter output voltage waveform.

D. Real-Time Work of 11-Level PIU

To study the performance of the proposed inverter, the real-time implementation of the proposed PIU using the FPGA SPARTAN 6 processor for lamp load is carried out and is shown in Fig. 18.

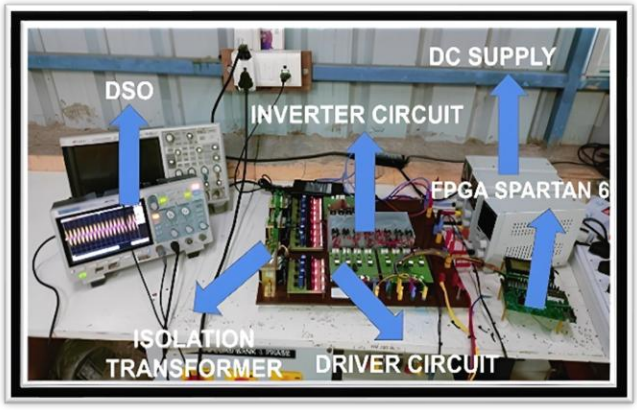
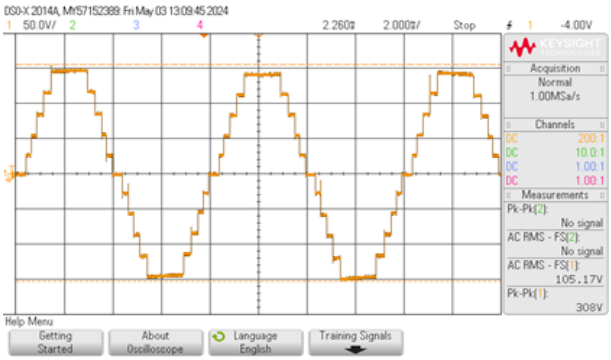


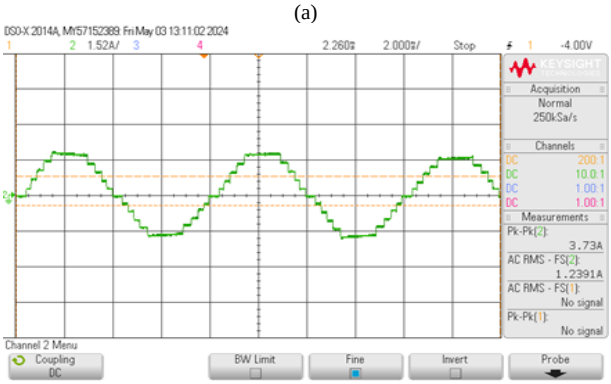
Fig. 18. Real-time work of PIU.

The hardware setup (Fig. 18) is now connected to a reactive load of R = 90 Ω, L = 40 mH and the current is seen in the DSO (Fig. 19(c)) with an output current value of 1.53 A. Figs. 20(a) and 20(b) show the output current when the PIU is subjected to a sudden change in the R and RL load.

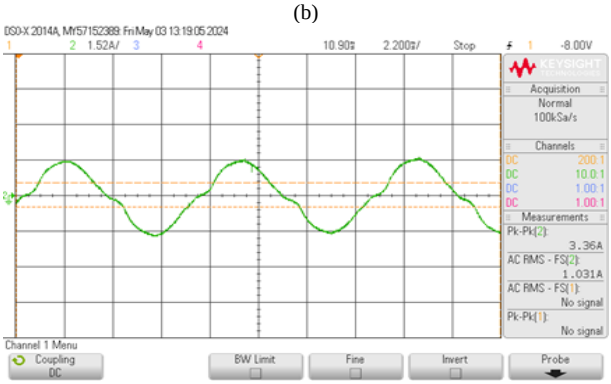
The inverter output voltage waveform is shown in Fig. 19(a). The maximum output voltage is observed as ±150 V, which satisfies the simulation results. The output current of the MLI feeding resistive load is inferred by using the current probe in the digital oscilloscope and is measured to be 1.52 A, which is shown in Fig. 19(b).



(a)

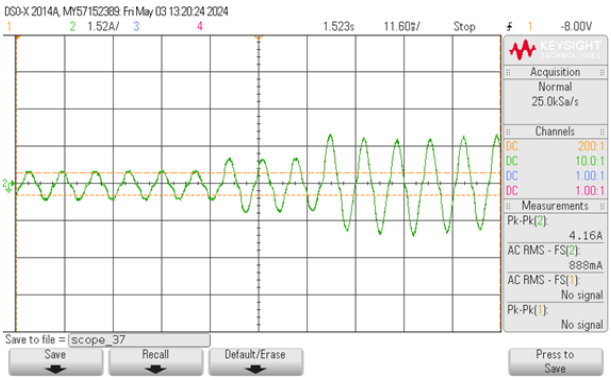


(b)

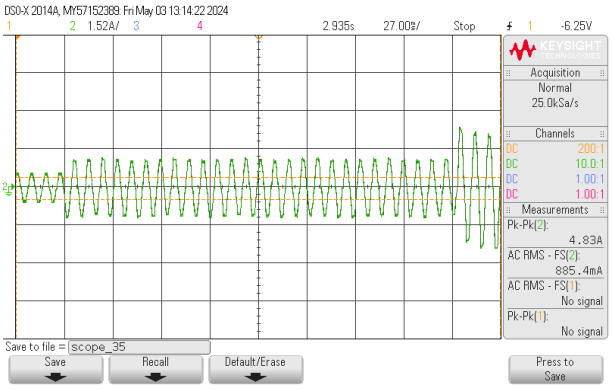


(c)

Fig. 19. (a) R and RL voltage output; (b) Output current for R load; (c) Output current for RL load.



(a)



(b)

Fig. 20. (a) Variable R - output current; (b) Variable RL - output current.

It is evident that the developed MLIs can perform well when faced with a sudden shift in load; the voltage magnitudes remain constant while the current magnitudes change with change in the loading conditions. From the above, real-time implementation and discussion, the features observed of PIU are promising.

V. CONCLUSIONS

From the study, the multilevel inverters (MLIs) can generate high-quality output voltage (V_o) with low harmonic distortion; they have become a desirable option for high-power applications. In the power sector, this technology is becoming increasingly popular for use in electric vehicles, motor drives, and renewable energy systems. Therefore, this article discusses the design features of inverters at the two, three, and higher levels used in the power industry. Furthermore, it is recommended to generate 11 voltage steps using a packed inverter unit (PIU) equipped with 11 IGBT switches and three unequal DC voltages. The amplitude of the DC sources is selected using the proposed axioms to produce larger voltage steps with the least number of circuit components. Furthermore, 11-level MLI with R/RL and variable R/RL loads are simulated and experimented with. The circuit components of the created circuit and the MLIs that are currently in use are compared. Finally, distinct performance metrics are seen from the designed inverters designed in real time when 11-level inverters are evaluated with constant and variable R/RL loads. 200 V is the output voltage produced by the 11-level MLI developed with 8.77 % THD and 95.64 % efficiency. Thus, this inverter is most suitable for renewable integration.

CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

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