

Mutator Circuit for Memcapacitor Emulator Using Operational Transconductance Amplifiers

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Abstract—In recent years, interest in memelements, including memcapacitors, has increased significantly following the realisation of memristors. This paper presents the design and implementation of a memcapacitor circuit based on operational transconductance amplifiers (OTAs). The proposed design is structured as a mutator circuit, where the second stage functions as a memristor, ultimately transforming the circuit into a memcapacitor emulator. The emulator features electronic tunability, which allows the charge value of the memcapacitor to be adjusted by modifying the capacitor in the mutator stage. The charge value of the memcapacitor can also be adjusted by varying the transconductance g_m value of the OTA active element. Additionally, the operational frequency of the memcapacitor can be varied by altering the capacitor in the second stage. An adaptive learning circuit based on the memcapacitor emulator is demonstrated to validate the circuit performance. The time response obtained when a sine signal is applied to the memcapacitor circuit, the input voltage-charge relationship, and the charge-time response obtained when a square wave is used to demonstrate its memory characteristics are provided. All simulations were conducted using LTSpice with Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm complementary metal oxide semiconductor (CMOS) process parameters. The results corroborate the effectiveness of the circuit, highlighting its potential for advanced electronic applications.

Index Terms—Mutator; Memcapacitor emulator; OTA; Electronic tunability; Memristor.

I. INTRODUCTION

After Chua [1] proposed the memristor in 1971, researchers did not show significant interest in this memelement until it was physically realised in HP laboratories by Strukov, Snider, Stewart, and Williams [2] in 2008. Subsequently, numerous studies have been conducted on memristors, focussing on various aspects such as fabrication [3]–[5], memristor emulator circuits [6]–[18], and applications of memristor-based circuits [14]–[20]. Di Ventra Pershin, and Chua [21] demonstrated that the concept of memory elements extends beyond resistive systems to include capacitive and inductive systems as well. Following this, mutator structures were introduced to convert memristors into memcapacitors and meminductors [22].

Memcapacitors establish a connection between flux and

the time integral of charge, exhibiting a pinched hysteresis loop between voltage and charge, while meminductors establish a connection between charge and the time integral of flux, displaying a pinched hysteresis loop between current and flux. However, memcapacitors and meminductors are not readily available as discrete circuit elements in the literature. This limitation has prompted researchers to explore alternative approaches. By configuring emulator circuits to mimic the behaviour of memcapacitors and meminductors, researchers can overcome fabrication challenges and explore potential applications of these intriguing devices. The literature is rich in various approaches to understanding and implementing memcapacitors and meminductors, with numerous SPICE models [23]–[28] and mutator and emulator circuits [22], [29]–[46]. SPICE models of memristors or active elements used in mutator structures are used in [22] and [29]. In other mutator structures containing memristors, numerous active and passive elements are used in both the memristor and mutator layers [30]–[32], [34].

In this paper, we propose an operational transconductance amplifier (OTA)-based memcapacitor mutator circuit. This structure consists of an active OTA element, a capacitor, a resistor, and a memristor. To utilise the same active element, we selected an OTA-based memristor as the memristor component. The memristor stage includes one OTA, a capacitor, a resistor, and a multiplier circuit. The proposed memcapacitor circuit is electronically tunable. The charge value of the memcapacitor can be adjusted by modifying the transconductance gain g_m of the OTA, as well as by changing the capacitor in the mutator stage. Additionally, the operating frequency of the memcapacitor can be tuned by altering the capacitor value in the memristor stage. By applying a sine signal to the input, we obtained a pinched hysteresis loop of the input voltage-charge characteristic of the memcapacitor for both a single memcapacitor and multiple memcapacitors connected in parallel. Furthermore, a square wave was applied to the input of the memcapacitor, and the resulting charge-time graph demonstrated the memory characteristic of the circuit. Additionally, to analyse the performance of the memcapacitor, the emulator structure was used in an adaptive learning circuit. All analyses were conducted using LTSpice with 0.18 μm Taiwan Semiconductor Manufacturing Company (TSMC) complementary metal oxide

semiconductor (CMOS) process parameters, and the results were consistent with previous memcapacitor circuits.

II. PROPOSED MUTATOR CIRCUIT

The OTA is a versatile electronic component widely used in analogue circuit design. Unlike traditional operational amplifiers, which provide a voltage output, an OTA converts an input voltage signal into an output current. The transconductance gain g_m of the OTA, defined as the ratio of the output current to the input voltage, is a key parameter and is electronically tunable. This feature allows OTAs to be employed in many electronic circuit applications. The ability to adjust the g_m value makes OTAs particularly useful in adaptive and reconfigurable circuits, including the proposed memcapacitor mutator circuit, where precise control of circuit parameters is essential. The electrical symbol and equivalent circuit of an ideal OTA are provided in Fig. 1.

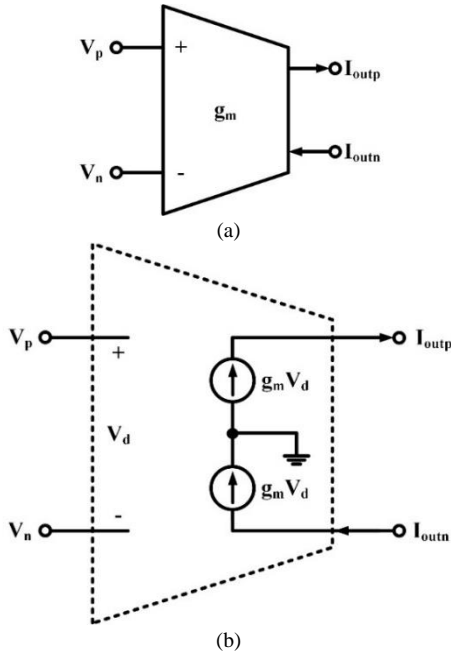


Fig. 1. (a) Electrical symbol; (b) Equivalent circuit of an ideal OTA.

Mathematically, the port relationships of the OTA can be expressed as

$$I_{\text{outp}} = -I_{\text{outn}} = g_m (V_p - V_n). \quad (1)$$

The OTA-based memcapacitor mutator structure is shown in Fig. 2. In this configuration, the first OTA-based stage functions as the mutator structure, while the second OTA-based stage acts as the memristor. The memristor structure used in the mutator circuit is based on the design proposed by Babacan, Yesil, and Kacar [10]. The proposed memcapacitor circuit utilises the ideal OTA as shown in Fig. 1. An OTA-based memristor was chosen for the mutator circuit to ensure consistency in the use of the same active element.

If the memristance value of the memristor is expressed as $M(q)$, then the V_p value for the mutator using (1) can be written as follows

$$V_p = -I_{\text{outn}} M(q) = g_m V_p M(q) - g_m V_n M(q). \quad (2)$$

When (2) is edited and rewritten,

$$V_p = \frac{g_m V_n M(q)}{g_m M(q) - 1}. \quad (3)$$

If the charge value is obtained from the input current of the memcapacitor:

$$I_{\text{in}} = I_{C1} = C_1 \frac{d(V_{\text{in}} - V_{R1})}{dt}, \quad (4)$$

$$q(t) = \int I_{\text{in}} dt = C_1 (V_{\text{in}} - V_{R1}). \quad (5)$$

The voltage on resistor R_1 is written as follows and if (1) is used,

$$V_{R1} = I_{\text{outp}} R_1 = g_m V_p R_1 - g_m V_n R_1. \quad (6)$$

If (5) is rearranged using (6),

$$q(t) = C_1 V_{\text{in}} - C_1 g_m V_p R_1 + C_1 g_m V_n R_1. \quad (7)$$

Using (3) and (7), the memcapacitance value of the circuit can be expressed as follows

$$C_M = \frac{q(t)}{V_{\text{in}}} = C_1 \left[1 + \frac{g_m R_1}{1 - g_m M(q)} \right]. \quad (8)$$

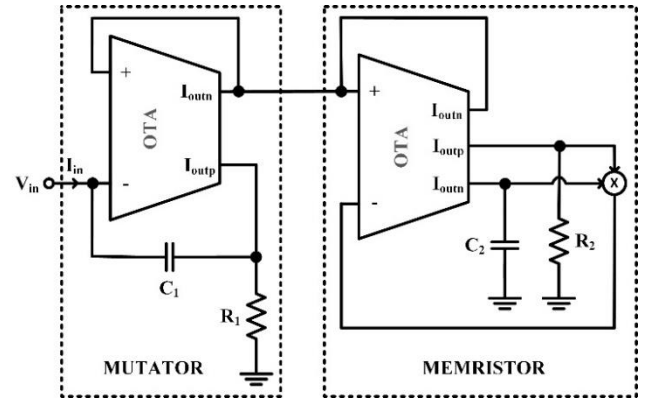


Fig. 2. Proposed memcapacitor emulator.

In the circuit provided in Fig. 2, the passive circuit elements are chosen as follows: $C_1 = 10$ pF, $C_2 = 900$ nF, $R_1 = 10$ k Ω , and $R_2 = 15$ k Ω . The transconductance gain g_m of the OTA is selected as 1.9 mS.

III. SIMULATION RESULTS

One of the key characteristics of memcapacitors is their ability to exhibit a pinched hysteresis loop when a sinusoidal signal is applied. In this study, a sinusoidal signal with an amplitude of 100 mV and a frequency of 1 kHz was applied to the proposed memcapacitor. The obtained time response of the memcapacitor and input voltage-charge characteristics are shown in Fig. 3. As depicted in Fig. 3(b), the expected pinched hysteresis loop was successfully obtained, confirming the anticipated behaviour of the proposed memcapacitor design.

Another important feature of memcapacitors is their memory capability. A pulse voltage signal was applied to the memcapacitor circuit to investigate this characteristic. The resulting time response is shown in Fig. 4. As illustrated in

the figure, the charge value of the memcapacitor resumes from where it left off after each pulse, demonstrating the memory property of the memcapacitor. This confirms that the proposed memcapacitor circuit effectively exhibits the expected memory behaviour.

The charge of a memcapacitor is directly proportional to its memcapacitance, so as the number of memcapacitors

connected in parallel increases, the total charge also increases. We compared the charge values of a single memcapacitor, two memcapacitors connected in parallel, and three memcapacitors connected in parallel. The input voltage-charge characteristics for these three cases are depicted in Fig. 5, where, as expected, the highest charge value is obtained when three memcapacitors are connected in parallel.

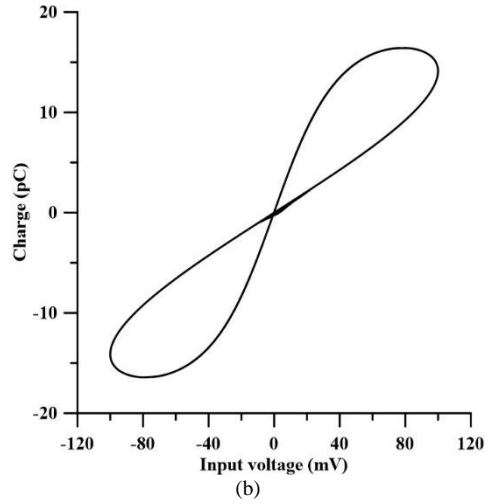
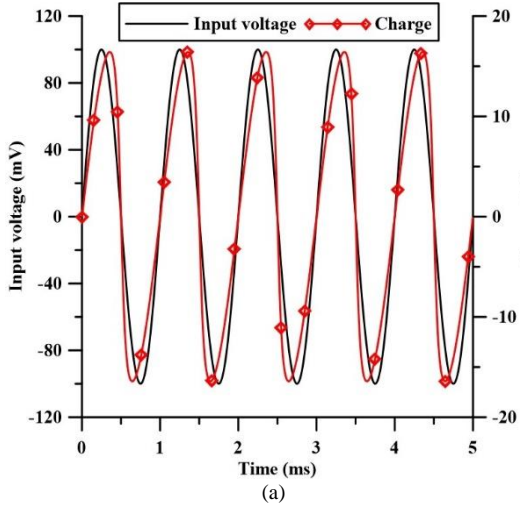


Fig. 3. (a) Time response; (b) Pinched hysteresis loop of the memcapacitor.

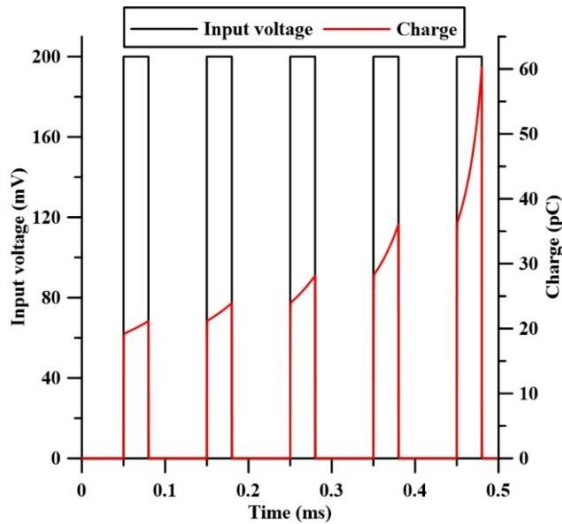


Fig. 4. Memcapacitor charge change when applied voltage pulse signal.

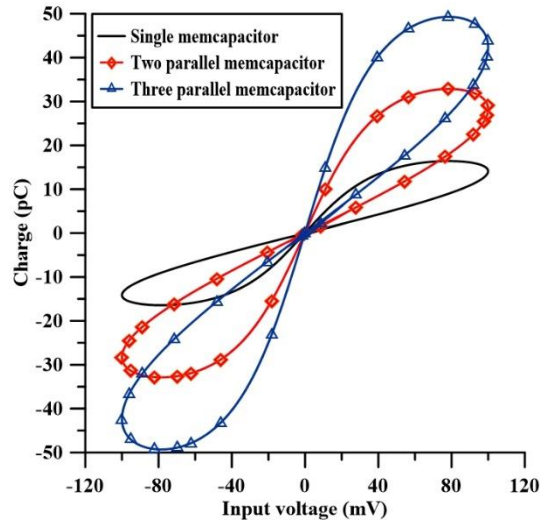
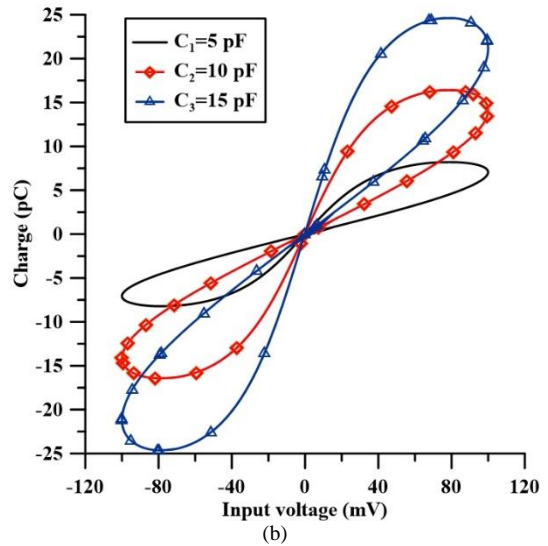
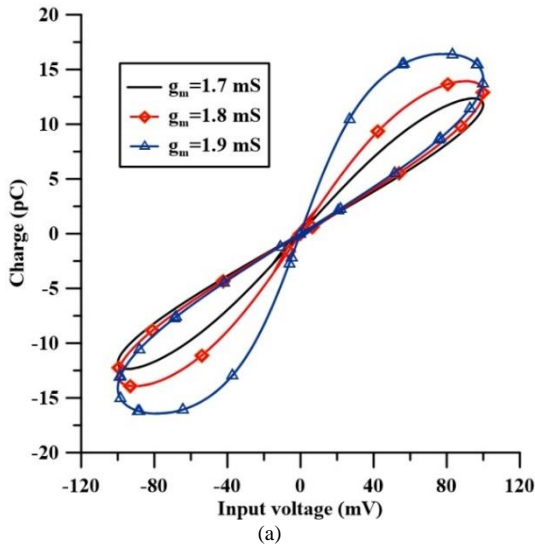


Fig. 5. The charge-voltage relationships of single, two parallel, and three parallel connected memcapacitors.



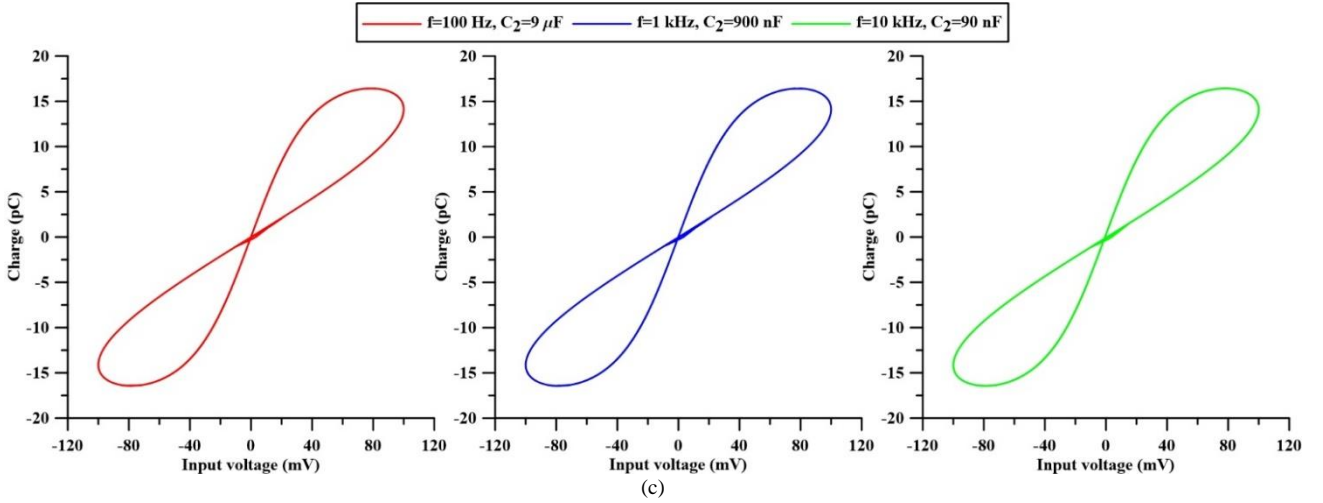


Fig. 6. Memcapacitor pinched hysteresis loops for different (a) g_m , (b) C_1 values, and (c) frequencies.

The proposed memcapacitor circuit is electronically tunable. Since it is based on an OTA, the charge value of the memcapacitor can be adjusted by changing the OTA's transconductance gain g_m . The input voltage-charge characteristics obtained for different g_m values of the OTA are shown in Fig. 6(a). Additionally, the charge value can also be adjusted by changing the capacitance value in the mutator stage of the memcapacitor circuit. The input voltage-charge characteristics obtained for different values of capacitor C_1 in the memcapacitor structure are shown in Fig. 6(b). Furthermore, the capacitance value in the memristor stage of the memcapacitor also affects the operating frequency. The circuit was operated at different frequencies for different values of the capacitor C_2 in the proposed memcapacitor structure, and the resulting input voltage-charge graphs are shown in Fig. 6(c).

IV. APPLICATION OF THE PROPOSED MEMCAPACITOR IN ADAPTIVE LEARNING CIRCUIT

The use of memelements in neural applications has become a popular research topic in recent years. To investigate the applicability of the proposed memcapacitor, the structure was used in an adaptive learning circuit to mimic amoeba behaviour [47]. Amoeba exhibits unique responses to changes in temperature. When there is any change in environmental temperature, amoebas exhibit a corresponding alteration in their locomotive speed. As the surrounding temperature varies, the movement of the amoeba also changes accordingly, and these changes accumulate over time even if the temperature changes occur at constant increments. During brief periods when the temperature remains stable, the amoeba maintains the speed it has reached since the last temperature change. This behaviour indicates a form of memory capability in amoeba. Researchers have modelled this behaviour by replacing passive elements in a series of RLC circuits with memory elements [42]–[46]. In this study, an adaptive learning circuit mimicking amoeba behaviour was implemented by replacing the capacitor in the RLC circuit with the proposed memcapacitor, as shown in Fig. 7, to demonstrate the effectiveness of the proposed memcapacitor.

The basic circuit elements used in the adaptive learning circuit are selected as follows: the resistor R is $1\text{ k}\Omega$ and the inductor L is 1 nH . Pulse signals with an amplitude of -

100 mV are applied to the input of the circuit, and the results are shown in Fig. 8.

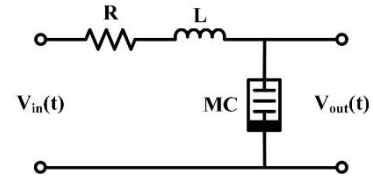


Fig. 7. Adaptive learning circuit using proposed memcapacitor.

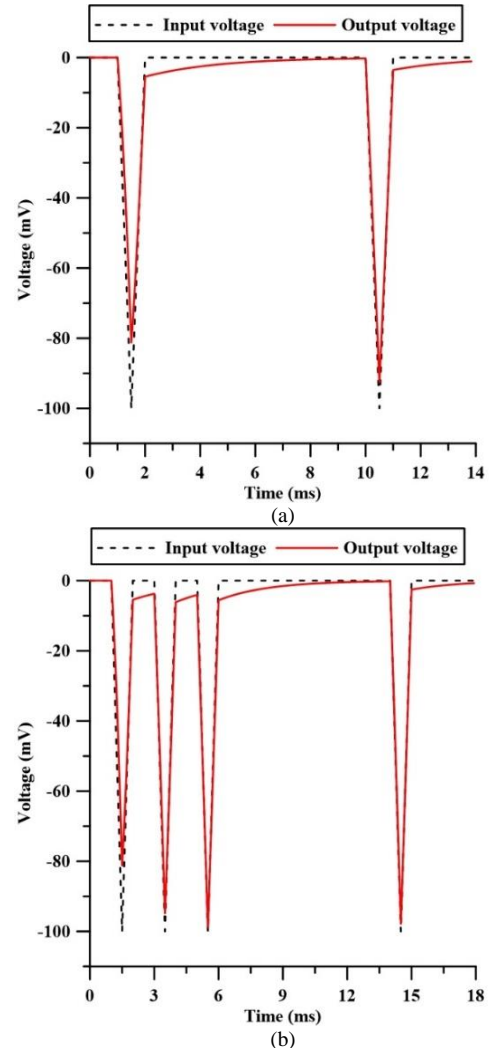


Fig. 8. Applied input voltage pulses and output responses obtained for (a) one signal and (b) three signals.

In this setup, the input signal $V_{in}(t)$ represents the change in the close environmental temperature, while $V_{out}(t)$ represents the change in the locomotive speed of the amoeba. When single pulses were applied to the circuit at 8 ms intervals, the output signal was -73.8 mV for the first pulse and -84.1 mV for the second pulse. When three pulses were applied at 1 ms intervals, the output signal dropped to -89.8 mV. After 8 ms, a single pulse was applied again and the output signal was measured as -88.9 mV. It has been observed that when multiple pulses occur consecutively, the output gradually decreases, but when a single pulse arrives after some time, the output slows down instantly. This observation confirms the circuit's ability to amoeba behaviour. From adaptive learning circuits utilising the memcapacitor, we determined that the proposed memcapacitor design is well-suited for real-time applications.

V. CONCLUSIONS

In this paper, we presented the design and implementation of a memcapacitor circuit using operational transconductance amplifiers (OTAs), structured as a mutator circuit. Our approach effectively emulates the behaviour of the memcapacitor by transforming an OTA-based memristor into a memcapacitor. The electronically tunable nature of the proposed circuit allows for precise control over the charge value by modifying the transconductance gain of the OTA or the capacitor in the mutator stage. This tunability extends to the operational frequency of the memcapacitor, which can be adjusted by varying the capacitance in the second stage.

The simulation results confirmed the theoretical expectations, demonstrating key characteristics of the memcapacitor such as the pinched hysteresis loop and the memory effect. The input voltage-charge relationship exhibited the anticipated pinched hysteresis loop when a sinusoidal input signal was applied. Additionally, the memory characteristic of the circuit was validated through the charge-time response obtained with a square-wave input, showing that the memcapacitor retains its charge value between pulses.

Furthermore, the applicability of the proposed memcapacitor in advanced electronic applications was illustrated by integrating it into an adaptive learning circuit designed to mimic amoeba behaviour. The circuit response to temperature changes, modelled as input voltage pulses, demonstrated a memory-like adaptation in the output signal, aligning with the locomotive speed adjustments observed in amoebas. Overall, the results highlight the potential of OTA-based memcapacitor circuits in various applications, including adaptive systems and neuromorphic computing.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

REFERENCES

- [1] L. Chua, "Memristor-The missing circuit element", *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507–519, 1971. DOI: 10.1109/TCT.1971.1083337.
- [2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found", *Nature*, vol. 453, no. 7191, pp. 80–83, 2008. DOI: 10.1038/nature06932.
- [3] T. Prodromakis, K. Michelakis, and C. Toumazou, "Fabrication and electrical characteristics of memristors with TiO_2/TiO_{2+x} active layers", in *Proc. of 2010 IEEE International Symposium on Circuits and Systems*, 2010, pp. 1520–1522. DOI: 10.1109/ISCAS.2010.5537379.
- [4] N. Duraisamy, N. M. Muhammad, H.-C. Kim, J.-D. Jo, and K.-H. Choi, "Fabrication of TiO_2 thin film memristor device using electrohydrodynamic inkjet printing", *Thin Solid Films*, vol. 520, no. 15, pp. 5070–5074, 2012. DOI: 10.1016/j.tsf.2012.03.003.
- [5] Y. Babacan, A. Yesil, and F. Gul, "The fabrication and MOSFET-only circuit implementation of semiconductor memristor", *IEEE Transactions on Electron Devices*, vol. 65, no. 4, pp. 1625–1632, 2018. DOI: 10.1109/TED.2018.2808530.
- [6] M. Mahvash and A. C. Parker, "A memristor SPICE model for designing memristor circuits", in *Proc. of 2010 53rd IEEE International Midwest Symposium on Circuits and Systems*, 2010, pp. 989–992. DOI: 10.1109/MWSCAS.2010.5548803.
- [7] H. Kim, M. Pd. Sah, C. Yang, S. Cho, and L. O. Chua, "Memristor emulator for memristor circuit applications", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 10, pp. 2422–2431, 2012. DOI: 10.1109/TCSI.2012.2188957.
- [8] C. Sánchez-López, J. Mendoza-Lopez, M. A. Carrasco-Aguilar, and C. Muñoz-Montero, "A floating analog memristor emulator circuit", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 5, pp. 309–313, 2014. DOI: 10.1109/TCSII.2014.2312806.
- [9] C. Yang, H. Choi, S. Park, M. Pd Sah, H. Kim, and L. O. Chua, "A memristor emulator as a replacement of a real memristor", *Semiconductor Science and Technology*, vol. 30, no. 1, art. 015007, 2015. DOI: 10.1088/0268-1242/30/1/015007.
- [10] Y. Babacan, A. Yesil, and F. Kacar, "Memristor emulator with tunable characteristic and its experimental results", *AEU - International Journal of Electronics and Communications*, vol. 81, pp. 99–104, 2017. DOI: 10.1016/j.aeue.2017.07.012.
- [11] A. Yesil, Y. Babacan, and F. Kacar, "Electronically tunable memristor based on VDCC", *AEU - International Journal of Electronics and Communications*, vol. 107, pp. 282–290, 2019. DOI: 10.1016/j.aeue.2019.05.038.
- [12] A. Yesil, Y. Babacan, and F. Kaçar, "Design and experimental evolution of memristor with only one VDTA and one capacitor", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 38, no. 6, pp. 1123–1132, 2019. DOI: 10.1109/TCAD.2018.2834399.
- [13] S. S. Prasad, P. Kumar, and R. K. Ranjan, "Resistorless memristor emulator using CFTA and its experimental verification", *IEEE Access*, vol. 9, pp. 64065–64075, 2021. DOI: 10.1109/ACCESS.2021.3075341.
- [14] A. Yesil, Y. Babacan, and F. Kaçar, "A new DDCC based memristor emulator circuit and its applications", *Microelectronics*, vol. 45, no. 3, pp. 282–287, 2014. DOI: 10.1016/j.mejo.2014.01.011.
- [15] Y. Babacan and F. Kacar, "FCS based memristor emulator with associative learning circuit application", *IU-Journal of Electrical & Electronics Engineering*, vol. 17, no. 2, pp. 3433–3437, 2017.
- [16] R. K. Ranjan, N. Raj, N. Bhuwal, and F. Khateb, "Single DVCCTA based high frequency incremental/decremental memristor emulator and its application", *AEU - International Journal of Electronics and Communications*, vol. 82, pp. 177–190, 2017. DOI: 10.1016/j.aeue.2017.07.039.
- [17] M. S. Feali, A. Ahmadi, and M. Hayati, "Implementation of adaptive neuron based on memristor and memcapacitor emulators", *Neurocomputing*, vol. 309, pp. 157–167, 2018. DOI: 10.1016/j.neucom.2018.05.006.
- [18] V. Saxena, "A compact CMOS memristor emulator circuit and its applications", in *Proc. of 2018 IEEE 61st International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2018, pp. 190–193. DOI: 10.1109/MWSCAS.2018.8624008.
- [19] S. Wen, X. Xie, Z. Yan, T. Huang, and Z. Zeng, "General memristor with applications in multilayer neural networks", *Neural Networks*, vol. 103, pp. 142–149, 2018. DOI: 10.1016/j.neunet.2018.03.015.
- [20] H. Lin, C. Wang, Q. Hong, and Y. Sun, "A multi-stable memristor and its application in a neural network", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 3472–3476, 2020. DOI: 10.1109/TCSII.2020.3000492.
- [21] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: Memristors, memcapacitors, and meminductors", *Proceedings of the IEEE*, vol. 97, no. 10, pp. 1717–1724, 2009. DOI: 10.1109/JPROC.2009.2021077.
- [22] D. Biolek, V. Biolková, and Z. Kolka, "Mutators simulating memcapacitors and meminductors", in *Proc. of 2010 IEEE Asia Pacific Conference on Circuits and Systems*, 2010, pp. 800–803. DOI: 10.1109/APCCAS.2010.5774993.

- [23] D. Biolek, Z. Biolek, and V. Biolkova, "SPICE modelling of memcapacitor", *Electronics Letters*, vol. 46, no. 7, pp. 520–522, 2010. DOI: 10.1049/el.2010.0358.
- [24] D. Biolek, Z. Biolek, and V. Biolkova, "Behavioral modeling of memcapacitor", *Radionengineering*, vol. 20, no. 1, pp. 228–233, 2011.
- [25] D. Biolek, M. Di Ventra, and Y. V. Pershin, "Reliable SPICE simulations of memristors, memcapacitors and meminductors", 2013. DOI: 10.48550/arXiv.1307.2717.
- [26] D. Biolek, Z. Biolek, and V. Biolková, "PSPICE modeling of meminductor", *Analog Integrated Circuits and Signal Processing*, vol. 66, no. 1, pp. 129–137, 2011. DOI: 10.1007/s10470-010-9505-5.
- [27] R. Sotner *et al.*, "On the performance of electronically tunable fractional-order oscillator using grounded resonator concept", *AEU - International Journal of Electronics and Communications*, vol. 129, article 153540, 2021. DOI: 10.1016/j.aeue.2020.153540.
- [28] H. Wang, X. Wang, C. Li, and L. Chen, "SPICE mutator model for transforming memristor into meminductor", *Abstract and Applied Analysis*, vol. 2013, art. ID 281675, pp. 1–5, 2013. DOI: 10.1155/2013/281675.
- [29] D. Biolek and V. Biolkova, "Mutator for transforming memristor into memcapacitor", *Electronics Letters*, vol. 46, no. 21, p. 1, 2010. DOI: 10.1049/el.2010.2309.
- [30] D. Yu, Y. Liang, H. H. C. Iu, and L. O. Chua, "A universal mutator for transformations among memristor, memcapacitor, and meminductor", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 10, pp. 758–762, 2014. DOI: 10.1109/TCSII.2014.2345305.
- [31] M. Pd. Sah, R. K. Budhathoki, C. Yang, and H. Kim, "A mutator-based meminductor emulator circuit", in *Proc. of 2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2014, pp. 2249–2252. DOI: 10.1109/ISCAS.2014.6865618.
- [32] M. Pd. Sah, R. K. Budhathoki, C. Yang, and H. Kim, "Mutator-based meminductor emulator for circuit applications", *Circuits, Systems, and Signal Processing*, vol. 33, no. 8, pp. 2363–2383, 2014. DOI: 10.1007/s00034-014-9758-9.
- [33] Z. G. Ç. Taşkıran, M. Sağbaş, U. E. Ayten, and H. Sedef, "A new universal mutator circuit for memcapacitor and meminductor elements", *AEU - International Journal of Electronics and Communications*, vol. 119, art. 153180, 2020. DOI: 10.1016/j.aeue.2020.153180.
- [34] D. Yu, X. Zhao, T. Sun, H. H. C. Iu, and T. Fernando, "A simple floating mutator for emulating memristor, memcapacitor, and meminductor", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 7, pp. 1334–1338, 2020. DOI: 10.1109/TCSII.2019.2936453.
- [35] M. Z. Hosbas, F. Kaçar, and A. Yesil, "Memcapacitor emulator using VDTA-memristor", *Analog Integrated Circuits and Signal Processing*, vol. 110, pp. 361–370, 2022. DOI: 10.1007/s10470-021-01974-0.
- [36] M. P. Sah, C. Yang, R. K. Budhathoki, H. Kim, and H. J. Yoo, "Implementation of a memcapacitor emulator with off-the-shelf devices", *Elektronika ir Elektrotechnika*, vol. 19, no. 8, pp. 54–58, 2013. DOI: 10.5755/j01.eee.19.8.2673.
- [37] D. S. Yu, Y. Liang, H. Chen, and H. H. C. Iu, "Design of a practical memcapacitor emulator without grounded restriction", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 4, pp. 207–211, 2013. DOI: 10.1109/TCSII.2013.2240879.
- [38] M. Konal and F. Kacar, "Electronically tunable meminductor based on OTA", *AEU - International Journal of Electronics and Communications*, vol. 126, art. 153391, 2020. DOI: 10.1016/j.aeue.2020.153391.
- [39] M. Konal, F. Kacar, and Y. Babacan, "Electronically controllable memcapacitor emulator employing VDCCs", *AEU - International Journal of Electronics and Communications*, vol. 140, art. 153932, 2021. DOI: 10.1016/j.aeue.2021.153932.
- [40] M. Konal and F. Kacar, "Electronically tunable memcapacitor emulator based on operational transconductance amplifiers", *Journal of Circuits, Systems, and Computers*, vol. 30, no. 5, p. 2150082, 2021. DOI: 10.1142/S0218126621500821.
- [41] A. Yesil and Y. Babacan, "Electronically controllable memcapacitor circuit with experimental results", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 4, pp. 1443–1447, 2021. DOI: 10.1109/TCSII.2020.3030114.
- [42] J. Vista and A. Ranjan, "Simple charge controlled floating memcapacitor emulator using DXCCDITA", *Analog Integrated Circuits and Signal Processing*, vol. 104, no. 1, pp. 37–46, 2020. DOI: 10.1007/s10470-020-01650-9.
- [43] A. Singh and S. K. Rai, "VDCC-based memcapacitor/meminductor emulator and its application in adaptive learning circuit", *Iranian Journal of Science and Technology, Transactions of Electrical Engineering*, vol. 45, no. 4, pp. 1151–1163, 2021. DOI: 10.1007/s40998-021-00440-x.
- [44] K. Bhardwaj and M. Srivastava, "New multiplier-less compact tunable charge-controlled memelement emulator using grounded passive elements", *Circuits, Systems, and Signal Processing*, vol. 41, no. 5, pp. 2429–2465, 2022. DOI: 10.1007/s00034-021-01895-3.
- [45] K. Bhardwaj and M. Srivastava, "Compact floating dual memelement emulator employing VDIBA and OTA: A novel realization", *Circuits, Systems, and Signal Processing*, vol. 41, no. 11, pp. 5933–5967, 2022. DOI: 10.1007/s00034-022-02067-7.
- [46] M. O. Korkmaz, Y. Babacan, and A. Yesil, "CCII-and OTA-based tunable memcapacitor emulator circuits without using passive elements", *Circuits, Systems, and Signal Processing*, vol. 43, pp. 4093–4120, 2024. DOI: 10.1007/s00034-024-02681-7.
- [47] Y. V. Pershin, S. La Fontaine, and M. Di Ventra, "Memristive model of amoeba learning", *Physical Review E*, vol. 80, p. 021926, 2009. DOI: 10.1103/PhysRevE.80.021926.



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