Evaluation and Implementation of EMI/EMC Compliance for a Proposed Power Electronics-Based Converter Topology for Electric Vehicles

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Abstract—**The demand for high-gain, efficient, and cost-effective power converters with simple control mechanisms to connect electric vehicle batteries to the grid is increasing. This study introduces a switched capacitor-based power boost converter circuit to meet these needs. The minimal number of power switches in the circuit simplifies control operations and improves practical applicability. The proposed converter boosts the battery pack voltage by a factor of 5 and 11 for duty ratios of 0.5 and 0.8, respectively, which is significant compared to conventional boost converters.**

However, designing an electromagnetic interference (EMI) filter is crucial when a power converter board requires the application of a wide range of switching frequencies to enhance electromagnetic compatibility (EMC) immunity. Therefore, as the next step, the EMI/EMC filter design stages were discussed for the proposed converter. For this purpose, 15 printed circuit board (PCB) design rules were checked using the Altium Designer EMI Design Rule Checker, and board EMI/EMC compatibility was analysed. The resonance between the power and ground layers in the PCB was assessed using the plane resonance analyser. The results of simulation and laboratory tests are presented, which confirms the theoretical studies. On the basis of the software results, the points on the electronic board most susceptible to visual interferences have been identified. To minimise these EMI/EMC errors, it is suggested to add electronic components, such as capacitors, at these points according to mathematical and software findings.

Index Terms—**Vehicle-to-Grid (V2G); Electric vehicle; DC-DC converter; Reliability; Electromagnetic interference (EMI).**

I. INTRODUCTION

The demand for DC-DC boost converters connected to electric vehicle batteries is increasing for energy conversion and transfer to the grid. This topic is known as vehicle-to-grid (V2G) technology [1], [2]. Converters with simple design and minimal current and voltage stress, especially for semiconductor components, are preferred [3], [4]. The key features of these converters include high efficiency, straightforward control circuits, and rapid performance. In

[3], a straightforward cascaded converter is introduced designed to boost voltage while reducing the stress on the main power switch and minimising the ripple of the input current. In [4], a soft-switched topology is proposed to reduce switching losses in semiconductor devices. Although successful results have been demonstrated, the mathematical analysis of the soft switching remains complex.

DC-DC boost converter circuits based on switched capacitor cell technology, utilising fewer power switch components simplify the control operations and improve practical applicability of the designed converter [5]–[7]. One of the primary advantages of switched-capacitor-based converter topologies is their ability to enhance voltage without the need for additional switches. This is achieved by the sequence of charging and discharging the capacitors at typically high frequencies, which is managed through the activation and deactivation of the diodes. As a result, voltage boosting is accomplished simply. Additionally, the overall cost of the converter topology is reasonable because inexpensive components are used.

Resonant-based switched capacitor converters are also known for their ability to provide high voltage gains [8]. However, a disadvantage of these converters is that the continuous regulation range is typically limited to a narrow band of switching frequencies.

In [9], a converter topology is presented that combines switched capacitor and coupled-inductor cells, capable of recycling the output capacitor using the energy leakage from the inductor. This process reduces the reverse recovery time for the converter diodes, thus enhancing the overall efficiency of the converter.

Since the goal in switched-capacitor-based converters is to continuously enhance the voltage at the load side, the current level for the same power output is reduced on the output side and other semiconductor devices in the intermediate layers of the converter. In [10], a type of these converters is introduced that minimises current ripples in the converter components by using a low-volume choke capable of operating in discontinuous current mode (DCM).

This study introduces a DC-DC boost converter circuit based on a novel and simple switched-capacitor cell

technology, which uses only one power switch component. In the proposed converter, integrating the corresponding voltage enhancer cell into a boost converter circuit reduces the voltage stress on the main circuit switch and significantly increases the battery voltage.

The proposed converter increases the battery pack voltage five times and 11 times for duty ratios of 0.5 and 0.8, respectively. On the contrary, a conventional converter boosts the voltage to twice and five times the battery voltage for the same duty ratios. This demonstrates the significant impact of the used SC cell on voltage enhancement, despite the proposed cell employing only three diodes and two capacitors, which is one of the novel aspects of the suggested topology.

Additionally, an LC filter can be implemented on the output side of the converter to smooth the load current and stabilise the generated voltage.

Another important consideration for the proposed converter, before it is applied to a battery pack, is equipping the converter topology with an electromagnetic interference (EMI) filter on both the input and output sides in simulation by applying designer software. EMI occurs when devices interact with each other or their surroundings, leading to disruption. Essentially, EMI is the electromagnetic energy emitted by one device that interferes with the performance of another. With the advancement of technology, EMI has become a significant and growing form of environmental pollution [11], [12]. Therefore, EMI tests are important issues that should be considered when designing a printed circuit board (PCB) [13]. For example, in [12], a single-stage EMI filter is developed by integrating a differential mode filter that provides equal attenuation to both differential mode and common mode noise at the switching frequency. Internal and external interferences, arising from both near-field and far-field sources, are represented as two distinct random voltage sources in the model in [13]. Midpoints interconnection is presented in [14] that can reduce the common mode noise up to 30 dB and realise the dc-link voltage auto-balance at the same time. A volume reduction model of common-mode inductors with chaotic pulse width modulation is used in [15] to minimise the EMI noises.

The PCB design for the relevant circuit was carried out using Altium Designer. Following the design, the EMI Design Rule Checker programme was used to analyse 15 rules to ensure the board's EMI/Electromagnetic Compatibility (EMC). The 15 rule control elements in EMIStream are based on extensive experience with EMI suppression countermeasures. This approach aims to avoid high testing costs and significant time losses.

According to the test results, the resonance map between the Power/Ground plane does not pose a risk across the board. A spectrum graph presented in the study shows the maximum voltage level for each frequency, with peaks at 150 MHz and 350 MHz exceeding -10 dB. To mitigate the resonance between planes, we placed a capacitor in the resonance region.

Section II describes the proposed converter topology and its operating principles. Section III details the EMI/EMC tests and their results. Sections IV and V provide the discussion and conclusions.

II. THE PROPOSED CONVERTER AND WORKING PRINCIPLES

The proposed battery-connected boost converter is depicted in Fig. 1(a). This illustration highlights that the proposed converter integrates only one power switch, thereby minimising the complexity of the converter topology and control circuit. Initially, the primary boost converter elevates the battery voltage, after which the switched capacitor cell further increases the voltage across capacitor C_2.

Analysing the operation of a switching converter necessitates examining two distinct time intervals: when the switch is connected and when it is disconnected. Figure 1(b) illustrates the state of the elements of the converter when the switch is connected. As depicted, power diodes D_2 and D_4 become forward-biased and consequently short-circuit, while diodes D_1 and D_3 are disconnected. During the subsequent time interval that is shown in Fig. 1(c), the statuses of these diodes change accordingly. The operational conditions of each working mode are elaborated on in detail.
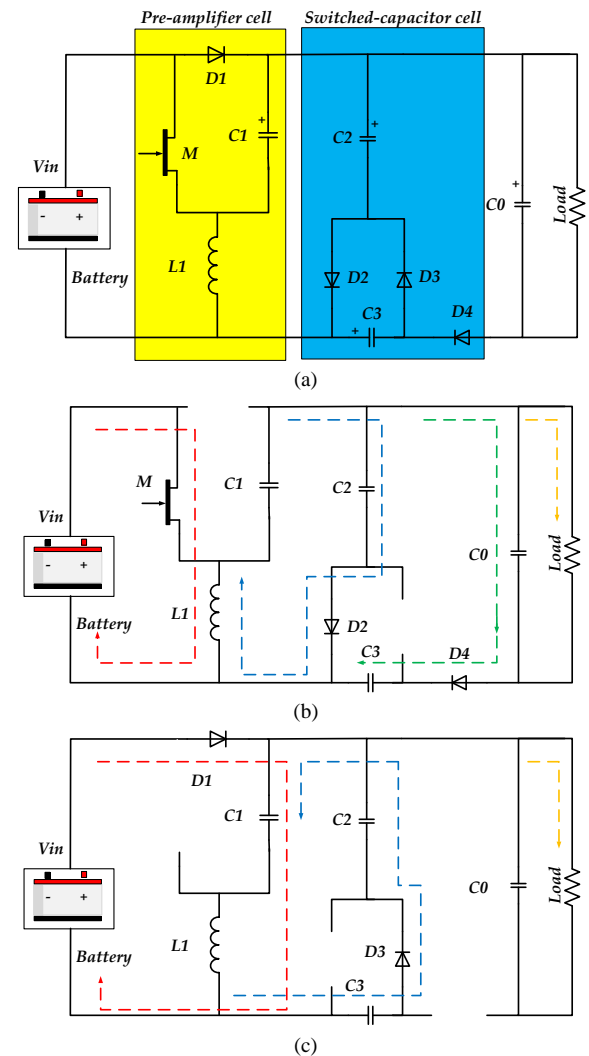

Fig. 1. (a) The proposed power converter topology, and semiconductor devices status and topology of the converter under the time durations in which the switch M is (b) connected and (c) disconnected.

According to Fig. 1(b), when the switch is connected, the inductor L_1 begins to charge. Consequently, the voltage across the inductor remains equal to the input voltage

$$V_{L1} = V_{in}. \tag{1}$$

According to Fig. 1(c), when the switch is disconnected, the voltage across the inductor L_1 starts to discharge and can be calculated using (2)

$$V_{L1} = V_{in} - V_{C1}. \qquad (2)$$

Since the total voltage across the inductor is equal to zero for a time period, it can be expressed as

$$\int_0^{DT} (V_{in})\, dt + \int_{DT}^{T} (V_{in} - V_{C1})\, dt = 0. \qquad (3)$$

This equation represents the voltage across capacitor C_1:

$$V_{C1} = \frac{V_{in}}{(1-D)}. \qquad (4)$$

Figure 1(b) shows that

$$V_{C2} = V_{in} + V_{C1} \rightarrow V_{C2} = V_{in}\frac{(2-D)}{(1-D)}. \qquad (5)$$

To find the voltage on capacitor C_3, Fig. 1(c) can be used

$$V_{C3} = V_{C2} - V_{in} = V_{in}\frac{(2-D)}{(1-D)} - V_{in} = V_{in}\frac{1}{(1-D)}. \qquad (6)$$

The voltage on output capacitor is equal to

$$V_{C0} = V_{C2} + V_{C3} \rightarrow V_{C0} = V_{in}\frac{(3-D)}{(1-D)}. \qquad (7)$$

Therefore, the gain of the proposed converter G, can be obtained as follows

$$G = \frac{V_0}{V_i} = \frac{3-D}{1-D}. \qquad (8)$$

Figure 2 clearly illustrates the gain of the proposed converter compared to the traditional boost converter. For instance, at a duty ratio of 0.5, the output voltage of the proposed converter is seven times the input battery voltage, while the output of the classic boost converter is only twice the input voltage, which is a significant difference.
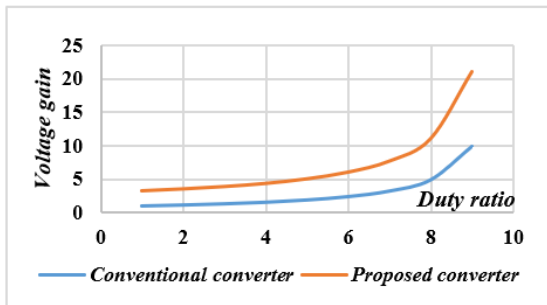

Fig. 2. Comparison of the voltage gain between the proposed and conventional boost converter configurations.

The maximum voltage on the switch can be obtained through

$$V_{M(off)} = V_{C1} = \frac{V_{in}}{(1-D)}. \qquad (9)$$

Equation (9) highlights that despite the significantly higher gain of the proposed converter compared to a conventional boost converter, the switch experiences similar voltage stresses. This parameter is crucial, as it indicates the acceptable reliability of the proposed converter for use in medium or high-power electric vehicles (EV) applications. In this topology, the voltage stresses are transferred to capacitors rather than being absorbed by semiconductor devices.
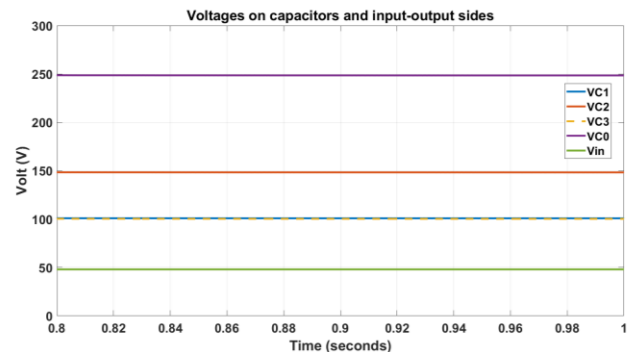
An important aspect and feature of a converter that is always considered is the reduction of voltage stresses. According to Figs. 1(b) and 1(c), the voltage stress on diodes D_1 to D_4 can be expressed and calculated as follows:

$$V_{D1} = -V_{C1} = -\frac{V_{in}}{(1-D)}, \qquad (10)$$

$$V_{D2} = V_{D3} = -V_{C3} = -\frac{V_{in}}{(1-D)}, \qquad (11)$$

$$V_{D4} = V_{C2} - V_{C0} = -\frac{V_{in}}{(1-D)}. \qquad (12)$$

These results are interesting because all the diodes experience the same voltage stress as those in a classic boost converter, yet the load output nodes achieve a voltage that is 3.5 times greater. Figure 3(a) illustrates the input side of the battery pack and the voltage values generated on the C_1 to C_0 capacitors in a duty ratio of 0.5. This figure validates the accuracy of (4) through (7). Additionally, the voltage stress on the switch and diodes D_1 to D_4 is measured and presented in Fig. 3(b). This figure demonstrates that (9) through (12) have been accurately calculated. For instance, the maximum voltage of nearly 100 V appears on the drain-source pin of the metal-oxide-semiconductor field-effect transistor (MOSFET), and all diodes experience the same voltage. Another confirmation of this figure is that when switch M is activated, diodes D_2 and D_4 are also activated while diodes D_1 and D_3 are deactivated, and vice versa. The current waveforms for the input source, switch M, and inductor L_1 are shown in Fig. 3(c). This figure verifies that switch M is activated during the intervals when diode D_1 is deactivated, as previously illustrated in Figs. 1(b) and 1(c). Additionally, the current waveform for inductor L_1 indicates that when switch M is activated, a positive voltage is applied to the inductor, causing it to charge.
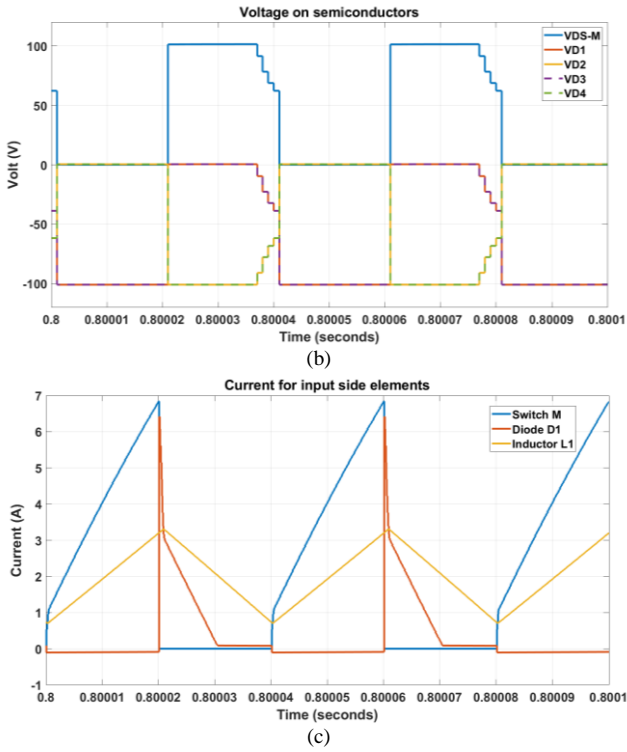

(a)

(b)

(c)

Fig. 3. Simulation results: (a) Input-output voltages and voltage on all capacitors; (b) Drain-source and anode-cathode voltages on switch and diodes; (c) Current for input side components.

On the contrary, when the switch is deactivated, a negative voltage is applied to the inductor, causing it to discharge. The state of the current in the inductor further confirms the accuracy of Figs. 1(b) and 1(c) and the theoretical operation of the converter.

In the laboratory, a workbench was set up to test the prototype power converter. Figure 4(a) shows the hardware undergoing experimental tests. Several practical measurements are provided in this subsection. Figure 4(b) shows the gate-source and drain-source voltages of transistor M. The switching frequency was set to 25 kHz as is the same as the cutoff frequency of the proposed electromagnetic interference (EMI) filter. This figure clearly demonstrates that when positive pulses reach the gate of the transistor, it activates and deactivates otherwise. The maximum voltage on the drain-source pins is reported to be 100 V, which was predictable for a duty ratio of 0.5 as theoretically presented in (9).
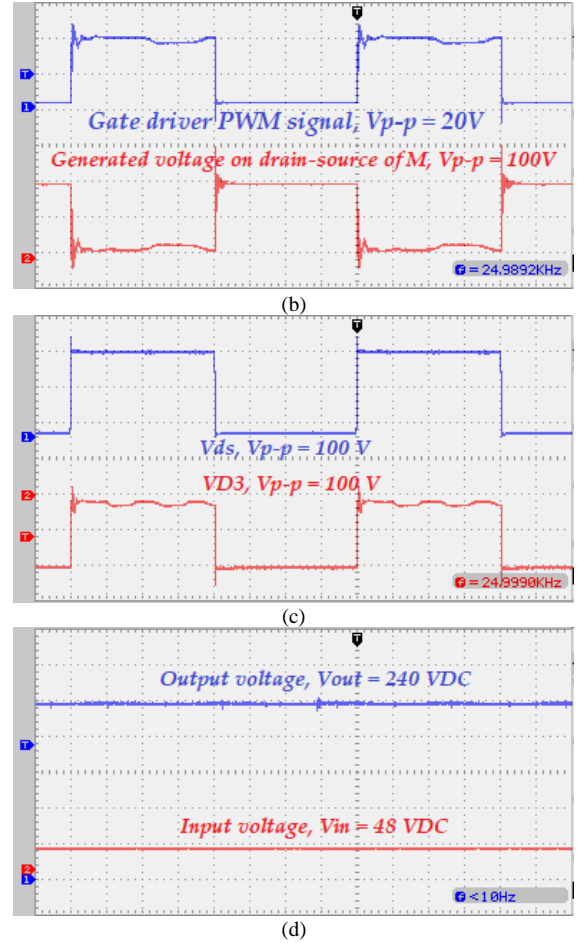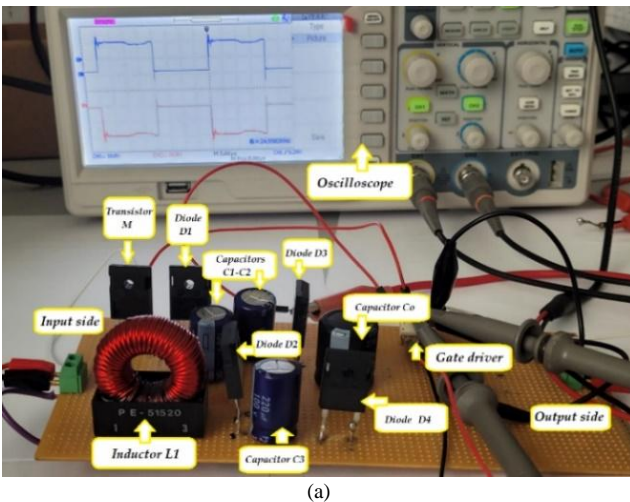

(a)

(b)

(c)

(d)

Fig. 4. (a) Laboratory workbench; (b) Gate-source and drain-source voltages for the switch M; (c) Switch state and diode D3 under the switching conditions; (d) Converter input-output voltages.

Figure 4(c) reports the voltage across diode D_3 when the switch is activated. This figure shows that the maximum $2V_{in}$ for a duty ratio of 0.5 drops across diode D_3, confirming (12). It also indicates that this diode and transistor are activated asynchronously.

Figure 4(d) presents the input and output voltages. For an input voltage of 48 V, around 240 VDC is obtained on the load side, confirming the correctness of (8), which is the most significant outcome of this study.

A. Efficiency Calculation

To calculate the power losses and efficiency of the proposed converter, all types of losses, including dynamic losses for all semiconductor devices and passive elements, as well as switching power losses for semiconductor devices, must be calculated separately. Afterward, the efficiency diagram can be presented. This converter consists of one power switch, four power diodes, and one inductor. The dynamic power losses for the capacitors are negligible and can be ignored with a proper approximation.

B. Loss Calculation for Power Switch

The relationship between the input and output currents for the proposed converter can be expressed as follows

$$V_{in}I_{in} = V_oI_o \rightarrow I_{in} = \frac{V_oI_o}{V_{in}} \rightarrow \frac{I_o}{I_{in}} = \frac{V_{in}}{V_o} = \frac{1-d}{3-d} \rightarrow$$

$$\rightarrow I_{in} = \frac{1-d}{3-d}I_o. \tag{13}$$

25

The root mean square (RMS) value of the switch current, considering the input and output voltage and current equations, can be obtained as follows

$$I_{S,rms} = \sqrt{\frac{1}{T}\int_0^{DT}(I_{in})^2\,dt} = \sqrt{\frac{1}{T}\int_0^{DT}\left(\left(\frac{1-d}{3-d}\right)I_o\right)^2 dt}$$

$$I_{S,rms} = \sqrt{\frac{1}{T}\int_0^{DT}(I_{in})^2\,dt} =$$

$$= \sqrt{\left(\frac{(1-d)}{(3-d)}I_o\right)^2 \frac{dT}{T}} = \sqrt{\frac{(1-d)^2}{(3-d)^2}I_o^2 d} = \sqrt{d}\,\frac{(1-d)}{(3-d)}I_o. \quad (14)$$

To calculate the dynamic losses of the switch $P_{r_{DS}}$,

$$P_{r_{DS}} = r_{DS}I_{S,rms}^2 = r_{DS}\left(\sqrt{d}\,\frac{(1-d)}{(3-d)}I_o\right)^2 = r_{DS}\times d\times\left(\frac{1-d}{3-d}\right)I_o^2 \rightarrow$$

$$\rightarrow P_{r_{DS}} = r_{DS}\times d\times\left(\frac{1-d}{3-d}\right)I_o^2. \quad (15)$$

r_{DS} R presents the internal resistance of the switch when is activated. The switching losses for this switch can be obtained as

$$P_{SW} = f_s C_s V_s^2 = f_s C_s\left(\frac{V_{in}}{1-d}\right)^2. \quad (16)$$

In (16), f_s, C_s, and V_s, respectively, present the switching frequency, parasitic capacitor of the drain-source pins, and voltage stress across the switch pins. Total power losses can be obtained as follows

$$P_{switch} = P_{r_{DS}} + \frac{P_{SW}}{2}. \quad (17)$$

C. Loss Calculation for Power Diodes

The RMS current for the diode D_1 is as follow

$$I_{D1,rms} = \sqrt{1-d}\,\frac{(1-d)}{(3-d)}I_o. \quad (18)$$

By calculating the RMS current for diode D₁, the dynamic power loss value for this diode can be presented

$$p_{dyn,D_1} = R_{F_1}I_{D_1,rms}^2 = R_{F_1}\left(\frac{(1-d)^3}{(3-d)^2}\right)I_o^2. \quad (19)$$

Since the current for diodes D_2 and D_3 is equal to I_{C2} for $(0-DT)$ and $(DT-T)$ time intervals, respectively, and I_{D_4} is equal to I_{C_3} for $(0-DT)$ time, the dynamic losses for diodes D_2, D_3, and D_4, respectively, are:

$$P_{dyn,D_2} = R_{F_2}I_{D_2,rms}^2 = R_{F_2}\times\sqrt{\frac{1}{T}\int_0^T(I_{C2})^2\,dt}, \quad (20)$$

$$P_{dyn,D_3} = R_{F_3}I_{D_3,rms}^2 = R_{F_3}\times\sqrt{\frac{1}{T}\int_{DT}^T(I_{C2})^2\,dt}, \quad (21)$$

$$P_{dyn,D_4} = R_{F_4}I_{D_4,rms} =$$

$$= R_{F_4}\times\sqrt{\frac{1}{T}\int_0^{DT}(I_{C3})^2\,dt}, \quad (22)$$

In these equations, R_{F_2} to R_{F_4} are the dynamic internal resistance of the diodes. Also, the switching losses of these diodes with V_{F_X} that indicated the forward bias diode voltage drop value, can be presented by

$$P_{SW,D_1} = V_{F_X}I_{D_X,ave}. \quad (23)$$

In recent equation, $I_{D_X,ave}$ presents the average current for each diode.

D. Loss Calculation for the Inductor

The RMS values of the currents for inductor L_1, is

$$I_{L_1,rms} = \frac{1-d}{3-d}I_o. \quad (24)$$

R_{L_1} is the internal resistances of the inductor L_1. So, the dynamic losses for this inductor can be obtained as follows

$$P_{rL_1} = R_{L_1}I_{L_1,rms}^2 = R_{L_1}\left(\frac{1-d}{3-d}\right)^2 I_o^2. \quad (25)$$

Therefore, by considering the calculated power losses through the presented equation, the total power loss equation can be presented as follows

$$P_{Loss} = P_{switch} + P_{D_1-D_4} + P_{L_1} = P_{switch} +$$

$$+ \sum_{a=1}^4 (P_{RF})D_a + \sum_{a=1}^4 (P_{VF})D_a + P_{rL_1}. \quad (26)$$

The efficiency of the suggested converter η is then as follows

$$\eta = \frac{P_o}{P_o - P_{Loss}} = \frac{1}{1 + \dfrac{P_{Loss}}{P_o}}. \quad (27)$$

Based on the simulation results for an output power of 200 W, the total losses have been calculated and are shown in Fig. 5(a). This figure clearly indicates that the dynamic and switching power losses of the diodes are the primary sources of losses, followed by the inductor and switch. The efficiency diagram of the proposed converter, including both simulation and experimental test results, is presented in Fig. 5(b). This figure demonstrates that the converter achieves maximum efficiency at higher power levels, with efficiencies of approximately 97.8 % for simulation and 94.5 % for experimental test results. The discrepancy between the software and hardware test results is attributed to some complex power losses that are difficult to calculate theoretically, as well as the quality of the components used, particularly the switching components and their internal resistances when connected.
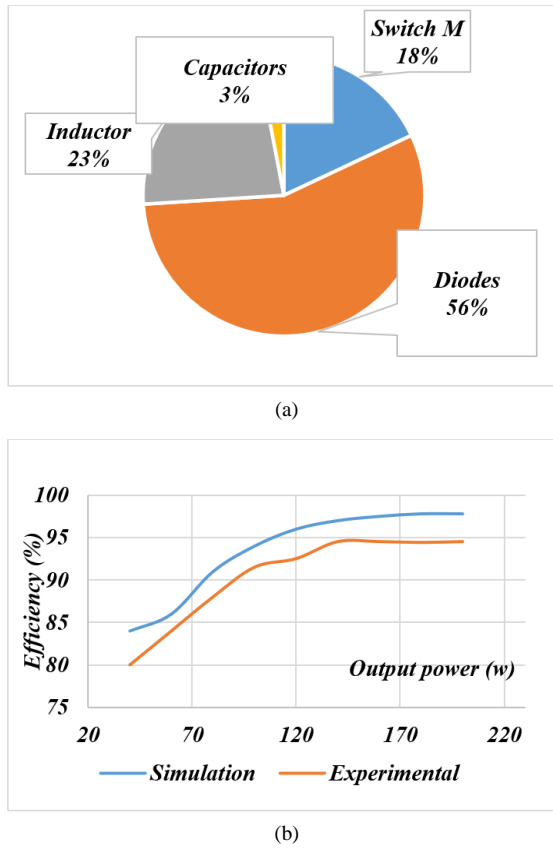
(a)

(b)

Fig. 5. (a) Loss distribution among the components of the proposed converter; (b) Converter efficiency for an output power of 200 W in both simulation and experimental tests.

Table I presents several new and successful DC-DC converters published over the last three years.

TABLE I. COMPARISON BETWEEN DIFFERENT CONVERTERS

Converter	S	D	L/T	C	Voltage gain	Efficiency (%)
[16]	3	5	2	4	$\dfrac{1+n+d}{1-d}$	91–94
[17]	2	2	2	2	$\dfrac{d}{(1-d)^2}$	92.7–94.2
[18]	1	5	3	3	$\dfrac{d(1+3d)}{(1-d)}$	83–94
Proposed	1	4	1	4	$\dfrac{3-d}{1-d}$	80–94.5

The table compares different specifications of converters, such as the number of switches (S), diodes (D), inductors (L), transformers (T), and capacitors (C). It also considers the voltage gain equations and the experimental efficiency of these converters. Among all the suggested converters, those in [18] and this study have only one power switch, ensuring simplicity in the control mechanism. This is because a higher number of switches requires more driver circuits, which complicates control, especially when isolation is needed. The presented converter has only one inductor, minimising dynamic losses. With respect to the number of diodes and capacitors, the proposed converter is in a reasonable position compared to the others. In the voltage gain equations, the parameter n indicates the number of enhancement cells, and most converters exhibit considerable voltage gains. The

efficiency of all converters can reach around 94 %, which is acceptable. Therefore, the table clearly shows that the proposed converter has a reasonable condition with the possibility of applying a simple control scheme.

III. SCHEMATIC AND PCB DESIGN

Various electromagnetic interference (EMI) issues can lead to electrical malfunctions, disrupt the proper use of radio frequencies, ignite flammable or hazardous environments. Low pass filters are effective in suppressing high-frequency EMI while allowing low-frequency signals to pass. They are the most commonly used electromagnetic compatibility (EMC) filters in the industry and typically consist of LC circuits.

In (28), the cut-off frequency of the filter is calculated as follows

$$f_c = \frac{1}{2\pi\sqrt{LC}}. \tag{28}$$

The selection of inductance and capacitance to be used in the filter is determined using (2) and (3):

$$L = \frac{1}{\left(2\pi f_c\right)^2 C}, \tag{29}$$

$$C = \frac{1}{\left(2\pi f_c\right)^2 L}. \tag{30}$$

Given that the switching frequency is targeted at 25 kHz, the cut-off frequency is adjusted to the same frequency. Therefore, the values of L and C can be calculated as follows. Alternative frequencies can be chosen and utilised. However, in this case, 25 kHz was selected based on the laboratory equipment available for testing.

Following the schematic design of the circuit presented in Fig. 6, the printed circuit board (PCB) layout was created using the Altium Designer programme. The PCB is configured to have four layers: Top Layer, Ground Plane, Power Plane, and Bottom Layer.
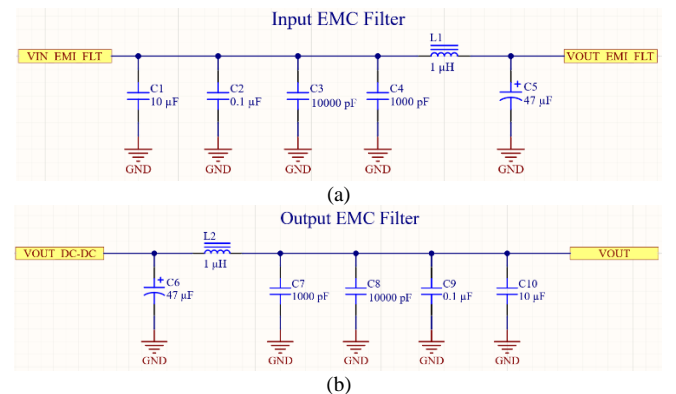

(a)

(b)

Fig. 6. (a) EMC input filter; (b) EMC output filter.

Once the PCB design is completed, the 15 rules depicted in Fig. 7 are scrutinised using the EMI Design Rule Checker programme to ensure the EMI/EMC compatibility of the board throughout the design phase. The 15 rule control elements in EMIStream draw on extensive expertise and experience in EMI suppression techniques. This process aims

to mitigate high testing expenses and prolonged durations.

Rule	f=0	0<f<10	10≤f<50	50≤f<100	100≤f
Trace Length	☐	☐	☐	☐	☑
Via Count	☐	☐	☐	☐	☐
Plane Edge	☐	☐	☐	☐	☑
Reference Change	☐	☑	☑	☑	☑
Return Path	☐	☑	☑	☑	☑
SG Trace	☑	☑	☑	☑	☑
Estimated Radiation	☐	☐	☑	☑	☑
SG Via Spacing	☑				
Plane Outline	☑ 1				
Filter Location	☑				
Filter In/Out Interference	☑				
Decoupling	☑				
Differential-Length	☐	☐	☐	☑	☑
Differential-Parallel	☐	☐	☐	☑	☑
Differential-Impedance	☐	☐	☐	☑	☑
Differential-Phase	☐	☐	☑	☑	☑
XTalk	☐	☐	☐	☐	☑
D/A Interference	☑				
IC GND Split	☑				

Fig. 7. Rules checked in the EMI Design Rule Checker programme.

After analysing the 15 rules, any errors and design recommendations are identified and documented by marking them on the PCB. Figure 8(a) illustrates the cause of the error, while Fig. 8(b) shows the location of the error marked on the PCB. For instance, these figures illustrate that there is an inadequate number of vias near the end of the PCB for the GND line. This deficiency in GND vias along the plane could extend the return path of the current, potentially increasing EMI propagation on the board. To address this issue, unnecessary planes should be removed, or a sufficient number of vias should be utilised. The aim is to rectify design-related EMI/EMC problems by implementing the suggested corrections provided by the programme.
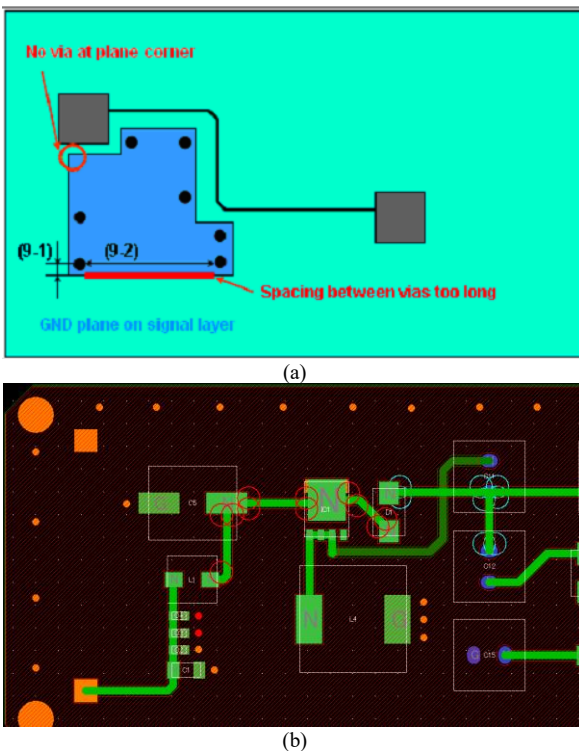

(a)

(b)

Fig. 8. (a) Error cause; (b) Error location.

Resonance between the Power and Ground planes can lead to increased EMI. The Power/Ground resonance analysis function considers plane shapes, capacitors, and the distance between Power and Ground planes, analysing resonance

based on the partial element equivalent circuit (PEEC) method. The Plane Resonance Analyser displays temperature points on the board and offers optimised capacitor placement to mitigate resonance. Additionally, the plugin enables far-field EMI calculation and multilayer resonance analysis.

Upon completion of the programme analysis, the main screen displays the maximum voltage distribution as a colour gradient. Red areas on the colour gradient indicate the highest risk of resonance, while colours closer to blue indicate a lower risk. Figure 9 illustrates the colour map generated after resonance analysis.
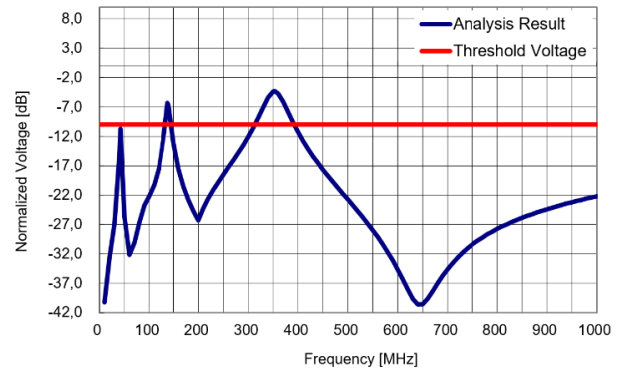

Fig. 9. Plane resonance spectrum chart.

The resonance map between the Power/Ground plane does not indicate a level of resonance that poses a risk across the entire board. Additionally, the programme generates a spectrum graph illustrating the maximum voltage level for each frequency.

The normalised voltage (dB) - frequency (MHz) curve is a critical tool in EMI/EMC analysis for high-frequency circuits and PCB design. Using a logarithmic scale to express the normalised voltage enables effective visualisation of a broad dynamic range. Peaks observed in the graph signify voltage increases at specific frequencies, known as resonance frequencies. These peaks aid in identifying resonant frequencies, where elevated voltage levels may lead to potential EMI issues within the circuit.

Once resonance frequencies and regions of high voltage are identified, design adjustments can be implemented to mitigate voltage levels at these frequencies. This may involve techniques such as integrating appropriate bypass capacitors, modifying trace placement, or optimising layer structure. The Threshold Voltage serves as a specific limit value on the normalised voltage graph. Voltage levels surpassing this threshold may indicate potential EMI problems or abnormal conditions that require attention during the design process.

Based on the spectrum provided in Fig. 9, the voltage on the power plane is reduced by half at -8 dB regarding the noise (applied voltage). With the inclusion of a margin of error, a maximum voltage recommendation of -10 dB is established for the spectrum graph. However, the peaks at 150 MHz and 350 MHz exceed the -10 dB threshold, indicating the need for precautions. To mitigate resonance between planes, a capacitor is placed in the resonance region.

IV. DISCUSSION

This section outlines some of the essential parameters for converter design, including cost analysis and its feasibility for electric vehicle (EV) applications, design challenges, and

future considerations. These topics are discussed in three distinct subsections.

A. Cost Analysis

DC-DC converters are crucial to improve the energy efficiency and performance of EVs. However, for widespread adoption, it is essential to carefully evaluate the cost-effectiveness and design expenses of this technology. DC-DC converters typically include semiconductor switches, inductors, transformers, capacitors, and control circuits. The performance of the converter is directly influenced by the quality and characteristics of these components. Additionally, automotive manufacturers must meet stringent testing requirements, necessitating the use of automotive grade AEC-Q100 and AEC-Q200 products in electronic circuits, which increases costs. To mitigate these expenses, a design that features a single switch and omits a transformer to reduce cost and volume is preferred, as presented in this study.

DC-DC converters in EVs must also undergo specific tests to meet safety and performance standards. Compliance with electromagnetic compatibility (EMC)/electromagnetic interference (EMI) regulations is critical, and failures in these tests can lead to additional costs and significant time delays. These issues can be identified and resolved using appropriate software. Although this software may be costly during the design phase, it can ultimately reduce total costs by preventing future problems.

B. Future Research Topics

Wide-bandgap semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), offer higher efficiency and power density compared to those of traditional silicon-based semiconductors. These materials can function at elevated temperatures and exhibit lower switching losses. This makes them ideal for designing circuits with greater efficiency and temperature resistance, particularly in DC-DC converters for electric vehicles. A key component of DC-DC converters is their control algorithms. Intelligent control algorithms enable power converters to dynamically adjust to varying load conditions and operational environments, enhancing efficiency and minimising energy losses. Integrating artificial intelligence and machine learning techniques can further optimise efficiency by performing real-time data analysis to detect abnormalities and maintain optimal system operation conditions.

C. Challenges of the Proposed Converter in Real-World Electric Vehicle Systems

In the realm of EVs, high-gain, efficient, and high-power converters are becoming increasingly important topics. Achieving these goals requires the use of SiC and GaN semiconductors. Designing the driver circuits for the switches in such power converter topologies poses a challenge, as they typically require high-frequency switching schemes executed with precise control. Additionally, the EMI filter design must be accurate and effective across a wide range of switching frequencies, often requiring a series of LC filter elements. These areas present promising avenues for future research in this field.

V. CONCLUSIONS

This study presents a single switched power converter capable of connecting to an electric vehicle battery pack for grid integration. The proposed converter features a preamplifier layer that easily doubles the voltage of the battery pack. The subsequent layer enhances this preamplified voltage through a switching scheme that uses only three diodes. Theoretical, simulation, and experimental test results demonstrate that for duty ratios of 0.5 to 0.9, the proposed converter can increase the battery pack voltage by 5 to 21 times, respectively, which is significant. Additionally, electromagnetic interference (EMI)/electromagnetic compatibility (EMC) filter designs are presented for both the input and output sides of the converter. These filters have a cutoff frequency set at 25 kHz, which matches the switching frequency. 15 experience-based rules were considered and sources of EMI/EMC noise were identified using the EMI Design Rule Checker programme. The plane resonance spectrum chart indicates that, across a wide frequency spectrum, the designed printed circuit board (PCB) in the Altium programme is suitable and applicable, generating a voltage below the threshold voltage. The efficiency of the proposed converter was evaluated through simulation using Matlab Simulink and on a hardware test bench in the laboratory, achieving a 97.8 % and 94.5 % efficiency for simulation and experimental tests, respectively, at 200 W power output. A cost analysis was conducted, and the application of silicon carbide (SiC) and gallium nitride (GaN) power semiconductor devices was discussed as key topics and challenges for future research.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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