Systematic Design of a Pseudodifferential VCO Using Monomial Fitting

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***Abstract*—Digital integrated electronics benefits from its higher abstraction level, allowing optimisation methods and automated workflows. However, analogue integrated circuit design is still predominantly done manually, leading to lengthy design cycles. This paper proposes a new systematic design approach for the sizing of analogue integrated circuits to address this issue. The method utilises a surrogate optimisation technique that approximates a simple monomial function based on few simulation results. These monomials are convex and can be optimised using a simple linear optimisation routine, resulting in a single global optimal solution. We show that monomial functions, in many cases, have an analytic relation to integrated circuits, making them well suited for the application. The method is demonstrated by designing a 14 MHz pseudodifferential voltage-controlled oscillator (VCO) with minimised current consumption and is manufactured in a 180 nm process. The measured total current matches the predicted and is lower than that for other similar state-of-the-art VCOs.**

***Index Terms*—CMOS; Modelling; VCO; Time-based; Optimisation.**

I. INTRODUCTION

Digital integrated circuit (IC) design has seen significant advancements in recent years, with a high degree of automation and optimisation commonplace. However, the same level of automation and optimisation has not yet been achieved in the design of analogue ICs, which has proven to be more complex and challenging. The design of analogue circuits is a manual process that involves a considerable amount of time and effort, significantly increasing the development cost, even though it only accounts for a fraction of the functionality in many mixed-signal ICs [1]. Thus, there is a growing need for optimisation and systematic design methods in analogue IC design to improve design efficiency and performance.

One of the primary challenges in applying optimisation methods to analogue IC design is the complexity of transistor models, which significantly impacts simulation time and convexity in analogue circuit optimisation. Transistor models used in analogue IC design are more complex than their digital counterparts, where highly abstracted models can be used. However, analogue transistor models are highly nonlinear and require extensive computation to evaluate their performance accurately. This complexity results in simulation times that are much longer than those required for digital circuits, making optimisation a computationally intensive task.

Over the years, many approaches have been tried to optimise analogue IC designs, generally falling into two categories: fast equation-based optimisation methods [2]–[11] and slow but precise simulation-based methods [12]–[20]. Equation-based methods work on simplified transistor models that enable fast solving. Generally, the equation-based methods use geometric programming [2]–[7] or the g_m/I_D method [8]. The main drawbacks of these methods are the simplified models that can introduce discrepancies between calculated and simulated performance. These discrepancies tend to grow with smaller process nodes because of increased nonlinearities in the transistor models. Furthermore, to apply these methods, a large number of design equations that are unique to any given circuit must be established. This task is both difficult and time-consuming.

The simulation-based methods address the drawbacks of the equation-based methods by optimising directly on the simulations with the complex transistor models. This removes any discrepancies from the solution, and no design equations need to be established. However, the method is computationally expensive and, depending on the circuit, can take anywhere from minutes to days to complete. Moreover, convexity is not guaranteed, making finding a global optimal solution challenging. Global optimisation techniques such as genetic algorithms (GA) and particle swarm optimisation (PSO) can help mitigate this challenge. However, they require many simulations, making them computationally expensive and impractical for large-scale analogue circuits.

This work presents a systematic design method that uses simple monomials together with optimisation to quickly and easily find device parameters that optimise the circuit. Because of the simplicity of the monomials, approximate maps can be established with a minimum of simulations. The resulting fitted models are convex through geometric programming, leading to a fast convergence to an approximate global optimal solution. We show that the method can be applied to both analogue and mixed-signal circuits by designing a pseudodifferential voltage-controlled

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oscillator (VCO) for time-based control applications where the objective is to minimise the current consumption while satisfying all the other specifications. The proposed method can deliver the simplicity of the simulation-based method while achieving convexity and high convergence speed associated with the equation-based methods. Finally, the designed VCO is implemented in a 180 nm process.

The paper is structured as follows. Section II covers the theory of the proposed surrogate optimisation method. Section III presents the pseudodifferential VCO structure and the method used to construct the relevant monomial models. Section IV applies the optimisation to the found surfaces and details how the results compare with the simulations. Finally, Section V presents the IC implementing the VCO in a 180 nm process and compares the performance with the simulation results obtained from the optimisation.

II. THEORY

A. Surrogate Optimisation

Optimisation can be a challenge when the objective function is either too difficult or too expensive to evaluate. This can be due to noise in the function resulting in a nonsmooth and nonconvex search space or because the computation is too time-consuming. In IC design, the latter is often the case. Since modern IC design software uses large high-fidelity BSIM models to accurately describe the behaviour of each transistor, a tremendous amount of computation is needed to evaluate a circuit that only grows with each transistor added to the circuit. In cases where the objective function is based on a metric that can only be extracted from transient simulations, the computation time for a single simulation can easily extend to several hours or days. As most optimisation methods require multiple iterations to converge to an optimum, optimisation directly on high-fidelity circuit simulations is, in many cases, impractical. To enable optimisation on these types of problems, the surrogate optimisation approach has previously been used successfully [21]–[25].

Surrogate optimisation consists of three steps:

1. A surrogate model that approximates the underlying function is fitted based on a few carefully chosen simulations;
2. A conventional optimisation is performed on the surrogate model;
3. The optimisation result is evaluated in simulation.

Figure 1 shows the flow of the method.

For the surrogate optimisation to work well, the surrogate model must provide a good approximation of the underlying function. This can be achieved by having prior knowledge about the underlying behaviour or by having a surrogate model with enough flexibility to approximate any function. While the latter is the most common for generalised solvers in which Gaussian process functions are commonly used, the former is preferred whenever possible. In Section III, we show that monomial functions are a good candidate for the surrogate model. This implies that a monomial fitting is needed in step 1 and that geometric programming is needed in the optimisation step. Both are covered in the following two sections.

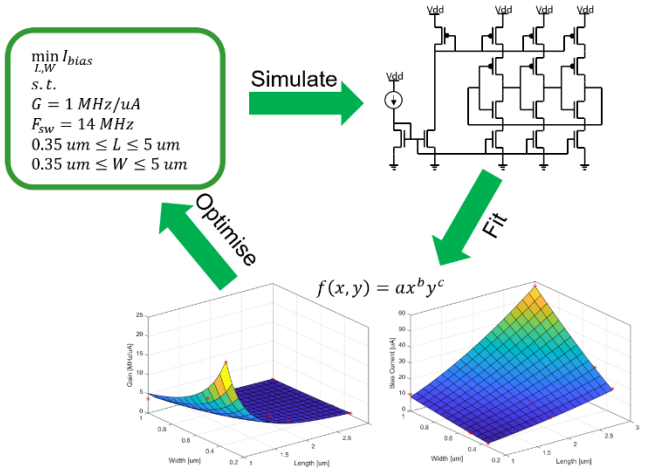

Fig. 1. Surrogate optimisation flow. First, a surrogate model is fitted to simulation results, then optimisation is performed on the surrogate model. Finally, the solution is verified in simulation.

B. Geometric Programming

Geometric programming is an optimisation technique that converts nonconvex posynomials and simpler monomials to a convex programme that can be solved with conventional optimisation methods [26]. In the case of monomials, this results in a linear programme. Equation (1) shows the structure of a monomial. It contains a coefficient $a > 0$, which is multiplied by all the variables $x_1 \cdots x_N$. All the variables can be raised to some power given by the coefficients $b_1 \cdots b_N$. A posynomial is simply a sum of monomials. In this work, it is sufficient to work with monomials. Thus, the following discussion will be limited to the use case of monomials in geometric programming

$$f(x) = a x_1^{b_1} x_2^{b_2} \ldots x_N^{b_N}. \tag{1}$$

Monomials can be converted to an affine form by applying a logarithmic transformation, as seen in (2)

$$g(z) = \ln\left(f\left(x\right)\right) = \ln\left(a\right) + b_1 z_1 + b_2 z_2 + \ldots + \ldots + b_N z_N, \tag{2}$$

where $z_n = \ln(x_n)$ is the transformed variable. By taking the logarithm, multiplication becomes addition and the exponents descend and become simple coefficients. Once the problem is of the form $g(z)$, a conventional simplex or interior point method can be used to find the global optimal solution. The solution to the original problem $f(x)$ is recovered through an exponential transformation of the solution for $g(z)$: $x_{opt} = e^{z_{opt}}$.

C. Monomial Fitting

Like geometric programming, the trick to monomial fitting is to apply a logarithmic transformation to convert the monomial to an affine function. Once an affine function is established, the fitting can be conducted using an ordinary least squares (OLS) fit. In practice, the fitting is done by creating the coefficient matrix M in (3) where $X_1 \cdots X_N$ are vectors containing the simulation points for each of the variables of interest. The last element in M is used to obtain the coefficient $\ln(a)$

$$M = \left[\ln(X_1) \quad \ln(X_2) \quad \ldots \quad \ln(X_N) \quad \mathbf{1}\right]. \tag{3}$$

With M created, the OLS fit is found by taking the pseudoinverse of M and multiplying it with the response vector Y

$$b = M^{\dagger} \ln(Y). \tag{4}$$

Depending on the value of b, the fitted function can have different behaviours. $b > 1$ results in a polynomial response, while $b = 1$ is a linear function. $0 < b < 1$ has a square root-like behaviour and $b = 0$ is a constant. For negative values of b, the inverse of the just mentioned behaviours is obtained. The fitting method is repeated for every response of interest. In the case of a pseudodifferential VCO, this can be the current consumption, phase noise, and gain.

III. Monomial Fitting of VCO

A pseudodifferential VCO is used as a test case to test the surrogate optimisation method. The pseudodifferential VCO consists of an operational transconductance amplifier (OTA) where each leg of the OTA connects to a current-controlled ring oscillator (CCO). The configuration allows the VCO to take in a differential input and output two pseudodifferential frequencies. This type of VCO is commonly used as an integrator in time-based control circuits where the two inputs are used for the reference and feedback voltage, leading to the integration of the error signal [27], [28]. Figure 2 shows the structure of the circuit. By mirroring the control output current from the OTA to the CCO, the behaviour of the OTA and CCO can be decoupled, meaning that the modelling of the VCO can be divided into deriving a surrogate model for the OTA and the CCO independently. These two models can then be recombined in the optimisation state. This allows for two low-order models that are easier to interpret compared to a single high-order model.

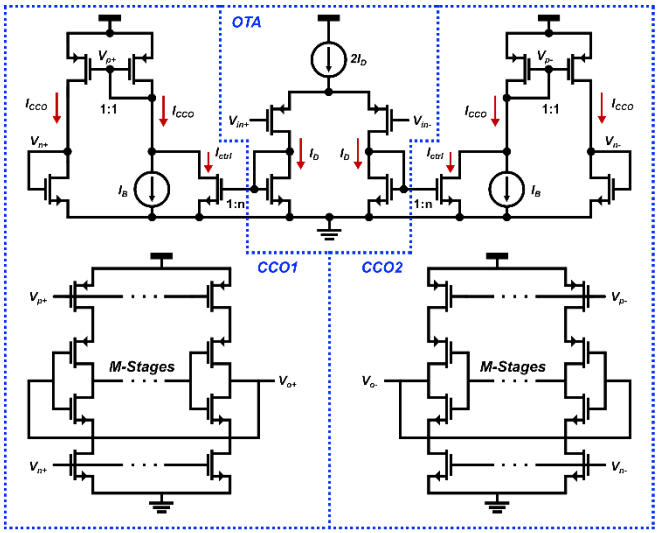

Fig. 2. Diagram of the pseudodifferential VCO. It is easily seen that the circuit consists of an OTA and two CCOs.

A. Surrogate Model - OTA

1. Modelling

The modelling of the OTA is based on the subcircuit shown in Fig. 3. The gain of the OTA is determined by the size of the input transistor pair (Q_1, Q_2) and the bias drain current I_D through the same devices. Because the OTA's gain is dependent on I_D, the tail current can be modeled as an ideal current source without any loss of generality. The devices (Q_3, Q_4) do not affect the OTA gain and are only used for the current mirroring to the CCO. From the Shichman-Hodges model, the gain, g_m, is approximately given by (5)

$$g_m \approx \sqrt{2\mu C_{ox} \frac{W}{L} I_D} = \alpha_{OTA} R^{0.5} I_D^{0.5}, \tag{5}$$

where μC_{ox} is a process constant, a_{OTA} is $\sqrt{2\mu C_{ox}}$, and R is the width-to-length ratio W/L. From (5), it is seen that the small signal gain of the OTA, g_m, can be approximated by a monomial in R and the bias drain current I_D. Based on this, a monomial fitting of the simulation data can be expected to serve as a good surrogate function for the true value of g_m.

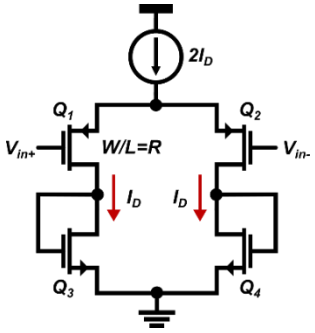

Fig. 3. Circuit diagram of the OTA.

2. Fitting

The OTA in Fig. 3 is simulated in Cadence Virtuoso with four different I_D and five different R for a total of 20 simulations. Since the only parameter of interest is the gain g_m, a simple dc operating point simulation is enough, making the simulations quick to conduct. In principle, a two-factor simulation could be used instead, resulting in four simulations. However, due to the speed of the chosen simulation, more points are tested to improve the fitting. Figure 4 shows all the simulated points (dots) and the contour lines for the fitted monomial shown in (6)

$$\overline{g_m}(R, I_D) = 6.36 R^{0.19} I_D^{0.83}. \tag{6}$$

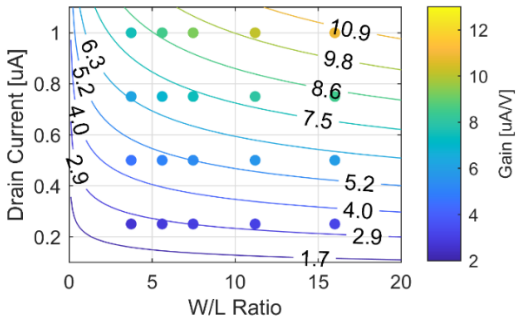

Fig. 4. Gain versus width/length ratio R and the drain current I_D. The dots show the simulated points with their colour indicating the gain. The contour lines show the monomial fit $g_m(R, I_D)$. The plot shows a good correlation between the simulation points and the fit monomial with $r^2 = 0.99$.

From (6), we find that the fitted exponents both have the same functional behaviour as the exponent given in (5). The

deviation from (5) suggests that the surrogate model is able to better capture unique nonlinearities of the process by appropriately adjusting the exponents. This is also seen in Fig. 4, where the colours of the dots are similar to the colour of the nearby contour lines, suggesting a good match between the model and the simulation results. The model achieves a coefficient of determination of $r^2 = 0.99$. In our specific case (6), it is found that the drain current has a significantly larger impact on the gain than the ratio of the input devices.

B. Surrogate Model - CCO

1. Modelling

Figure 5 shows the CCO subcircuit for the surrogate modelling. The CCO is identical to the CCO in Fig. 2, with the only difference being that the control current I_{ctrl} and the bias current I_B are combined into a single current source I_{CCO}. The starved inverter ring oscillator (Q_9-Q_{12}) consists of M identical stages. Finally, all the current mirrors are unity gain for simplicity, meaning that the starved inverter can sink and source the same maximum current I_{CCO}.

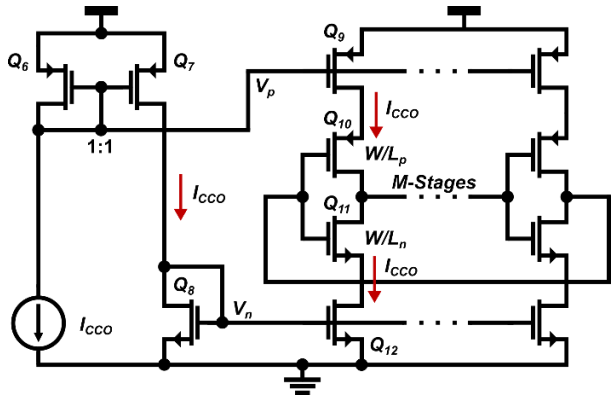

Fig. 5. CCO diagram. The control current from the OTA is modelled as an ideal current source.

The parameters of interest for the CCO are usually the idle frequency, f_{osc}, the gain K_{CCO}, the current consumption, which scales with the current I_{CCO}, and the phase noise PN. The idle frequency of a ring oscillator is inversely proportional to the number of stages in the oscillator, M, and the time constant for charging the gate capacitance C_G through a transistor with a resistance R_{on}. This results in the relation in (7). Since C_G scales with the area of the transistor WL, and the on-resistance can be approximated by $L/\lambda_L I_{CCO}$, a monomial in M, I_{CCO}, L, and W can be achieved.

$$f_{osc} \propto \frac{1}{MR_{on}C_G} \approx \frac{\lambda_L I_{CCO}}{C_{ox}ML^2W} = a_{f_{osc}} I_{CCO} M^{-1} L^{-2} W^{-1}. \quad (7)$$

Taking the derivative in regards to I_{CCO}, the current-to-frequency gain K_{CCO} is found to be (8), a monomial in M, L, and W

$$K_{CCO} = \frac{df_{osc}}{dI_{CCO}} \propto \frac{\lambda_L}{C_{ox}ML^2W} = a_{K_{CCO}} M^{-1} L^{-2} W^{-1}. \quad (8)$$

Likewise, by isolating I_{CCO} in (7), (9) is obtained, which is also a monomial in M, f_{osc}, L, and W

$$I_{CCO} \propto \frac{C_{ox}Mf_{osc}L^2W}{\lambda_L} = a_{I_{CCO}} Mf_{osc}L^2W. \quad (9)$$

Like with the OTA, we find that most of the physical parameters of interest for the optimisation are naturally expressed as monomials in the Shichman-Hodges modelling framework. This sparks confidence in the monomial functions being a good candidate function for surrogate optimisation within the IC design.

Unlike the previous parameters, the phase noise is not easily expressed analytically. However, according to [29], phase noise can be modelled with a posynomial and often approximated with a monomial.

Equations (7)–(9) create a large search space in the variables M, I_{CCO}, L_n, W_n, L_p, and W_p, where n and p denote the N-type metal-oxide-semiconductor (NMOS) (Q11) and the P-type metal-oxide-semiconductor (PMOS) (Q10) device, respectively. While this 7-dimensional search space can be used directly for the model fitting, it is beneficial to reduce the search space by imposing constraints on some of the variables based on the knowledge of the system. By inspection, it is observed that having length and width as variables for both Q10 and Q11 causes an overparametrisation of the model. This means that a variable can be removed without reducing the solution space. In this case, W_p and W_n are merged into a single parameter W. Moreover, it is of interest to fix the number of stages M. M is an integer variable that is only allowed to take odd values. Hence, it cannot be properly represented by a monomial. In our case, we fix M to 7 stages.

The following constraints will usually be applied first in the optimisation step. However, to visualise the results for this paper, they are imposed now to reduce the number of variables to two. It is desirable to have an identical rise and fall time in the oscillator, as this is known to improve phase noise. The rise and fall time is strongly related to (7), making the monomial a good candidate function for the modelling. By restricting it now, a mapping between L_p and L_n can be found, thereby removing L_p from the search space. Lastly, f_{osc} is fixed to 14 MHz causing I_{CCO} to be determined from L_n and W. With this, the search space is reduced to the variable L_n and W which can be easily visualised.

2. Fitting

The CCO in Fig. 5 is simulated in Cadence Virtuoso using the two-factor approach, meaning that two different widths and lengths for the inverter device (Q_{10}, Q_{11}) are used for a total of just four simulations. The width and length are picked such that they are placed at the corners of the search space. For each simulation, W and L_n are picked, then I_{CCO} and L_p are adjusted to ensure similar rise and fall time and the correct f_{osc}. Since the frequency is a temporal measure, a transient simulation is needed. Furthermore, a periodic steady state (pss) analysis is needed to obtain K_{CCO} and the phase noise PN. Figure 6 shows the four simulated points with the contour lines of the fitted monomials for the current I_{CCO}, Gain K_{CCO}, and Phase Noise PN. Similarly, (10)–(12) shows the fitted monomials:

$$\overline{I_{CCO}}(W, L_n) = 1.80 L_n^{1.52} W^{1.28}, \quad (10)$$

$$\overline{K_{CCO}}(W,L_n) = 10.37 L_n^{-2.21} W^{-1.34}, \quad (11)$$

$$\overline{PN}(W,L_n) = 76.01 L_n^{0.11} W^{0.04}. \quad (12)$$

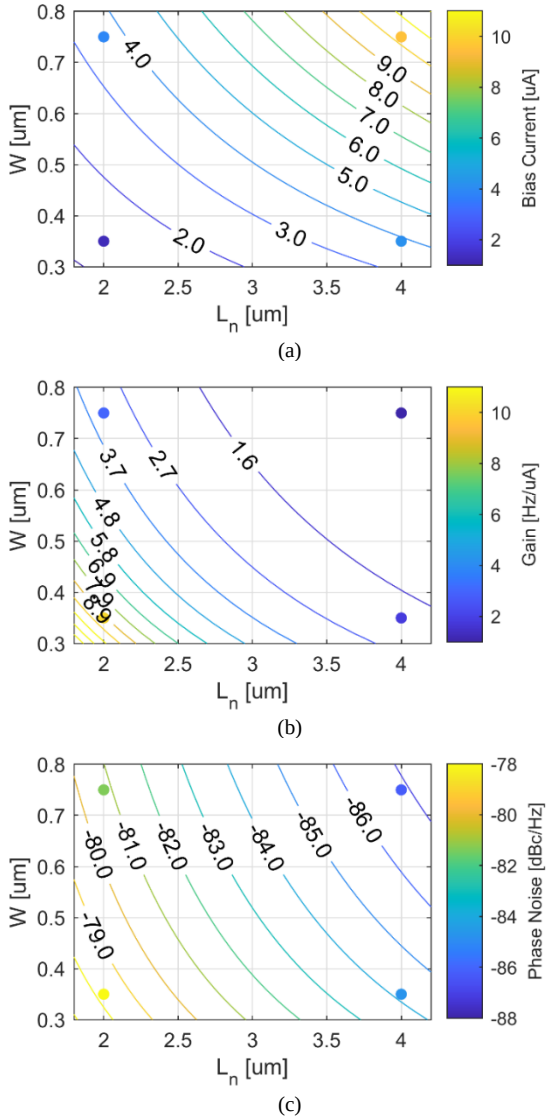

Fig. 6. Fitted monomials with simulation results (dots) for different lengths L_n and widths W: (a) Bias current I_{CCO} - r^2 = 0.98; (b) CCO gain K_{CCO} - r^2 = 0.98; (c) Phase noise PN at 100 kHz - r^2 = 0.97.

The exponents in the fitted monomials (10) and (11) align with the exponents derived in (9) and (8), with slight differences indicating that the fitted monomials better capture process-dependent properties. This is further supported by the graphs in Fig. 6, which show a high correlation between the simulated points and the surrogate models with coefficients of determination at $r^2 = 0.98$ for I_{CCO} and K_{CCO}, and $r^2 = 0.97$ for PN.

IV. Optimisation

With all approximate surrogate functions determined, it is possible to minimise the preferred objective function while simultaneously satisfying all the necessary constraints. Table I shows all the constraints specified for the pseudodifferential VCO. Because f_{osc} and t_{err} were restricted in the fitting process, only K_{VCO} must be included as a constraint in the optimisation programme. For the objective function, the current I_{CCO} is minimised. I_{CCO} is mirrored into all the inverter stages in the CCO, making it proportional to the total current consumption of the CCO. By minimising I_{CCO}, the total current of the CCO is also minimised.

TABLE I. SPECIFICATIONS FOR THE PSEUDODIFFERENTIAL VCO.

Name	Parameter	Value
Idle Frequency	f_{osc}	14 MHz
VCO Gain	K_{VCO}	1 MHz/V
t_{rise}/t_{fall}	t_{err}	1

A. Bounds

In addition to the constraints in Table I, general upper and lower bounds for device sizes, current, and scaling are also needed. The device sizes are L_n and W in (10) and (11), and the ratio R in (6). The current refers to the drain current I_D in (6). Lastly, the scaling refers to the factor n scaling between the OTA and the CCO in Fig. 2, which has not been included in any of the surrogate models. Table II shows all the bounds.

TABLE II. UPPER AND LOWER BOUNDS FOR THE OPTIMISATION.

Name	I_D [µA]	R []	n []	L_n [µm]	W [µm]
Upper (*ub*)	3	20	4	4	1
Lower (*lb*)	0.5	1.6	0.25	2	0.35

B. Gain Constraint

The total gain of the VCO is the product of the OTA gain g_m and the CCO gain K_{CCO} combined with the scaling factor n. Equation (13) shows the combined equality constraint for K_{VCO}

$$K_{VCO} = \overline{g_m}(I_D,R)\, n \overline{K_{CCO}}(W,L_n) = \\ = a_{OTA} a_{CCO} R^{B_R} I_D^{b_I} n L_n^{b_L} W^{b_W}. \quad (13)$$

Since (13) is a monomial, it is converted to its convex affine form through logarithmic transformation so that it can be used in the optimisation. Equation (14) shows the transformed constraint. Notice that all the design variables are replaced with z_n

$$\ln(K_{VCO}) = \ln(a_{OTA} a_{CCO}) + \underbrace{b_R \ln(R)}_{z_1} + \\ + \underbrace{b_I \ln(I_D)}_{z_2} + \underbrace{\ln(n)}_{z_3} + \underbrace{b_L \ln(L_n)}_{z_4} + \underbrace{b_W \ln(W)}_{z_5}. \quad (14)$$

C. Optimisation Problem

Using the logarithm of model (10) as the objective function, the complete optimisation programme is formulated in (15). The programme is linear and solved using a dual simplex algorithm

$$\begin{aligned} &\text{minimize } \ln\left(\overline{I_{CCO}}(W,L_n)\right) \\ &\text{subject to:} \\ &(14), \\ &\ln(lb) \le z \le \ln(ub). \end{aligned} \quad (15)$$

Multiple other objective functions can be formalised in addition to the objective function used in (15). Other objective functions could be but are not limited to minimising device sizes or phase noise.

Table III shows the recovered solution where all variables

except W sit on the optimisation bounds. Solutions to linear optimisations are always found on the bounds, the only reason not to be to satisfy a constraint, like in the case of W. The objective function reaches its minimum of $I_{CCO} = 7.26$ µA.

TABLE III. OPTIMAL SOLUTION.

Name	I_D [µA]	R []	n []	L_n [µm]	W [µm]
From (15)	0.5	1.6	0.25	4	0.57

Inserting the found values into the circuit in Virtuoso Cadence yields the results in Table IV.

TABLE IV. SIMULATED PERFORMANCE OF THE VCO FOR THE TWO CONFIGURATIONS "OPTIMAL" AND "REFINED" TOGETHER WITH THE EXTRACTED RESULTS.

Name	Target	Optimal	Refined	Extracted	Unit
f_{osc}	14.00	14.00	13.84	12.83	MHz
t_{err}	1.00	1.02	1.00	1.05	
K_{VCO}	1.00	0.89	0.99	0.84	MHz/V
K_{CCO}	1.03	0.97	1.12	0.89	MHz/µA
g_m	3.89	3.58	3.58	N/A	µA/V
I_{tot}	min	55.88	51.90	51.81	μA_{rms}
PN	-85.89	-86.51	-85.86	-91.31	dBc/Hz

We find that the simulated values are within 2 % of the target for all parameters except K_{CCO} and g_m, which are 8.0 % and 5.8 % lower than the target. This causes K_{VCO} to decrease by a similar amount. The deviation from the target is expected, since the found optimum is based on simple approximations of the underlying behaviour. Thus, a final fine-tuning is needed.

To get K_{VCO} closer to the target, the width and bias current is decreased to $W = 0.54$ µm and $I_{CCO} = 6.67$ µA, respectively. The updated results are shown in Table IV in the column "Refined". In the refined design, K_{CCO} is larger due to the smaller gate capacitance in the ring oscillator and the reduced current. This results in the correct gain for K_{VCO}. Furthermore, the increased frequency following from the smaller capacitance is compensated by the reduced current, resulting in a decrease of the total current I_{tot} by 3.98 µA. Finally, the column "Extracted" shows the post-layout simulation results for the "Refined" parameters. The most noticeable difference is the drop in K_{CCO} and, thereby, K_{VCO} and f_{osc} due to added capacitance in the switching nodes of the ring oscillator. The added parasitic capacitance also results in a more stable frequency, leading to improved phase noise.

V. EXPERIMENTAL VALIDATION

An IC is manufactured in a 180 nm TSMC complementary metal-oxide-semiconductor (CMOS) process to verify the results in Section IV. Figure 7 shows the fabricated IC. The IC has a total area of 2.84 mm^2 and consists of two identical pseudodifferential VCOs, each spanning 78 µm × 125 µm, resulting in an active area of 0.01 mm^2.

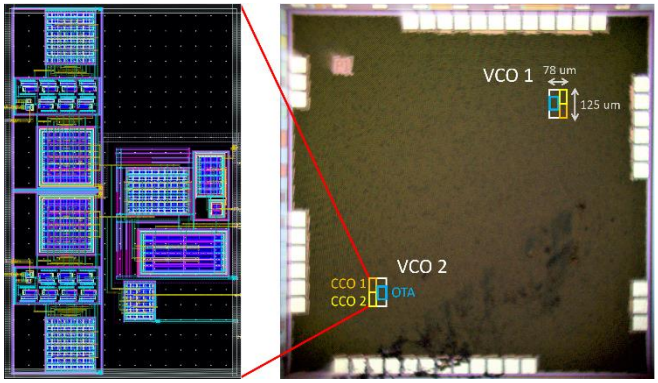

Fig. 7. Die photo and layout. The placement of the two VCOs is highlighted. The two top metal layers are fully stitched; hence it is not possible to see the circuit on the die.

The IC operates on a supply voltage of 1.8 V, and the OTA input pair is biased by 550 mV. Two design mistakes not related to the method covered in the previous sections resulted in undesirable behaviours of the VCO. The first mistake is seen in Fig. 8, which shows the output waveforms of the VCO. Due to an insufficient output buffer, the output of the VCO cannot deliver the current needed to fully drive the output, resulting in partial charging of the output capacitance and a peak voltage of 1.3 V instead of 1.8 V.

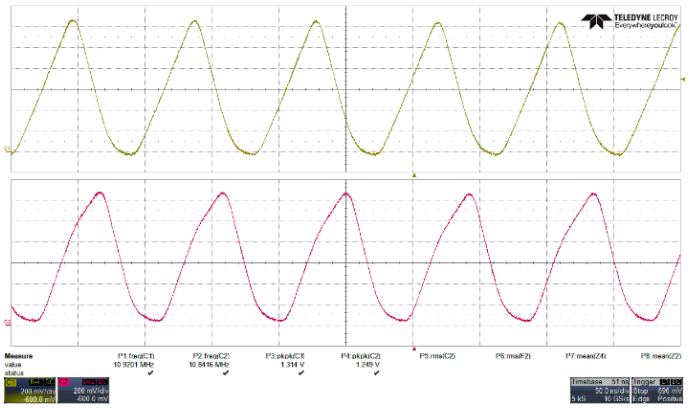

Fig. 8. Measured output waveform of the two CCOs in the pseudodifferential VCO at idle operation. Measurements were done with an active probe to reduce the capacitive load. Due to an insufficient output buffer, the squared waveform has deteriorated.

The second issue is that there is too little decoupling capacitance on the chip that leads to crosstalk between the two CCOs resulting in a modulation of the frequencies. Due to the deteriorated output signal and unstable frequency, phase noise and jitter measurements have not been performed.

To obtain a breakdown of the gains in the VCO, both K_{CCO} and K_{VCO} are measured. K_{CCO} is measured by removing the bias current for the OTA rendering $I_{ctrl} = 0$ and sweeping the CCO bias current I_B while measuring the average

frequency. Figure 9 shows the measured frequency and the resulting gain. Similarly, K_{VCO} is measured by changing the differential voltage $V_{diff} = V_{in+} - V_{in-}$ of the OTA while measuring the frequency output of both CCOs. K_{VCO} was first measured with the designed OTA bias current of 1 µA, which resulted in a lower gain than expected of 0.5 MHz/V. Due to the lower gain, the frequency offset becomes more prominent to a point where the frequency difference is only 40 kHz at $V_{diff} = -0.5$ V. To compensate, the bias current of the OTA is increased to 3 µA for the second measurement of K_{VCO} to recover the intended gain. Figure 10 shows the frequency and gain for the 1 µA and 3 µA cases.

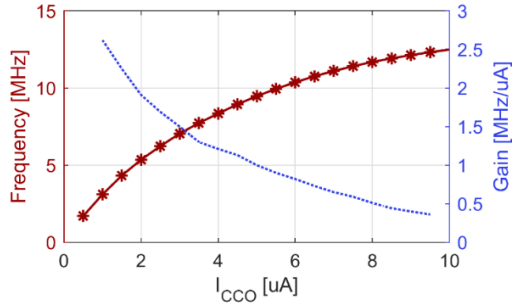

Fig. 9. Measured output frequency versus bias current for the CCO. The dotted line shows the corresponding gain K_{CCO}.

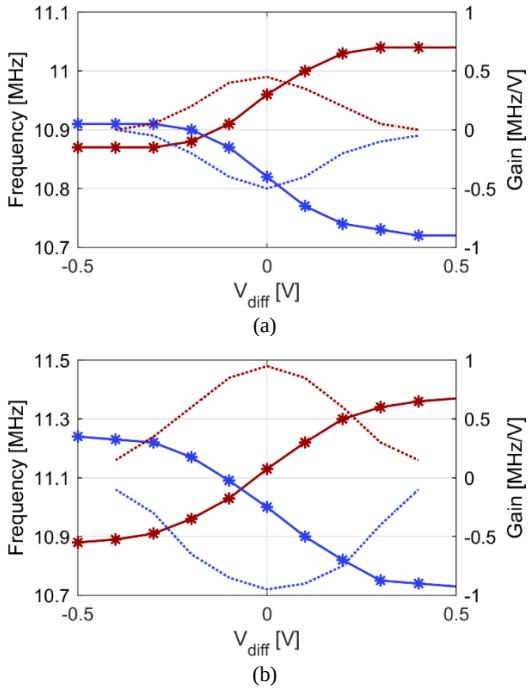

Fig. 10. Measured pseudodifferential output frequency (solid) and gain (dotted) for various inputs of differential voltage: (a) OTA biased with 1 µA. The response is severely affected by the frequency offset; (b) OTA biased with 3 µA. Due to the higher gain, the frequency offset is less prominent. The blue lines are the first CCO, and the red lines are the second CCO.

Table V provides a summary of the main results, as well as the parasitic simulation results extracted from Table IV. Inspecting the table, we find that for the original 1 µA of the bias current, both the gains and the frequency are lower than expected. The decrease in K_{VCO} is not fully accounted for in K_{CCO}, indicating that g_m has also decreased. However, the total current consumption corresponds to the extracted simulation results. By increasing the OTA bias current to 3 µA, g_m is increased to a point where K_{VCO} is recovered at the expense of the VCO current increasing to 57.07 µA.

TABLE V. SUMMARY OF THE MEASURED RESULTS.

Name	Extracted	Measured	Measured	Unit
f_{osc}	12.83	10.89	11.07	MHz
K_{VCO}	0.84	0.48	0.95	MHz/V
K_{CCO}	0.89	0.70	0.65	MHz/µA
I_{tot}	51.81	51.67	57.07	μA_{rms}

Finally, a comparison to other similar VCOs is presented in Table VI. A selection of current-starved ring oscillator VCOs with idle frequencies between 1 MHz and 250 MHz is used for the comparison. Because most VCO designs documented in the literature are meant for phased locked loops (PLLs) and radio frequency (RF) applications, only a tiny portion covers the range of interest in the comparison. To make the results comparable, the total current covers the current used to power a single CCO.

TABLE VI. COMPARISON TO THE STATE-OF-THE-ART.

Name	Presented	[30]	[31]	[32]
Year	2023	2021	2012	2013
Type	Meas.	Sim	Sim.	Sim
Process [nm]	180	180	180	50
Stages	7	3	5	21
V_{dd} **[V]**	1.8	1.8	1.8	1.0
f_{osc} **[MHz]**	10.9	1.0	222.5	105.4
I_{VCO} **[µA$_{rms}$]**	25.8	42.0	58.4	47.0

I. CONCLUSIONS

This paper proposes a surrogate optimisation method for designing analogue integrated circuits. By fitting monomial functions based on a few simulations, the circuit behaviour is approximated by a convex function, which is easily optimised using geometric programming. We showed that the monomial functions mimic the Shichman-Hodges models while better capturing process-specific nonlinear behaviours. A 14 MHz pseudodifferential VCO was designed to verify the method by independently modelling an OTA and a CCO and connecting them in the optimisation step. The fitting was made from 20 simulations for the OTA and just four simulations for the CCO. The fitted models showed good correlations with the simulation results with coefficients of determination between 0.97 and 0.99. The simulation of the optimised VCO showed a small mismatch between the optimal solution based on the model and the simulated performance, the worst mismatch being 8 %. The designed VCO was manufactured in a 180 nm process. Comparisons with the state-of-the-art showed reduced current consumption.

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CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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