Time-Based High-Pass, Low-Pass, Shelf, and Notch Filters

Nicolai J. Dahl^{1,*}, Pere L. Muntal², Michael A. E. Andersen¹

¹Department of Photonics and Electrical Engineering, Technical University of Denmark, Elektrovej B325, Kgs. Lyngby, 2800, Denmark ²Skycore Semiconductors, Fruebjergvej 3, Copenhagen, 2100, Denmark nicoje@dtu.dk; plm@skycore-semi.com; maea@dtu.dk

Abstract—This paper presents formulations for time-based first-order and second-order high-pass, shelf, and notch filters. These formulations are an extension to the existing literature where low-pass filters are already developed using a multiphase controlled oscillator in conjunction with a phase detector and charge pump. The presented high-pass filter expands the circuit by introducing a current-controlled delay line (CCDL) that provides a direct path from input to output. By combining the high-pass filter with the low-pass filter, we show that shelf and notch filters can be obtained without an increase in circuit complexity compared to the high-pass filter. The results show good matching between the ideal small signal and the simulated time-based large signal frequency response. The simulated of total harmonic distortion for the filters shows an increase in distortion due to the nonlinearities introduced by the CCDL for the high-pass, notch, and shelf filter compared to the existing low-pass filter. The derivation of the new filter types allows the creation of complex high-order time-based filters by combining multiple first- or second-order filters.

Index Terms—Time-based; Filter; Modelling; CMOS; PLL.

I. INTRODUCTION

In recent years, there has been a growing interest in the emerging topic of time-based systems [1]–[3]. Time-based systems replicate continuous analogue behaviour but use time as the variable instead of voltage and current. This results in circuits that use voltage-controlled oscillators (VCOs), controlled delay lines (CDLs), logic, and phase detectors (PDs) instead of Op-Amps, resistors, and capacitors. The lack of large passive components makes time-based systems appealing for integrated circuits due to their better scaling with process nodes and the removed size penalty from capacitors. Integrated time-based circuits have already proved their functionality in many applications, such as Op-Amps [4]–[6], time-based filters [7]–[11], and time-based control [12]–[15].

Regarding the time-based filters, the focus has mainly been on constructing low-pass filters where different approaches have been tried. The authors in [7], [9] use a multiphase phase-locked loop (PLL) structure where an input current controls a current-controlled oscillator (CCO) to obtain a

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fully time-based low-pass filter. In [10], a similar approach is used to construct a time-based gyrator to emulate an inductor used for an integrated resistor-inductor-capacitor (RLC) filter. In [11], a method is described that achieves filtering through boolean operations on generated pulse-width modulation (PWM) signals. Furthermore, in [4], [5], time-based operational amplifiers for filtering applications are implemented. Commonalities for these types of filters are their ability to work at very low supply voltages and low power draws while maintaining a low total harmonic distortion (THD) and high spur-free dynamic range (SFDR). This is achieved through their more digital nature and the good linearity of the VCOs. Furthermore, because of the PLL structure employed, infinite DC gain is achieved, resulting in good attenuation capabilities.

Table I shows the reported performance of time-based filter implementations together with selected filter implementations using various kinds of active building blocks (ABBs). The two key observations are the improved THD and power consumption of the time-based implementations.

However, the design of filters different from the low-pass filter has received limited attention. Having a broader range of time-based filter types available will enable the design of more complex filter structures such as high-pass, band-pass, notch, and shelf filters, thereby opening up time-based filters to more applications.

This paper will expand on the work done in [7] by formulating a high-pass filter and a shelf filter, as well as a general second-order filter, all while using a filter structure similar to the one presented in the paper.

The paper is structured as follows. Section II reviews the first-order time-based low-pass filter presented in [7] and replicates some of the main results in simulation. Section III expands on the work by introducing extensions to the proposed circuit to achieve a time-based high-pass filter with accompanying simulation results. Section IV combines the high-pass and low-pass filters to produce a time-based shelf filter. Finally, we show that the filters can be cascaded to obtain second-order filters with complex poles. The paper ends with a discussion of some of the nonlinear effects and a conclusion to summarise the findings.

Reference	Туре	Order	Process	Supply Voltage	Total Harmonic Distortion (THD)	Spur-Free Dynamic Range (SFDR)	Total Power	Area
[7]	Time-Based	4	90 nm	0.55 V	0.1 %	61 dB	2.9 mW	0.29 mm2
[11]	Time-Based	4	65 nm	0.50 V	0.22 %	55 dB	73 nW	0.007 mm2
[16]	DDCC+	4	130 nm	±0.75 V	5 %	N/A	3.65 mW	N/A
[17]	VDIBA	2	180 nm	±0.9 V	3.15 %	N/A	N/A	N/A
[18]	PCA	1	BJT	±5 V	0.383 %	N/A	25.7 mW	N/A
[19]	ABB	1	N/A	±5 V	2.2 %	60 dB	57.6 mW	N/A

TABLE I. COMPARISON OF STATE-OF-THE-ART CONTINUOUS LOW-PASS FILTERS.

II. TIME-BASED LOW-PASS FILTER

In [7], a prototype low-pass filter with a structure similar to the structure in Fig. 1 is proposed. The circuit is built around a multiphase current-controlled ring oscillator (CCO) and a phase detector (PD) that compares the phase of the CCO (ϕ) with a reference clock (ϕ_{Ref}) . CCOs have the property of integrating the phase based on the input according to (1)

$$\phi = |\omega(t)dt| = |I_{in}(t)k_{CCO} + \omega_{idle}dt, \qquad (1)$$

where ω is the switching frequency of the CCO in radians, I_{in} is the input current to the CCO, and k_{CCO} is the current-to-frequency gain of the CCO. The integrated phase ϕ is compared to ϕ_{Ref} in the phase detector, which evaluates the phase difference and outputs it as a PWM signal. Hence, the CCO, ϕ_{Ref} , and PD form a structure that outputs the integral of the input of the CCO as a PWM signal. By feeding back the output of the PD, the integrator is placed in a closed-loop configuration that results in a low-pass filter. Since the CCO needs the feedback as a current, a charge pump (CP) is added to convert the PWM voltages from the PD to the current I_{fb} . I_{fb} is subtracted from I_{in} , and the resulting error current enters the CCO. Equation (2) shows the resulting closed-loop transfer function

$$H_{LP}(s) = \frac{k_{out}}{k_{CP}} \frac{1}{1 + \frac{s}{k_{CCO}k_{PD}k_{CP}}},$$
 (2)

where k_{CP} is the gain of the charge pump in the feedback path, which equals the charge pump current, and k_{PD} is the gain of the phase detector, which equals $1/2\pi$. The filter cutoff frequency is the product of the gains $\omega_c = k_{CCO}k_{PD}k_{CP}$. The DC gain of the filter is given by the ratio of the output gain coming from the output generation k_{out} and k_{CP} . If an output current is needed, a CP, as in Fig. 1, or a current mirror of I_{fb} can be used. The same methods can be used with a load resistor if an output voltage is required. Alternatively, the authors in [7] use a switch resistor circuit to generate the output voltage due to its high linearity compared to the other methods.

Finally, the filter is parallelised to extend the frequency range of the low-pass filter and reduce the impact of spurious tones. *N* evenly spaced phases are tapped out of the CCO and enter *N* PDs to produce *N* distinct PWM signals. The PWM signals drive a bank of charge pumps with shorted outputs. Shorting the outputs equals a summation of all the currents, resulting in a factor *N* increase in the transition density and

2N+1 current levels. The resolution increase leads to cancelling of all PWM tones up to NF_{sw} . In practice, perfect cancelation is impossible due to mismatches in the spacing of the different phases. Another benefit is the increased transition density of I_{fb} going back to the CCO. Because the switching density is increased with a factor of N, the switching receives more filtering in the CCO due to parasitic capacitance. This leads to a more stable frequency of the CCO.

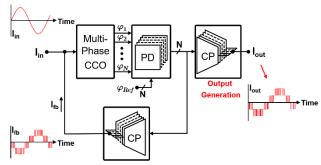


Fig. 1. Diagram of the multiphase time-based low-pass filter. The filter consists of a multiphase current controlled oscillator (CCO), a bank of N parallel phase detectors (PD), and two banks of N charge pumps (CP) with shorted outputs, one for the feedback current I_{fb} and one for the output generation. The waveform of I_{out} is seen in the small graph.

Results. To have a comparison for the high-pass and shelf filters presented in sections III and IV, a large signal simulation of the frequency response of the low-pass filter is conducted. The first-order low-pass filter is implemented in Cadence Virtuoso using Verilog-A to create behavioural models of all the blocks depicted in the circuit in Fig. 1. The PD and the CP are implemented in the same behavioural model to simplify the modelling. The CCO is designed to function as a differential ring oscillator. It outputs N=16 evenly spaced phases, each having an idle frequency of $F_{sw}=10$ MHz. The gains k_{CCO} and k_{CP} are picked such that the filter has a cutoff frequency of $f_c=10$ kHz, and k_{out} is set equal to k_{CP} to get a pass band gain of 0 dB.

To simulate the frequency response of the circuit, a small sinusoidal current is applied to I_{in} and a series of transient simulations with increasing frequency of the input current are conducted. Then, the fast Fourier transform (FFT) is calculated for each simulation to extract the magnitude and phase information needed for the Bode plots. Since the FFT needs at least one period of the input signal to be computed, the simulation time is dependent on the input frequency, causing the low-frequency simulations to take multiple hours to complete. When working with transistor-level simulations, a periodic AC simulation can be used instead to quickly obtain the same results.

Figure 2 shows the simulated frequency response along with the ideal small-signal response of the first-order low-pass filter. We find that the simulated response matches the ideal response, with no major deviations.

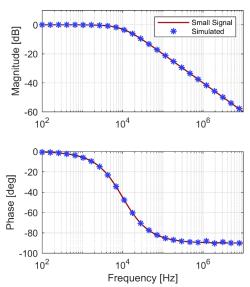


Fig. 2. Frequency response of the time-based first-order low-pass filter depicted in Fig. 1. The filter is designed to have a gain of 0 dB and a cutoff frequency of $f_c = 10 \, \text{kHz}$. The solid line shows the ideal small-signal response, and the dots show the simulated circuit.

Next, the large signal behaviour is simulated to determine how much distortion is introduced by processing the signal in the time-based domain. To do this, the circuit is simulated at its maximum output amplitude capabilities, which corresponds to 0%-100% duty cycle in PD. The input frequency is placed in the filter pass band.

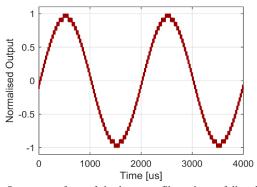


Fig. 3. Output waveform of the low-pass filter when a full-scale 500 Hz input is applied. The output is normalised by the input amplitude.

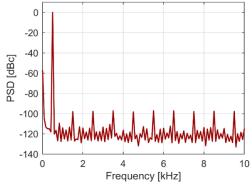


Fig. 4. Power spectrum of the first-order low-pass filter when a 500 Hz current is applied on the input. All harmonics are well suppressed by more than 90 dB inside the pass band.

For the low-pass filter, an input frequency of 500 Hz is used. Figure 3 shows the resulting full-scale (FS) output waveform, with all of the 33 current levels present. Figure 4 shows the power spectral density (PSD) of the waveform in Fig. 3. All harmonics are well suppressed inside the pass band, leading to a spur-free dynamic range (SFDR) of 97.04 dB. The total harmonic distortion (THD) is calculated on the basis of the first 10 harmonics and is found to be 0.003 %. This shows good linearity for the filter.

III. TIME-BASED HIGH-PASS FILTER

To obtain a high-pass filter behaviour, a zero at DC must be added to the low-pass filter transfer function in (2). This zero usually comes from a feedforward path that couples the filter input directly to the output, providing an instantaneous change in the output whenever the input changes. In the time domain, this can be achieved by introducing a controlled delay line (CDL) between the oscillator and the phase detector. A controlled delay line is made from a current-starved inverter delay line that provides a phase shift proportional to its control signal [15]. The behaviour can be described as follows

$$\phi_{CDL} = I_{in} k_{CDL}. \tag{3}$$

By suddenly changing the control current (I_{in}) to the CDL, a sudden change in ϕ occurs as the phase shift changes. This breaks the phase lock of the loop by moving ϕ out of alignment with ϕ_{Ref} , resulting in a spike in the duty cycle of the PWM signals coming out of the PDs. The spike is reflected in the output and causes a change in the frequency of the CCO. The frequency change moves ϕ back in alignment with ϕ_{Ref} leading to a phase lock. As the circuit approaches the phase lock, the duty cycle decreases, resulting in the output asymptotically going back to zero.

Adding a current-controlled delay line (CCDL) to each of the outputs of the CCO in our circuit leads to the updated time-based circuit shown in Fig. 5.

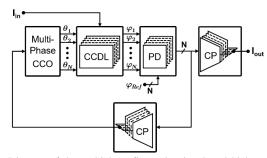


Fig. 5. Diagram of the multiphase first-order time-based high-pass filter. The main difference from the low-pass filter is the introduction of a current controlled delay line (CCDL).

Notice that the input current, in this case, only enters the filter through the controlled delay lines and that the CCO only has the feedback signal as the input. From this, the new transfer function can be derived to be (4)

$$H_{HP}(s) = \frac{k_{out}k_{CCDL}}{k_{CP}k_{CCO}} - \frac{s}{\frac{s}{k_{CCO}k_{PD}k_{CP}}}.$$
 (4)

Adding a bank of N parallel CCDLs is bound to increase the complexity and, thereby, the area and current consumption of the circuit. A single CCDL uses less current and area than the CCO. According to [7], the low-pass filter area is dominated by the CCO. Assuming that the current consumption follows the same trend, we estimate the area and current to increase somewhere between N/2 and N.

The technique of adding a zero using a controlled delay line has previously been used in time-based Op-Amps [4], where it is used to improve the phase margin.

Results. Like the low-pass filter, the high-pass filter is implemented in Cadence Virtuoso using behavioural Verilog-A blocks matching the circuit blocks in Fig. 5. The circuit uses 16 phases and has a switching frequency of 10 MHz. The high-pass filter is designed to have a cutoff frequency of $f_c = 10$ kHz by picking k_{CCD} and k_{CP} , accordingly. Likewise, k_{CCDL} and k_{out} are picked such that a pass band gain of 0 dB is achieved. Figure 6 shows the Bode plot of the high-pass filter with the ideal small-signal response. We find that the simulated response is nearly identical to the ideal response with no significant deviations and an attenuation of 20 dB/dec.

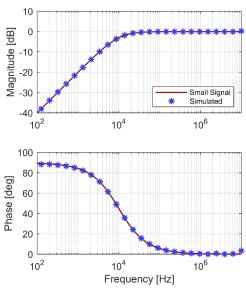


Fig. 6. Frequency response of the time-based first-order high-pass filter. The solid line shows the ideal response, and the dots show the simulated circuit. A good correlation between theory and simulation is observed.

Figure 7 shows the PSD of the high-pass filter when a 500 kHz FS input is applied. The spectrum is shown up to the switching frequency. Unlike the low-pass filter, this time, the harmonic content is significantly larger, with the second and third harmonics both being close to -60 dBc. This results in a THD of 0.156 %, equivalent to a 52 times increase compared to the low-pass filter. The SFDR is limited by the second harmonic to 56.74 dBc. The increase in THD is contributed to the higher frequency of the pass band and nonlinearities from the CCDL. When calculating the gain of the CCDL, it is assumed that the switching frequency is constant. However, since the CCDL sits in the feedback path in series with the CCO, constant change in the switching frequency affects the CCDL gain. This causes a nonlinear gain variation that leads to distortion.

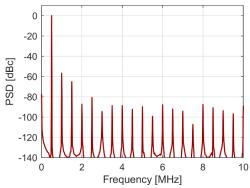


Fig. 7. Power spectrum of the first-order high-pass filter when a 500 kHz current is applied on the input. The second, third, and fifth are dominant.

IV. TIME-BASED SHELF FILTER

With the high-pass and low-pass filters derived, the two filters can be combined to form a shelf filter. To combine the two filters, the filter input simply connects to the CCO and the CCDL. Hence, the filter complexity remains the same as for the first-order high-pass filter. Figure 8 shows the combined filter, while (5) shows the resulting transfer function

$$H_{shelf}(s) = H_{LP}(s) + H_{HP}(s) = \frac{k_{out}}{k_{CP}} \frac{1 + s \frac{k_{CCDL}}{k_{CCO}}}{1 + \frac{s}{k_{CCO}k_{PD}k_{CP}}}.$$
 (5)

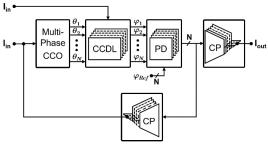


Fig. 8. Diagram of the multiphase first-order time-based shelf filter. The only difference from the high-pass filter is that the input enters both the CCO and the CCDL.

Since the denominator is the same for both H_{LP} and H_{HP} , it remains the same, and only the nominator is changed, which causes the zero to move from zero to $-k_{CCO}/k_{CCDL}$. The combination results in the low-pass filter response dominating at low frequencies while the high-pass filter dominates at high frequencies. Equations (6) and (7) show the gain for the low-frequency and high-frequency plateaus, respectively. These gains are identical to the pass band gains of the low-pass and high-pass filters discussed in Sections II and III:

$$G_{LP} = \lim_{s \to 0} H_{shelf}\left(s\right) = \frac{k_{out}}{k_{CP}},\tag{6}$$

$$G_{HP} = \lim_{s \to \infty} H_{shelf}(s) = k_{out} k_{PD} k_{CCDL}.$$
 (7)

By having different pass band gains for each filter, a

transition band is created around the cutoff frequency, where the gain changes from G_{LP} to G_{HP} as the frequency increases.

Results. Similar to the previous two filters, the shelf filter is implemented in Cadence Virtuoso using behavioural Verilog-A blocks according to the circuit in Fig. 8. The shelf filter is designed based on (6) and (7) to have a DC gain of 0 dB and a 20 dB drop in gain in the transition band, which spans one decade from 10 kHz to 100 kHz. Like the previous filters, 16 phases are used, and the switching frequency is 10 MHz. Figure 9 shows the simulated frequency response of the shelf filter with the ideal small-signal response. Once again, we find that the simulated response matches the ideal small-signal response.

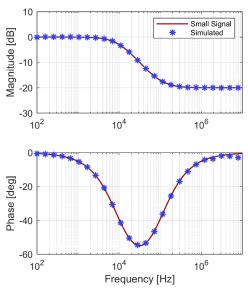


Fig. 9. Frequency response of the time-based first-order shelf filter. The solid line shows the ideal small-signal response, and the dots show the simulated circuit. Once again, a good correlation is observed.

Finally, Fig. 10 shows the PSD of the shelf filter for a 500 Hz FS tone placed in the pass band.

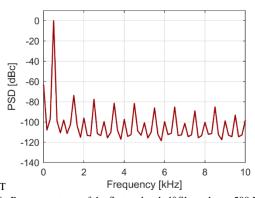


Fig. 10. Power spectrum of the first-order shelf filter when a $500~\mathrm{Hz}$ current is applied to the input.

he amplitude of the harmonics is in between the results from the low-pass filter and the high-pass filter with an SFDR of 73.80 dBc and a THD of 0.027 %, equivalent to 9 times the low-pass filter. As the shelf filter has two plateaus, the THD and SFDR are also tested for 500 kHz. Here, the SFDR is 57.01 dBc, and the THD is 0.141 %, which is similar to the performance of the high-pass filter. The reason why the distortion is lower at lower frequencies is due to the integrating behaviour of the CCO. The input of the CCDL can

be considered a disturbance to the system that the integrator tries to suppress. At low input frequencies, the open-loop integrator gain is higher. This leads to attenuation of the CCDL input, thereby achieving the high-pass filter effect, but the increased gain also provides a stronger feedback linearisation, resulting in lower distortion.

V. TIME-BASED SECOND-ORDER FILTERS

The first-order filters presented in Sections II to IV can be extended to higher-order filters by cascading the filter and applying a minor modification to the feedback. Figure 11 shows an example of a time-based second-order filter.

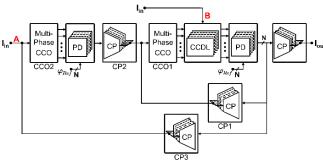


Fig. 11. Diagram of a generalised second-order multiphase time-based filter. "A" and "B" indicate the two input ports to the filter. All feedback paths are taken from the output of the last stage in the filter.

The filter consists of an inner loop (CCO1, CCDL, and CP1) identical to the first-order shelf filter, and an outer loop containing CCO2, CP2, and CP3. Two input ports (A and B) are present, with A entering the outer loop and B the inner loop. Applying the input to A, a second-order low-pass filter is obtained. A similar configuration is also reported in [7], with the main difference being the lack of the CCDL since it can be omitted for the low-pass filter. In the same manner, connecting the input only to B leads to a second-order high-pass filter. Equations (8) and (9) show the transfer function for port A and B, respectively:

$$H_{A}(s) = \frac{k_{out}k_{1}k_{2}}{s^{2} + k_{CP1}k_{1}s + k_{1}k_{2}},$$
 (8)

$$H_{B}(s) = \frac{k_{out}k_{CCDL}s^{2}}{s^{2} + k_{CPL}k_{1}s + k_{1}k_{2}},$$
(9)

where k_1 and k_2 are lumped gains as given by (10)

$$\begin{vmatrix} k_1 = k_{CCO1}k_{PD} \\ k_2 = k_{CP3}k_{CCO2}k_{PD}k_{CP2} \end{vmatrix}.$$
 (10)

The transfer functions (8) and (9) have the structure of second-order prototype filters, which means that the filters can be described by a damping ratio ζ and a cutoff frequency ω_c given by the relations in (11)

$$\begin{bmatrix} k_1 = \frac{2\zeta\omega_c}{k_{CP1}} \\ k_2 = \frac{\omega_c k_{CP1}}{2\zeta} \end{bmatrix}. \tag{11}$$

As a result, complex pole pairs can be achieved, enabling

increased filtering options compared to the first-order filters. Besides low-pass and high-pass filters, the structure in Fig. 11 also allows for other filter structures by applying the input signal to both ports simultaneously, as was the case with the first-order shelf filter. These filters include, among others, a notch filter (12) and a shelf filter (13):

$$H_{notch}(s) = H_A(s) + H_B(s) =$$

$$= \frac{k_{out}(k_1 k_2 + k_{CCDL} s^2)}{s^2 + k_{CP1} k_1 s + k_1 k_2},$$
(12)

$$H_{shelf}(s) = H_{A}(s) - H_{B}(s) = \frac{k_{out}(k_{1}k_{2} - k_{CCDL}s^{2})}{s^{2} + k_{CPI}k_{1}s + k_{1}k_{2}}.$$
(13)

A commonality for the combined filters is the limited control of the damping of the zeros due to the missing first-order term in the nominator. As a result, the two zeros can be made either purely imaginary or real-valued with one zero in the right half-plane (RHP) and one in the left half-plane (LHP). The imaginary zeros are obtained by summing the two inputs as done with the notch filter in (12). Similarly, the real-valued zeros are obtained by applying the inverted current to one of the inputs, as done for the shelf filter in (13). However, since the zeros in the shelf filter are real, the damping for the zeros will always be $\zeta = 1$.

Results. To complete the section concerning the second-order filters, simulations of the frequency responses for the high-pass, notch, and shelf filter are provided. The used setup is similar to the first-order filters, with the use of 16 phases and a switching frequency of 10 MHz. As previously, Cadence Virtuoso and Verilog-A are used to implement the filters using behavioural models of each block corresponding to the blocks shown in Fig. 11.

Figure 12 shows the second-order high-pass filter when $\omega_c = 10 \times 2\pi \ \text{ms}^{-1}$ and $\zeta = 0.5$, resulting in a slightly underdamped response. The simulated results follow the small-signal model and reproduce both the small resonance peak and the 40 dB/dec attenuation all the way to -80 dB.

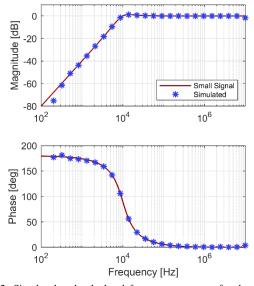


Fig. 12. Simulated and calculated frequency response for the time-based second-order high-pass filter.

Figure 13 shows the PSD of the second-order high-pass filter when a 500 kHz tone is applied. The THD is 0.155 % and the SFDR is 56.79 dBc. The magnitude of the harmonics and the distortion is similar to that of the first-order high-pass filter suggesting that the outer loop of the second-order filter has a limited impact on the distortion and the distortion remains dominated by the CCDL.

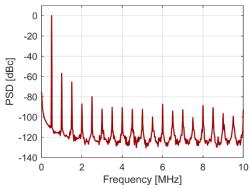


Fig. 13. Power spectrum of the second-order high-pass filter when a 500 kHz current is applied on the input. The magnitudes of the harmonics are comparable to the first-order high-pass filter.

Figure 14 shows the notch filter (12) with a damping ratio of $\zeta = 1$. For this filter, the damping ratio determines the width of the notch and, thus, how concentrated the attenuation should be. The simulated response reproduces the small-signal response well and reaches a peak attenuation of -58.79 dB at 10 kHz. At 10 kHz, the nominator in (12) is zero, leading to –inf dB. However, due to the changing delay and frequency of the time-based circuit introducing nonlinear behaviours, complete cancelation cannot be realised.

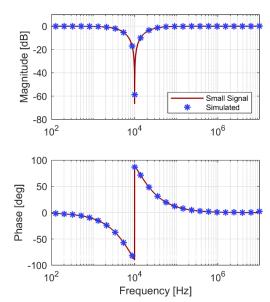


Fig. 14. Simulated and calculated response for the time-based notch filter. The simulated response reaches a peak attenuation of -58.79 dB.

Figure 15 shows the PSD of the notch filter with the same test conditions as the high-pass filters. The THD is 0.313 %, and the SFDR is 50.64 dBc. Here, the THD is doubled and the SFDR is halved compared to the high-pass filters. Inspecting the power spectrum, the relative magnitude of all the harmonics remains the same as the high-pass filter, but the general level has increased by 6 dB.

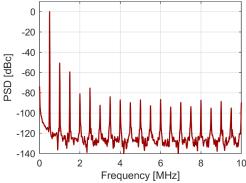


Fig. 15. Power spectrum of the notch filter when a 500 kHz current is applied on the input. The magnitude of the harmonics is 6 dB larger than that of the high-pass filter.

Lastly, Fig. 16 shows the second-order shelf filter (13) with $\omega_c = 100 \times 2\pi \text{ ms}^{-1}$ and $\zeta = 1$, and Fig. 17 shows the PSD.

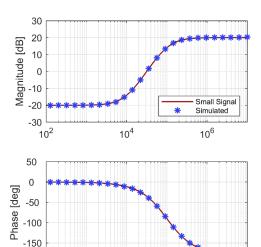


Fig. 16. Simulated and calculated frequency response for the second-order shelf filter.

Frequency [Hz]

10⁴

10⁶

-200

10²

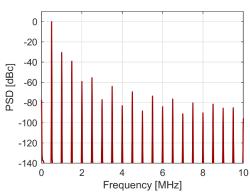


Fig. 17. Power spectrum of the second-order shelf filter when a 500 kHz current is applied on the input. All harmonics are significantly larger than any of the other filters.

Looking at Fig. 16, the transition band spans from 10 kHz to 100 kHz, where the gain changes with 40 dB/dec, showing a second-order response. The simulated response matches exactly with the calculated small-signal response. The phase shift does not follow the same trajectory as the first-order shelf filter because this filter has a zero in the RHP, leading to a -90-degree phase change. As a result, the phase transitions from 0 degrees to -180 degrees throughout the

transition band.

Looking at the PSD in Fig. 17, we find that the harmonics are significantly larger than what has been observed for any of the other filters. Most harmonics are greater than -80 dB and both the second and third harmonics are greater than -40 dB. As a result, the THD becomes 3.157 %, which is 20 times larger than the second-order high-pass filter, and the SFDR becomes 30.60 dBc. It seems that the fact that the two inputs (A, B) swing with an opposite sign causes larger frequency swings in CCO1, which in turn provides a stronger excitation to the nonlinear gain of the CCDL, causing more distortion.

VI. NONIDEAL SYSTEM BEHAVIOURS

A. CCDL

In the previous sections, we observed that the CCDL leads to a substantial increase in the THD compared to the first-order low-pass, indicating that a nonlinear effect is at play. Table II provides a summary of the reported THD and SFDR for all tested filters.

TABLE II. SUMMARY OF THE REPORTED THD AND SFDR FOR ALL TESTED FILTERS.

Type	THD [%] (dB)	SFDR [dBc]
First Low-Pass	0.003 (-91.59)	97.04
First High-Pass	0.156 (-56.12)	56.74
First Shelf @500 Hz	0.027 (-71.36)	73.80
First Shelf @500 kHz	0.141 (-57.01)	57.01
Second High-Pass	0.155 (-56.19)	56.79
Second Notch	0.313 (-50.09)	50.64
Second Shelf	3.157 (-30.01)	30.60

Table II provides three key takeaways:

- 1. The first-order and second-order high-pass filters, as well as the first-order shelf filter at 500 kHz, all perform identically;
- 2. The THD and SFDR improve for the first-order shelf filter as the test frequency is decreased;
- 3. The notch filter and the second-order shelf perform significantly worse than any of the other filters.

The first point clearly shows that the introduced nonlinearity stems from the CCDL, and the contribution remains the same across all the filters. This also means that increasing the order of the high-pass filter does not impact the amount of distortion in either direction.

The second point shows that the control input of the CCDL behaves as a disturbance to the system that is compensated by the CCO. From an open-loop perspective, the filter is an integrator with infinite gain at DC. Thus, the lower the frequency of the test tone, the more gain the filter will have to suppress any nonlinearities introduced. As the test tone frequency increases, the distortion will increase until the frequency variation of the CCO becomes sufficiently small to impact the gain of the CCDL.

The third point indicates that the control current that enters CCO1 can easily be amplified when using second-order filters and higher, especially when multiple inputs are used for the filter, as is the case with the notch and second-order shelf filter. This leads to larger frequency changes from CCO1, negatively impacting the distortion and dynamic range.

It should be possible to circumvent the introduced nonlinearities from the CCDL by constructing the filter in a differential manner. However, this remains to be tested.

B. Switching Frequency

As the frequency increases, it will, at some point, reach the Nyquist frequency. At this point, the conversion from current to time will start to degrade, since more signal information needs to be encoded into each switching cycle, effectively limiting the quality of the signal representation. As a result, artefacts due to cycle slipping [20] can occur for inputs of a large amplitude. By limiting the amplitude, fewer current levels are needed to represent the output. This leads to an increased transition density for the remaining levels, artificially increasing the switching frequency. Hence, for smaller amplitudes, it is possible to extend the pass band of the high-pass filter beyond the switching frequency.

VII. CONCLUSIONS

This paper introduced time-based first-order and secondorder high-pass filters and shelf filters, as well as a secondorder notch filter. The filters are based on an existing timebased low-pass filter structure that employs a multiphase controlled ring oscillator with phase detectors. By adding controllable delay lines between the oscillator and the phase detector, we showed that one or more zeros corresponding to the number of poles are introduced to the system transfer function. When the filter input is connected to the controlled delay lines, a high-pass filter is created, and when the input is connected to both the controlled oscillator and delay line, a shelf filter or a notch filter is created depending on the sign of the two input currents. Simulations of the filter frequency responses matched the theory well. Power spectrums, together with total harmonic distortion, were simulated for all filters. Results showed that the controllable delay line increased the amount of distortion from 0.003 % for the firstorder low-pass filter up to 0.16 % for the first-order high-pass and shelf filter and the second-order high-pass filter. The notch filter and the second-order shelf filter had twice and 20 times more distortion, respectively, making them less attractive. The derivation of the new filter types allows the creation of complex high-order time-based filters by combining multiple first-order and second-order filters.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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