Novel Lossless Positive-/Negative-Grounded Capacitance Multipliers Using VCII

Mohammad Faseehuddin[1, *], Sadia Shireen[1], Sawal Hamid Md Ali[2], Worapong Tangsrirat[3]
[1]Faculty of Engineering, Symbiosis Institute of Technology (SIT),
Symbiosis International University (SIU),
Lavale, Mulshi, Pune, Maharashtra 412115, India
[2]Department of Electrical, Electronic and Systems Engineering, Universiti Kebangsaan Malaysia,
Bangi 43600, Selangor, Malaysia
[3]Department of Instrumentation and Control Engineering, School of Engineering,
King Mongkut's Institute of Technology Ladkrabang (KMITL),
Bangkok 10520, Thailand
[*]mohammad.faseehuddin@sitpune.edu.in, sadia.shireen.phd2021@sitpune.edu.in,
sawal@ukm.edu.my, worapong.ta@kmitl.ac.th

***Abstract*—In the presented research, the second-generation voltage conveyor (VCII) is used in the design of active capacitance multipliers. In this paper, three positive and one negative lossless grounded capacitance multipliers (GCMs) are designed. All of these GCMs are designed using two VCIIs, one capacitor, and two resistors. There is no need for any passive component matching to implement a GCM. The multiplication factor of GCMs can be set/varied by changing the values of two resistances as per requirement. Considering nonideal constraints, GCMs are analysed mathematically to evaluate the effect of nonideal current and voltage transfer gains on the performance of the proposed GCMs. Also, parasitic analysis is conducted to study the effect of VCII node impedance on the performance of the presented GCMs. The simulation analysis is performed using Cadence Virtuoso in 0.18 µm Silterra Malaysia process design kit (PDK). Additionally, the macro-model of commercially available integrated circuit, AD844, is used to design the proposed GCM-2 to further prove the theoretical findings.**

***Index Terms*—Grounded capacitance multiplier (GCM); Lossless capacitance multiplier; Second-generation voltage conveyor (VCII); Multiplication factor.**

I. INTRODUCTION

The passive capacitor occupies a large silicon area on the chip and once fabricated, its value cannot be altered or tuned [1]–[3]. This makes the integrated circuit (IC) fabrication of large-value capacitors difficult and impractical. On the other hand, active capacitors with adjustable values can be designed. Active analogue blocks (AABs) along with passive elements such as resistors and small-value capacitors can realise large capacitance [1]–[20]. Active capacitance multipliers (CMs) can be easily fabricated on chip due to the small value of the passive capacitor required. Additionally, the capacitance can be tuned by setting the values of resistors and transconductance (g_m) of the ABBs. Active CMs are frequently used in phased lock loops [1], frequency filters [1]–[4], sensors [5]–[8], biological circuits [2], etc. It is very clear from the literature that CM circuits can be designed employing various current mode/voltage mode ABB, such as operational transconductance amplifier (OTA) [3], [4], voltage differencing buffered amplifier (VDBA) [6], second-generation current controlled conveyor (CCCII) [8], dual X second-generation current conveyor (DXCCII) [9], current amplifier (COA) [10], voltage conveyor VCII- [14], etc.

In the recent past, researchers have started employing the second-generation voltage conveyor (VCII) which is a counterpart of the second-generation current conveyor (CCII). Although the concept of VCII [12]–[15] was discussed almost two decades ago in 2004 by the authors in [16]. The ABB has recently become popular among researchers in lieu of simple circuit level implementation, high range of operating frequency, low power consumption, small chip area and availability of low impedance voltage output/current input terminals and high impedance current output/voltage input terminals. VCII is best suited for circuits whose outputs are obtained in voltage form. Furthermore, the addition and subtraction of current signals can be easily performed using VCII. Owing to its simple structure, the VCII does not require complex complementary metal-oxide-semiconductor (CMOS) implementation, thus reducing the number of transistors leading to reduced parasitic effects, increased in bandwidth, and smaller chip area.

According to the value of the realised capacitors, the CMs can be classified as positive [11] or negative [14]. Table I presents a comparative analysis of the proposed CMs with designs available in the literature. In this research, three positive- and one negative-grounded capacitance multipliers (GCMs) are designed using two VCIIs, one capacitor, and two resistors. The presented designs do not require the matching of passive elements. When the resistance value is adjusted, the multiplication factor can be easily tuned. The VCII is designed and simulated using Cadence Virtuoso using 0.18 µm Silterra Malaysia process design kit (PDK).

Manuscript received 16 January, 2023; accepted 5 June, 2023.
This research was supported by UKM, Malaysia under Grant No. GUP-2020-009.

The theoretical and simulation results exhibit close resemblance. Additionally, for proof of concept, the AD844 integrated circuit behavioural model is used to design VCII and capacitance multiplier circuits in PSpice software.

TABLE I. COMPARATIVE ANALYSIS OF SOME STATE-OF-THE-ART CAPACITANCE MULTIPLIERS.

Ref. No.	No. of ABB	No. of R + C	Floating Capacitor	Supply Voltage	Technology Used	Emulator Type
[2]	2-CFOA	2 + 1	Yes	±10 V	BJT (AD844)	Positive
[3]	2-OTA and 2-Current Mirror	0 + 1	Yes	±5 V	BJT	Positive
[4]	2-OTA	1	Yes	2.2 V	CMOS 0.5 µm	Positive
[5]	2-OTA	0	Yes	NA	BJT (CA3280)	Positive
[6]	2-VDBA	0 + 1	Yes	±0.75 V	CMOS 0.25 µm	Positive
[7]	2-CFOA	2 + 1	No	± 9 V	BJT (AD844)	Positive
[8]	3-CCCII	1 + 1	No	± 2.5 V	BJT	Positive
[9]	1-DXCCII	0 + 1	Yes	±1.65 V	CMOS 0.35 µm	Positive
[10]	1-CCII-, 1-COA	2 + 1	No	±1.5 V	CMOS 0.5 µm	Positive
[11]	2-CFOA (Fig. 2)	2 + 1	No	± 2.5 V	CMOS 0.35 µm	Negative
[14]	2-VCCII	2	Yes	±1.65 V	CMOS 0.35 µm	Positive/Negative
[18]	1-OTA, DVB	1 + 1	Yes	±5 V	BJT (AD844)	Positive
[19]	1-CFOA, 1-OTA	0 + 1	No	±5 V	BJT (AD844), LM13700N	Positive
Proposed	2-VCCII	2	Yes	±0.9 V	CMOS 0.18 µm	Positive/Negative

II. SECOND-GENERATION VOLTAGE CONVEYOR (VCII)

The second-generation voltage conveyor (VCII) is a simple and compact three-terminal active block. The VCII [12]–[15] is composed of current and voltage followers. The block diagram of the VCII is depicted in Fig. 1. The Y terminal is the low impedance current input terminal, the X terminal is the high impedance current output (voltage input) terminal, and the Z terminal is the low impedance voltage output terminal. Equations (1)–(4) give the current-voltage relations of the VCII:

$$I_X = I_Y, \tag{1}$$

$$I_X = -I_Y, \tag{2}$$

$$V_X = V_Z, \tag{3}$$

$$V_Y = 0. \tag{4}$$

In the case of VCII+, $I_X = I_Y$, and for VCII-, $I_X = -I_Y$.

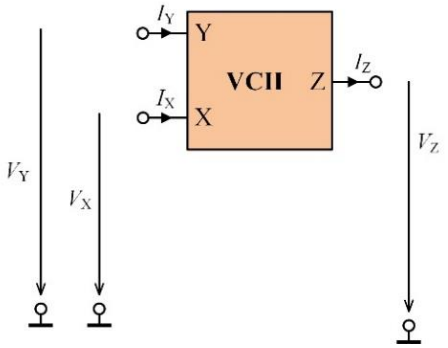


Fig. 1. Symbolic representation of VCII.

The CMOS implementation of VCII+/- is shown in Fig. 2 [15]. The transistors M_1 to M_7 form the current follower, and transistors M_8 to M_{12} form the voltage buffer. In Fig. 2(b), the VCII- implementation is presented, M_{13}, M_{14}, M_{B7}, and M_{B6} provides the current reversal. Transistors M_{B0} to M_{B5} establish the necessary bias currents in the circuit.

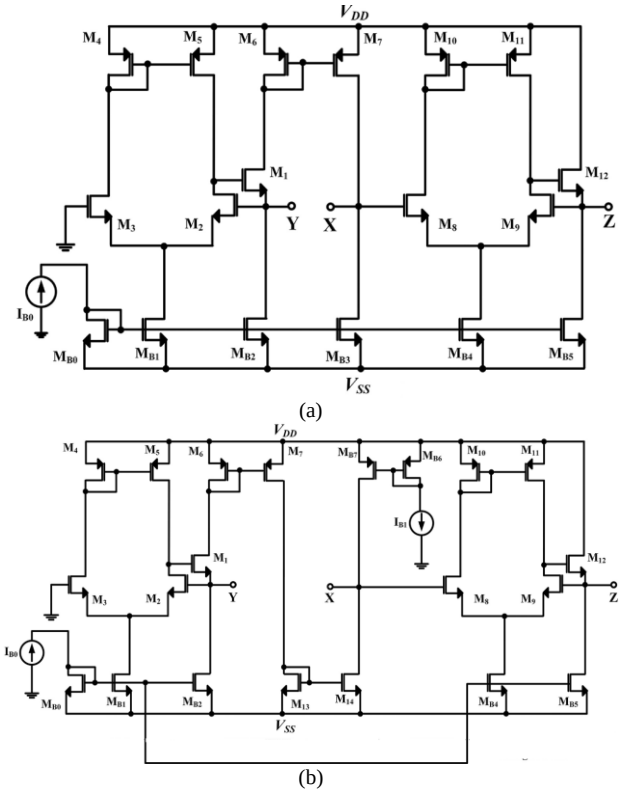


Fig. 2. CMOS implementation of (a) VCII+ and (b) VCII-.

III. PROPOSED GROUNDED CAPACITANCE MULTIPLIERS

Three positive GCMs and one negative GCM are proposed as presented in Fig. 3(a)–(d). The designs utilise two VCIIs+/-, one capacitor C_1, and two resistors R_1 and R_2. The GCM-1, GCM-3, and GCM-4 realise positive capacitance. Negative capacitance simulator (GCM-2) is obtained by replacing VCII- with VCII+ in GCM-1. Negative GCM-2 can be used to cancel parasitic capacitance present in any circuit. In all four GCMs, the capacitance is realised at port X. The GCMs do not require any kind of passive component matching. Table II gives the expression

for the realised capacitance. The multiplication factor (K) can be varied according to the resistance values R_1 and R_2.

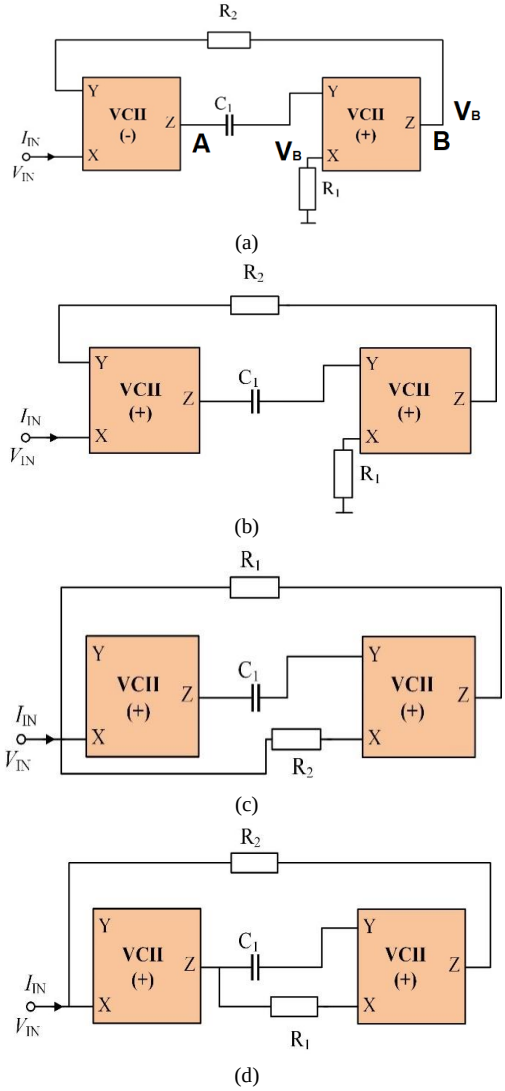


Fig. 3. Proposed capacitance multipliers: (a) GCM-1; (b) GCM-2; (c) GCM-3; (d) GCM-4.

The analysis of GCM-1 is as follows.
Applying KCL at node B:

$$I_{Y1} = \frac{V_B - 0}{R_2} = I_{IN}, \tag{5}$$

$$I_{IN} = \frac{V_B}{R_2}. \tag{6}$$

Applying KCL at node A:

$$V_{Z1} = V_{X1} = V_{IN}, \tag{7}$$

$$I_{Y2} = I_{X2} = V_{IN} sC_1 = \frac{0 - V_B}{R_1}, \tag{8}$$

$$V_{IN} sC_1 R_1 = -V_B. \tag{9}$$

Putting the value of V_B in (6) we get

$$C_{eq} = \frac{I_{IN}}{V_{IN}} = -\frac{sC_1 R_1}{R_2}. \tag{10}$$

In a similar fashion, taking both the first and second VCII as positive, a negative capacitance multiplier is obtained. The analysis procedure is similar to that followed to examine GCM-1.

TABLE II. EXPRESSIONS FOR THE REALISED IMPEDANCE.

GMC No.	Expression of Capacitance	Multiplication Factor
GCM-1	$C_{eq} = sC_1\left(\frac{R_1}{R_2}\right)$	$K = \left(\frac{R_1}{R_2}\right)$
GCM-2	$C_{eq} = -sC_1\left(\frac{R_1}{R_2}\right)$	$K = -\left(\frac{R_1}{R_2}\right)$
GCM-3	$C_{eq} = sC_1\left(1+\frac{R_2}{R_1}\right)$	$K = \left(1+\frac{R_2}{R_1}\right)$
GCM-4	$C_{eq} = sC_1\left(\frac{R_1}{R_2}\right)$	$K = \left(\frac{R_1}{R_2}\right)$

IV. NONIDEAL ANALYSIS

Considering the effect of frequency-dependent current and voltage transfer gains on the operation of the VCII, the V-I relations of the VCII will be modified as $I_X = \beta_j I_Y = -\beta_j' I_Y$, $V_X = a_i V_Z$, and $V_Y = 0$, where j = 1, 2 indicates the number of VCII. We can also represent $\beta_j = 1 - \varepsilon_i$ and $a_j = 1 - \varepsilon_v$, where ε_i and ε_v ($|\varepsilon_i| << 1$ *and* $|\varepsilon_v| << 1$) signify the current and voltage tracking errors. Ideally, $\beta = \beta' = \alpha = 1$. The nonideal voltage and current transfer gains cause deviations in the realised values of the capacitor multiplier. To study the effect of tracking errors, a reanalysis of the proposed circuits is carried out. The modified values of the impedances are presented in (11)–(14):

$$\frac{I_{IN}}{V_{IN}} = -\frac{sC_1 R_1 \alpha_1 \alpha_2 \beta_1' \beta_2}{R_2}, \tag{11}$$

$$\frac{I_{IN}}{V_{IN}} = -\frac{sC_1 R_1 \alpha_1 \alpha_2 \beta_1 \beta_2}{R_2}, \tag{12}$$

$$\frac{I_{IN}}{V_{IN}} = sC_1 \alpha_1 \alpha_2 \beta_2 \left(1+\frac{R_2}{R_1}\right) + \frac{(R_1+R_2)}{R_1 \times R_2} - \alpha_2 \left(\frac{R_1+R_2}{R_1 \times R_2}\right), \tag{13}$$

$$\frac{I_{IN}}{V_{IN}} = sC_1 \alpha_1 \alpha_2 \beta_2 \left(\frac{R_1}{R_2}\right) + \frac{\alpha_2}{R_2} - \left(\frac{\alpha_1 \alpha_2}{R_2}\right). \tag{14}$$

V. PARASITIC ANALYSIS

Figure 4 depicts the nonideal model of the VCII± together with the parasitic elements. R_Y is the parasitic resistance associated with the low impedance of the input current at the Y terminal. R_Z is the parasitic resistance associated with the Z terminal of the low-impedance voltage output. In an ideal condition, both R_Y and R_Z are equal to zero. Parallel parasitic resistances R_X and parasitic capacitance C_X are the parasitics associated with the high-impedance current output terminal X, which is equivalent to infinity in a perfect condition. This section explores the influence of parasitic impedance on the simulator circuits indicated in Fig. 3.

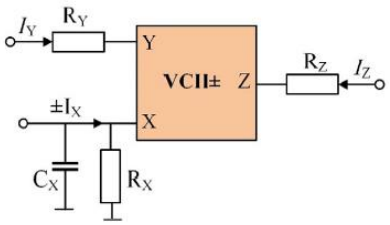


Fig. 4. Nonideal equivalent circuit of VCII± including parasitics.

Taking into account the parasitic impedances of the VCII±, the input impedance of the GCM-1 and GCM-2 circuits in Fig. 3 can be found as

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \pm \left[\frac{1}{sC_1\left(\frac{R_1'}{R_2'}\right)} + \frac{(R_{Z1} + R_{Y2})}{R_1'} \right] \left(1 + sR_1'C_{X2}\right), \quad (15)$$

where $R'_1 = R_1//R_{X2}$ and $R'_2 = R_2 + R_{Y1} + R_{Z2}$. Equation (15) shows that the VCII± parasitics have a direct effect on the frequency performance of the proposed GCM-1 and GCM-2 circuits. Practically, $R_1 << R_{X2}$, $R_1 >> (R_{Z1} + R_{Y2})$, and $R_2 >> (R_{Y1} + R_{Z2})$, (15) can be approximated as

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \pm \left[\frac{(1 + sR_1C_{X2}}{sC_1\left(\frac{R_1}{R_2}\right)} \right]. \quad (16)$$

Assuming $j\omega$ is substituted for s in (16), the frequency limitation of the proposed GCM-1 and GCM-2 circuits in Fig. 3 can be expressed as

$$\omega << \min \left| \frac{1}{R_1C_{X2}} \right|. \quad (17)$$

In the same way, an examination of the proposed GCM-3 that incorporates parasitic impedance effects yields the following input impedance function

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \left[\frac{1 + s(R_{Z1} + R_{Y2})C_1}{sC_1\left(1 + \frac{R_2}{R_1'}\right)} \right], \quad (18)$$

where $R'_1 = (R_1 + R_{Z2})$. Since $R_1 >> R_{Z2}$, the simulator can perform as a lossless grounded capacitance multiplier for the frequency range of operation as

$$\omega << \min \left| \frac{1}{(R_{Z1} + R_{Y2})C_1} \right|. \quad (19)$$

Furthermore, considering the parasitic effects on the proposed GCM-4 simulator in Fig. 3 its input admittance can be written as

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \left[\frac{1 + sR_{Y2}C_1}{sC_1\left(\frac{R_2}{R_1'}\right)} \right]. \quad (20)$$

As a result of (20), the useful frequency of the circuit in this case will be constrained by

$$\omega << \min \left| \frac{1}{R_{Y2}C_1} \right|. \quad (21)$$

VI. Simulation Results

To verify the proposed capacitance multiplier circuits, the VCII is designed in 0.18 µm Silterra Malaysia technology for a supply voltage of ±0.9 V. The width of the NMOS transistor is taken as 13.5 µm, and for PMOS, it is set at 40.5 µm. The length of both NMOS and PMOS is fixed at 0.54 µm [15]. The simulation analysis is done in the Cadence Virtuoso design software. The bias currents of the VCII are taken to be $I_{bias1} = I_{bias2} = 25$ µA. AC analysis is performed to evaluate the current and voltage gain and bandwidth of VCII as presented in Fig. 5(a) and Fig. 5(b). Parasitic resistance associated with the Y, X, and Z nodes is also determined by AC analysis, as shown in Fig. 6(a) and Fig. 6(b). The important design parameters of the designed VCII are summarised in Table III.

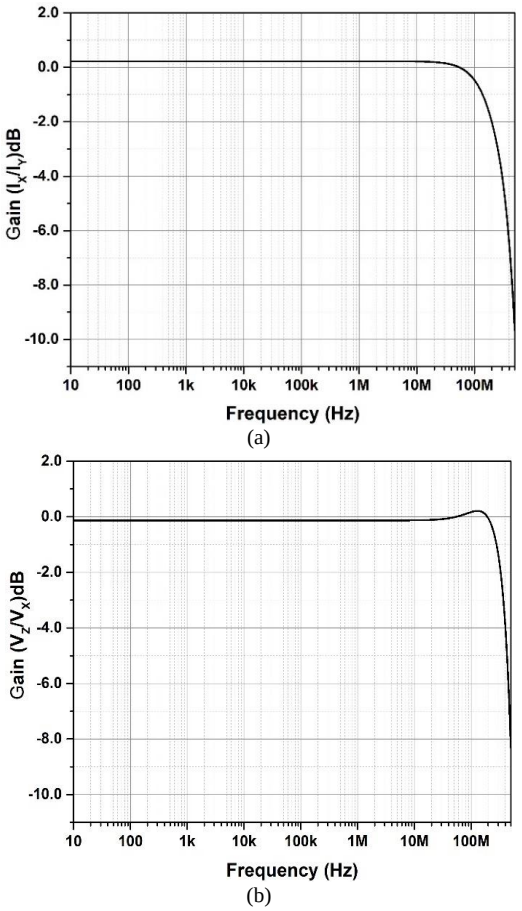
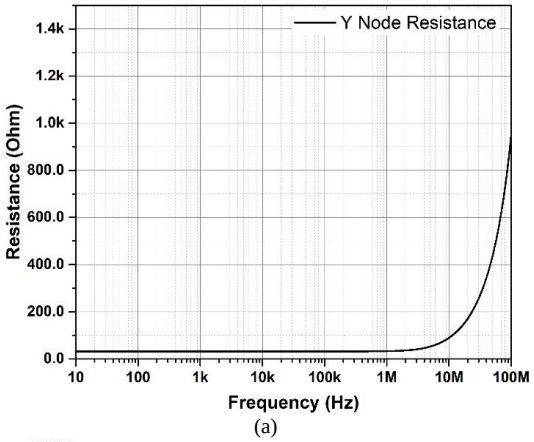
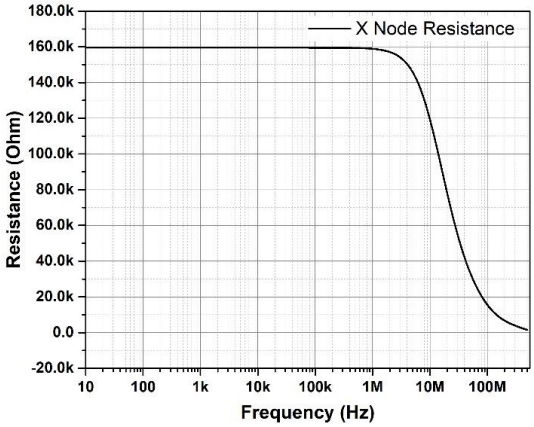


Fig. 5. AC analysis: (a) Current transfer bandwidth; (b) Voltage transfer bandwidth.



(a)



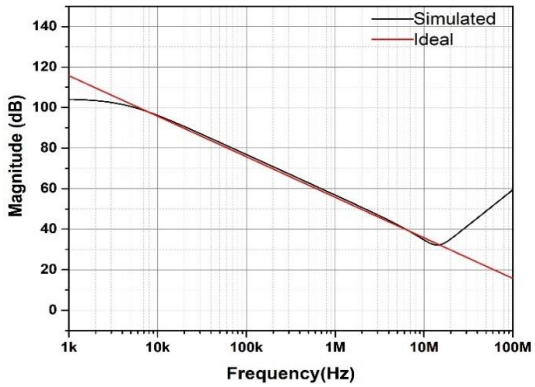
(b)

Fig. 6. AC analysis: (a) Y-node resistance; (b) X-node resistance.

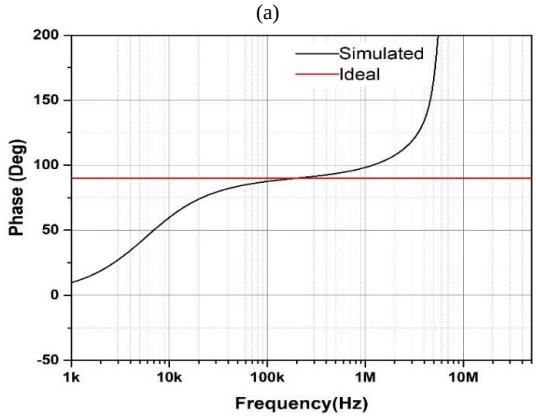
TABLE III. PERFORMANCE PARAMETERS OF VCII.

Parameters	Values
Parasitic at nodes Y @1 KHz	31.164 Ω
Parasitic at nodes X @1 KHz	159.88 kΩ
Parasitic at nodes Z @1 KHz	31.76 Ω
Current transfer gain	1.02
Voltage transfer gain	0.98
DC Voltage range	±400 mV
DC Current range	±45 µA
Current transfer bandwidth	254.09 MHz
Voltage transfer bandwidth	371.52 MHz

The negative capacitance multiplier GCM-2 is designed first for the multiplier factor K = 5.2 by selecting $R_1 = 26\,k\Omega$, $R_2 = 5\,k\Omega$, and $C_1 = 50\,pF$. The realised capacitance is 260 pF. The simulated and ideal magnitude and phase responses of GCM-2 are presented in Fig. 7(a) and Fig. 7(b). It can be seen from the figures that the multiplier works up to 10 MHz. To further validate the functionality of the capacitance multiplier, time domain analysis is performed. A sinusoidal signal of 100 mVp-p is applied at the input, and the resulting output current is measured as presented in Fig. 8(a). The phase difference of 90^0 between current and voltage verifies the correct functioning of the GCM-2. The Lissajous curve given in Fig. 8(b) further validates the phase difference. Now, the magnitude and phase of GCM-1 for (K = 5.2) are plotted for temperatures of 25 °C, 50 °C, 75 °C, and 100 °C to study the effect of temperature on the performance of GCM-1. It can be inferred from Fig. 9(a) and Fig. 9(b) that the realised capacitance remains almost constant.

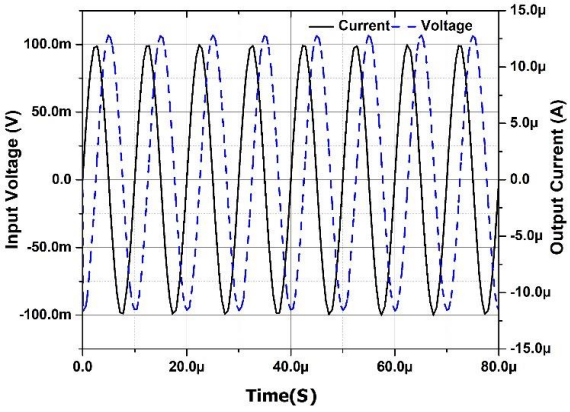


(a)

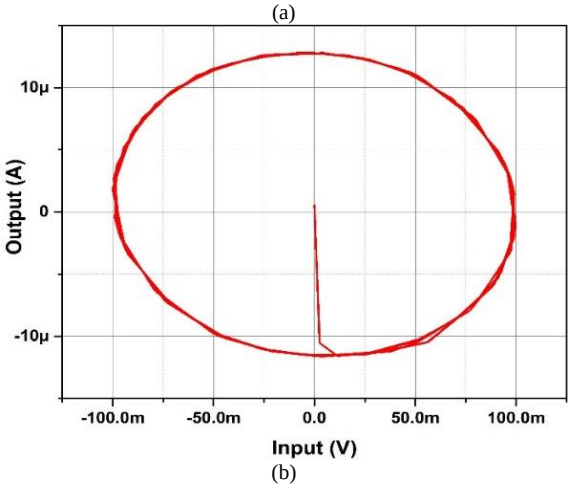


(b)

Fig. 7. Ideal and simulated response of GCM-2: (a) Magnitude response; (b) Phase response.



(a)

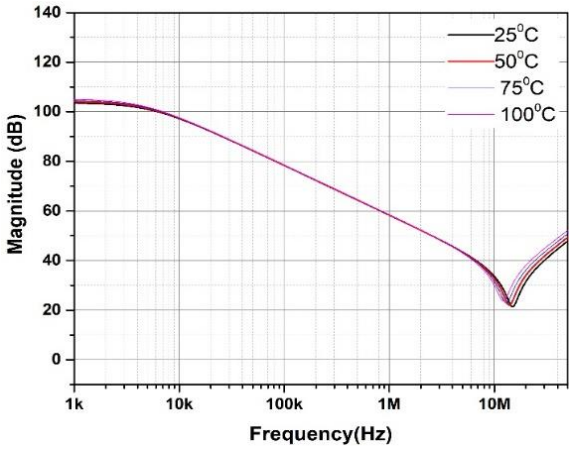


(b)

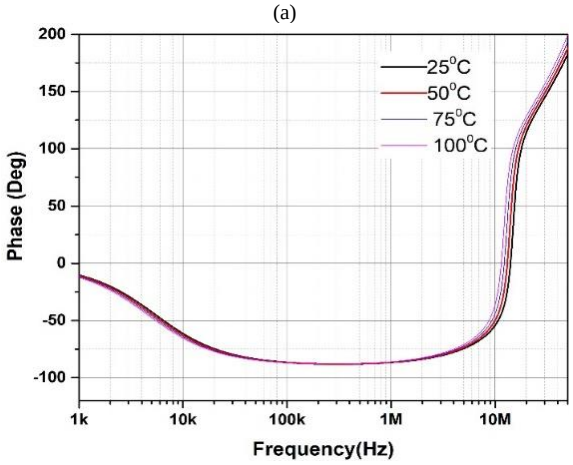
Fig. 8. Analysis of the time domain of GCM-2: (a) Transient response; (b) Lissajous curve.

To further study the performance of the proposed capacitance multiplier (GCM-2) under process variations, Monte Carlo analysis is conducted with 200 runs for GCM-2. It can be deduced from the results presented in Fig. 10(a) and Fig. 10(b) that the proposed design is not significantly affected.

The GCM-1, which is a positive capacitance multiplier, is again designed for the multiplication factor of K = 4 by selecting $R_1 = 20\,k\Omega$, $R_2 = 5\,k\Omega$, and $C_1 = 50\,pF$. The simulated and ideal magnitude responses of GCM-1 are presented in Fig. 11.

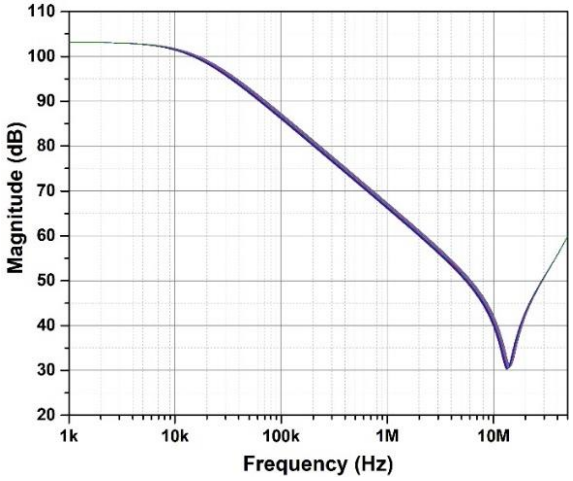


(a)

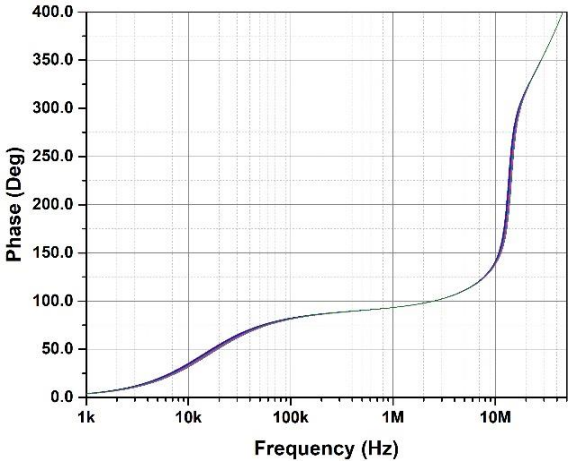


(b)

Fig. 9. GCM-1 frequency response for different temperatures: (a) Magnitude response; (b) Phase response.



(a)



(b)

Fig. 10. Monte Carlo analysis of GCM-2 for 200 runs: (a) Magnitude response; (b) Phase response.

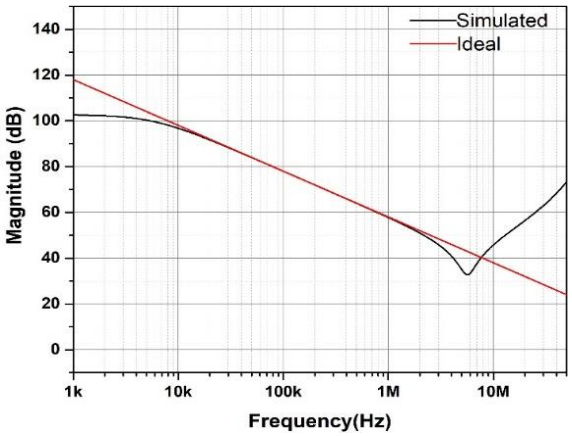


Fig. 11. Ideal and simulated magnitude response of GCM-1.

The GCM-3 is also verified by designing it for a multiplication factor of K = 51 by selecting $R_2 = 50\,k\Omega$, $R_1 = 1\,k\Omega$, and $C_1 = 50\,pF$. It can be seen from the magnitude plot in Fig. 12(a) that there is a small-scale error between the ideal and simulated values. The error can be minimised by properly selecting the W/L ratios of the transistors to minimise the voltage and current transfer errors and parasitic effects.

To validate the applicability of the proposed GCMs in practical applications, the GCM-1 and GCM-3 are employed in the design of a second-order low-pass filter (LPF). The circuit of second-order RC-LPF is presented in Fig. 13.

In the low-pass filter, the capacitor C_1 is implemented using the proposed capacitance multipliers GCM-1 and GCM-3 and C_2 is taken as normal passive capacitor. The designed capacitance multipliers are intended to be used as integrated circuits where in both the capacitors in Fig. 13 can be implemented using capacitance multipliers. The expression for the cut-off frequency of the filter is presented in (22)

$$f_o = \frac{1}{2\pi} \times \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}. \tag{22}$$

The LPF is designed for two different frequencies by setting the component values as $R_1 = 5\,k\Omega$, $R_2 = 5\,k\Omega$,

$C_1 = 40\ pF$, and $C_2 = 10\ pF$. In the second case, the filter frequency is varied by selecting $R_1 = 5\ k\Omega$, $R_2 = 5\ k\Omega$, $C_1 = 250\ pF$, and $C_2 = 10\ pF$. The capacitor C_1 in Fig. 9 is replaced by GCM-1 which has a multiplication factor of K = 4 for the first case and K = 5 for the second case. The ideal and simulated frequency response of the LPF is presented in Fig. 14.

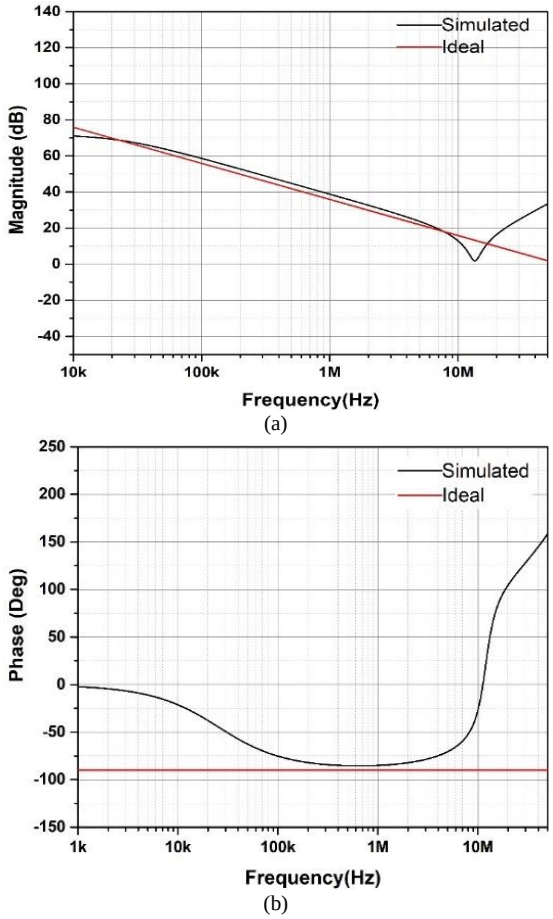


Fig. 12. Ideal and simulated response of GCM-3: (a) Magnitude response; (b) Phase response.

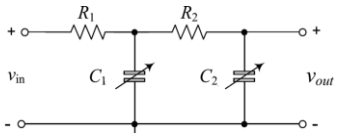


Fig. 13. Circuit of second-order LPF.

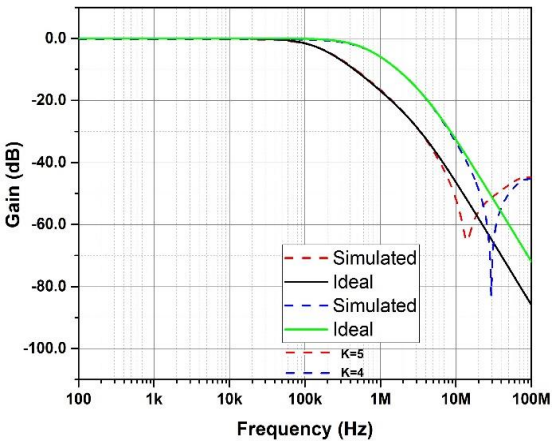


Fig. 14. Ideal and simulated response of the LPF using GCM-1.

To test GCM-3, it is again employed in the design of LPF filter presented in Fig. 13. The filter component values are fixed as $R_1 = 1\ k\Omega$, $R_2 = 1\ k\Omega$, $C_1 = 220\ pF$, and $C_2 = 100\ pF$. The C_1 is realised through GCM-3 by setting the multiplication factor to K = 11. The ideal and simulated frequency response of the LPF is presented in Fig. 15 which confirms the working of the GCM-3.

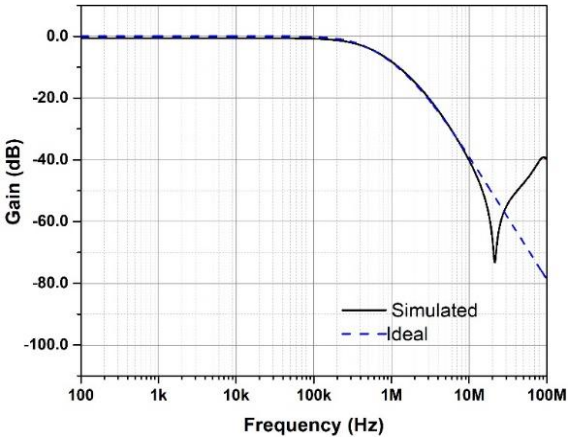


Fig. 15. Ideal and simulated response of the LPF using GCM-3.

To further investigate the performance of the GCM-2, it is designed using the macro-model of the commercially available IC-type AD844 in PSPICE [15]. The supply voltage of ±5 V is used. The implementation requires two AD844 ICs to design GCM-2 as given in Fig. 16.

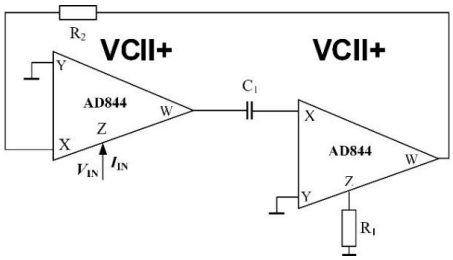


Fig. 16. The AD844 implementation of GCM-2.

To realise a capacitance of 5 nF, the passive component values are set as $R_1 = 25\ k\Omega$, $R_2 = 5\ k\Omega$, and $C_1 = 1\ nF$. The simulated and ideal magnitude and phase responses of GCM-2 are presented in Fig. 17 and Fig. 18.

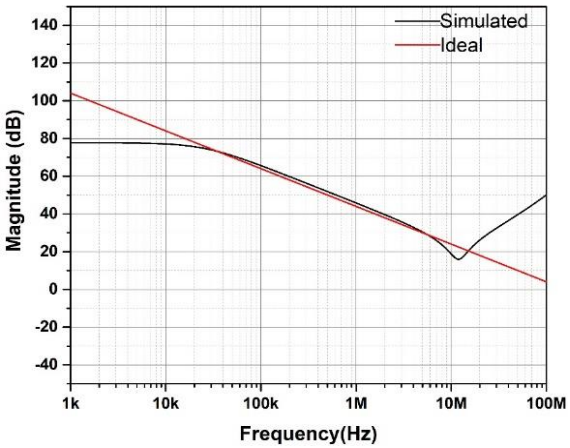


Fig. 17. Ideal and simulated magnitude response of GCM-2.

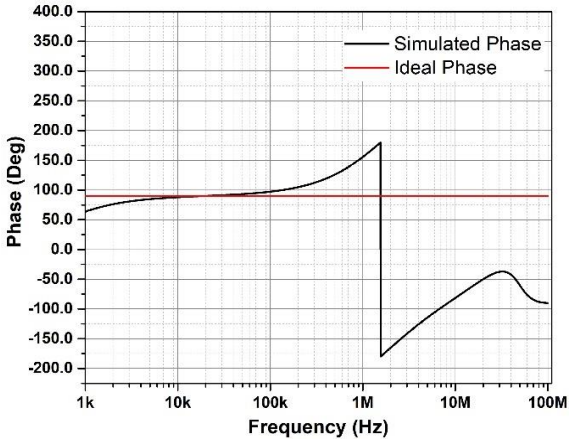


Fig. 18. Ideal and simulated phase response of GCM-2.

VII. CONCLUSIONS

This paper presents four new topologies of grounded capacitance multipliers (positive/negative) using the VCII. The developed GCMs employ two VCIIs, one capacitor, and two resistors. The multiplication factor can be easily set by setting the resistor ratio. The capacitance multiplication factor of 51 is achieved in the case of GCM-3. The presented GCMs work in the frequency range of 10 kHz to 10 MHz. The parasitic and nonideal analysis is carried out to gauge the effect of parasitic impedance and frequency-dependent current and voltage transfer gains on the performance of the proposed GCMs. The proposed GCMs are used in the design of the LPF to validate their performance. GCMs are examined using Cadence Virtuoso using 0.18 µm Silterra Malaysia PDK. The GCMs consume a power of approximately 5 mW. Additionally, the AD844 IC macro-model is used to realise GCM-2 as a proof of concept. The theoretical and simulation results bear a close resemblance.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

REFERENCES

[1] W. Tangsrirat and O. Channumsin, "Tunable floating capacitance multiplier using single fully balanced voltage differencing buffered amplifier", *Journal of Communications Technology and Electronics*, vol. 64, pp. 797–803, 2019. DOI: 10.1134/S1064226919080163.

[2] R. Verma, N. Pandey, and R. Pandey, "Novel CFOA based capacitance multiplier and its application", *AEU - International Journal of Electronics and Communications*, vol. 107, pp. 192–198, 2019. DOI: 10.1016/j.aeue.2019.05.010.

[3] S. Mihalache and F.-S. Dumitru, "Current-mode capacitance multiplier with reduced parasitic elements", in *Proc. of 2016 18th Mediterranean Electrotechnical Conference (MELECON)*, 2016, pp. 1–6. DOI: 10.1109/MELCON.2016.7495302.

[4] I. Padilla-Cantoya, L. Rizo-Dominguez, and J. E. Molinar-Solis, "Capacitance multiplier with large multiplication factor, high accuracy, and low power and silicon area for floating applications", *IEICE Electronics Express*, vol. 15, no. 3, p. 20171191, 2018. DOI: 10.1587/elex.15.20171191.

[5] J. Aguado-Ruiz, J. Hernandez-Alvidrez, A. J. Lopez-Martin, R. G. Carvajal, and J. Ramirez-Angulo, "Programmable capacitance scaling scheme based on operational transconductance amplifiers", *Electronics Letters*, vol. 45, no. 3, 2009. DOI: 10.1049/el:20093596.

[6] P. Moonmuang and W. Tangsrirat, "Electronically tunable resistor less capacitance multiplier employing VDBAs", in *Proc. of the 3rd International Conference on Communication and Information Processing*, 2017, pp. 512–515. DOI: 10.1145/3162957.3163048.

[7] M. Dogan and E. Yuce, "A new CFOA based grounded capacitance multiplier", *AEU - International Journal of Electronics and Communications*, vol. 115, art. 153034, 2020. DOI: 10.1016/j.aeue.2019.153034.

[8] M. T. Abuelma'Atti and N. A. Tasadduq, "Electronically tunable capacitance multiplier and frequency-dependent negative-resistance simulator using the current-controlled current conveyor", *Microelectronics Journal*, vol. 30, no. 9, pp. 869–873, 1999. DOI: 10.1016/S0026-2692(99)00025-7.

[9] I. Myderrizi and A. Zeki, "Electronically tunable DXCCII-based grounded capacitance multiplier", *AEU - International Journal of Electronics and Communications*, vol. 68, no. 9, pp. 899–906, 2014. DOI: 10.1016/j.aeue.2014.04.013.

[10] G. Ferri and S. Pennisi, "A 1.5-V current-mode capacitance multiplier", in *Proc. of the 10th International Conference on Microelectronics*, 1998, pp. 9–12. DOI: 10.1109/ICM.1998.825555.

[11] A. Lahiri and M. Gupta, "Realizations of grounded negative capacitance using CFOAs", *Circuits, Systems, and Signal Processing*, vol. 30, pp. 143–155, 2011. DOI: 10.1007/s00034-010-9215-3.

[12] L. Safari, G. Barile, V. Stornelli, and G. Ferri, "A review on VCII applications in signal conditioning for sensors and bioelectrical signals: New opportunities", *Sensors*, vol. 22, no. 9, p. 3578, 2022. DOI: 10.3390/s22093578.

[13] L. Safari, G. Barile, G. Ferri, and V. Stornelli, "A new low-voltage low-power dual-mode VCII-based SIMO universal filter", *Electronics*, vol. 8, no. 7, p. 765, 2019. DOI: 10.3390/electronics8070765.

[14] V. Stornelli, L. Safari, G. Barile, and G. Ferri, "A new VCII based grounded positive/negative capacitance multiplier", *AEU - International Journal of Electronics and Communications*, vol. 137, art. 153793, 2021. DOI: 10.1016/j.aeue.2021.153793.

[15] L. Safari, E. Yuce, S. Minaei, G. Ferri, and V. Stornelli, "A second-generation voltage conveyor (VCII)–based simulated grounded inductor", *International Journal of Circuit Theory and Applications*, vol. 48, no. 7, pp. 1180–1193, 2020. DOI: 10.1002/cta.2770.

[16] J. Čajka and K. Vrba, "The voltage conveyor may have in fact found its way into circuit theory", *AEU - International Journal of Electronics and Communications*, vol. 58, no. 4, pp. 244–248, 2004. DOI: 10.1078/1434-8411-54100239.

[17] R. Sotner, J. Jerabek, and L. Langhammer, "Tunable fractional-order capacitance multiplier using current gain adjustment", in *Proc. of 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2020, pp. 1–4. DOI: 10.1109/ICECS49266.2020.9294960.

[18] R. Sotner, J. Jerabek, L. Polak, R. Prokop, and W. Jaikla, "A single parameter voltage adjustable immittance topology for integer- and fractional-order design using modular active CMOS devices", *IEEE Access*, vol. 9, pp. 73713–73727, 2021. DOI: 10.1109/ACCESS.2021.3081140.

[19] M. A. Al-Absi and M. T. Abuelma'atti, "A novel tunable grounded positive and negative impedance multiplier", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 6, pp. 924–927, 2019. DOI: 10.1109/TCSII.2018.2874511.

[20] Y. B. Acharya, "Logarithmic current electrometer using commercially available Current conveyor AD844", *International Journal of Electronics*, vol. 93, no. 4, pp. 223–229, 2006. DOI: 10.1080/00207210500519521.