Analysis and Implementation of Switched Capacitor-based Multi-Level Inverter for Electric Vehicles Applications

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***Abstract*—Significant interest has been shown in switched capacitor (SC)-based multi-level inverters (MLIs), which decrease the need for a DC supply and enhance power quality. The common issues with SC-MLIs include an uneven distribution of conducting paths, increased voltage drop across capacitors, the sum of all inverter DC link voltages across the highest voltage rated switches, and a higher total standing voltage (TSV). The purpose of this paper is to create a SC-MLI with less components in order to maintain a constant voltage across the capacitors, to obtain higher voltage gain with fewer parts, fewer conducting routes, lower TSV, and to create a more affordable and effective inverter. The structure of the MLI is created by a cascade interconnection between the number of SC cells. A single input multiple output (SIMO) converter boosts the DC-link voltage over the stable DC voltage of the solar panels using a modified perturb and observe (P&O) method. Additionally, fewer switches in the conduction path and 50 % of the switches operating at normal frequency guarantee a decrease in an overall loss of power in the proposed network. The benefits of the recommended MLI are made clear by comparing them with 17-level MLIs in terms of the number of elements, stress, gain, and cost factor. Detailed experimental results are shown under various transient conditions to show that the 17-level prototype is operationally viable. The total harmonic distortion (THD) is found to be identical and is less than 5 %, which meets IEEE standards.**

***Index Terms*—Switched capacitor; Photovoltaic; Electric vehicles; Multi-level inverter; Maximum power point tracking; Total harmonic distortion.**

I. INTRODUCTION

The challenge of fundamental inverters in achieving the favoured situations, such as a sine output and minimal total harmonic distortion (THD), has become more difficult as the demands for maximum power quality in industrial applications and photovoltaic (PV) systems have increased. Multi-level inverters (MLIs) are given more consideration to meet the required specifications and provide an alternative in terms of delivering high-quality power, reduced switching stress, modular construction, absence of electromagnetic interference (EMI), etc. [1]–[3]. Compared to fundamental inverters such as the flying capacitor (FC) type, the most current multi-level inverter configurations require a simpler structure in the system [4], cascaded H-bridge (CHB) [5], and the neutral point clamped (NPC) [6]. In recent years, different MLI topologies have been described in [7] without connection with the three traditional forms of categorisation. Furthermore, the authors in [8] present the sub-multi-level converter designs. Configurations based on coupled inductors are described in [9]. Although these structures are fundamental, expanding them to maximum levels is a difficult task. In [10], a novel switched capacitor (SC)-based MLI topology with enhanced approaches is introduced.

Numerous topologies in both symmetric [11], [12] and asymmetric are discussed [13], [14]. Asymmetric topologies use DC sources with various voltage magnitudes as opposed to symmetric topologies, which use the same magnitude DC sources. In [15], the development of a switched ladder MLI is described to produce the highest level with smaller components. Reduced switch designs have been created in [16], [17], although the authors can use stronger DC sources to produce the necessary output voltage level. With the different sources (V_{dc2}-V_{dc1}) used in [18], the level-generating unit cannot synthesise the voltage level. A coupled inductor based on a non-isolated multi-input interleaved converter has been described in [19]. In terms of the SC method, the authors in [20] depict a novel MLI topology with a full bridge. The application is limited by the control complexities and increased device count in the SC-MLI topology with a full-bridge back-end described in [21]. The high-frequency output cannot be produced with a low switching loss since the carrier frequency serves as the switching frequency [22]. Due to the smaller size and smaller weight of the system, high-frequency output can be used to implement circuits in electric vehicles (EVs) [23]. According to [24], various technological challenges are encountered and overcome; the effectiveness of EVs depends on the way energy storage devices are interfaced.

The single-DC-source SC-based MLI presented in [25] is made up of two capacitors, nine switches, and two diodes. MLI uses a grid-connected photovoltaic (PV) system

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without a transformer, as shown in [26]. Additionally, there are numerous topologies that support the use of T-type NPC MLI as a crucial component of the overall structure [27]. Ten switches are needed for the cascade TNPC MLI in conjuction with the FC H-bridge architecture presented in [28], and FC is reported to have the fewest devices. To decrease the number of switches, DC sources, and control complexity, various design changes have recently been made [29]. These architectures can be generically categorised into two multi-sources non-step-up MLIs and decreased input SC-based boost type topologies. The switched diode and source MLIs are regarded as the non-boosting type MLIs since they lack the intrinsic boosting feature. The structures are created in [30], [31] to attempt and minimise the number of DC sources.

Capacitors are placed throughout the load and receive an equal distribution of the input voltage; as a result, they cannot increase the output. Series diodes are used in the circuit conduction route presented in [32] for use in renewable energy applications. Therefore, it is impossible for them to operate with extremely inductive loads.

The configuration presented in [33] also has the added benefit of improving the voltage by incorporating a floating capacitor. The voltage spike that appears due to inductive loads alone during the first voltage step can be removed by adding another switch [34]. For DC Microgrids, an intelligent controller with a higher gain non-isolated converter has been described in [35]. SC-MLIs with a single source, including enlarged versions, are also covered by the most recent studies. The charge spike in SCs is addressed in [36] by constructing an MLI with a quasi-resonant front-end architecture and a full back-end bridge. Source voltage is shared between capacitors, and each capacitor is charged evenly. As a result, this architecture does not effectively increase voltage. At the cost of sizable elements, the MLI circuits described in [37], [38] satisfactorily minimise voltage stress. The development of a single-source hybrid NMLI to produce different levels of output while reducing the stress on switches is also investigated in [39]. The proposed converter block diagram is illustrated in Fig. 1. The DC-AC inverter and load are fed with the voltage from a DC-link [40]. Temperature and irradiation both affect the solar PV's output, which is not constant [41]. Consequently, it is crucial to get the greatest power from the PV module, which is considered maximum power point tracking (MPPT) [42], so that the PV panels can generate effectively despite numerous environmental changes. A DC-DC converter significantly contributes to the handling of higher power when MPPT is present in a system due to the way the duty cycle changes [43].

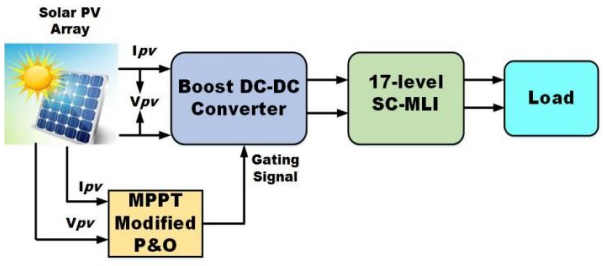


Fig. 1. Generalised block diagram of the proposed converter.

A control strategy is necessary for a PV-fed inverter to generate a constant DC voltage. Numerous approaches, including particle swarm optimisation (PSO), fuzzy genetic algorithms, and artificial intelligence (AI), have recently been used to have an automatic control based on training data to manage desired voltage [44]. It is a remarkable work to choose the MPPT methodology for the appropriate application because each method has advantages and disadvantages of its own.

Conventional techniques cannot extract global MPP (GMPP) under partial shading conditions (PSC) [45]. With the use of several MPPT methodologies, the performance of the converter and the variable step size-radial basis function network (VSS-RBFN) MPPT is evaluated.

The main function of the multi-level inverter is to integrate various levels of DC voltages to obtain the required voltage. Because of this, multi-level inverters may readily supply the high power needed by a huge electric traction drive. Due to the low weight and size of the system, the high-frequency output can be used to implement circuits in electric vehicles (EVs) [46], [47]. To produce an output voltage with a 17-level range, the authors used two DC sources and self-balancing DC-link capacitors. Because capacitors are self-balancing, a more complicated control algorithm is not necessary to maintain voltage balance. The modified P&O-powered MPPT approach is used to harvest the peak energy of the solar array. Additionally, the proposed topology provides much less total standing voltage (TSV), making it a viable solution for high voltage applications. The performances of these MLIs are depicted and compared with numerous MLI techniques based on different metrics, including device count, power losses, efficiency, and THD. The proposed system is examined in MATLAB/Simulink, as opposed to being examined experimentally using a hardware setup.

The design consideration of the proposed techniques is in Section II. The converter technique is proposed in Section III, and MPPT controller is proposed in Section IV. The simulation results and the discussion are presented in Section V. Experimental results are analysed in Section VI. The evaluation of power losses and efficiency is presented in Section VII. The comparison study is presented in Section VIII and Section IX presents the conclusions.

II. DESIGN CONSIDERATION

A. Solar PV

The analysis of a PV system includes a critical component called "solar cell modelling". An analogous circuit with characteristics of power voltage (P-V) and current-voltage (I-V), the impact of solar temperature and irradiance, and PSC are three categories that can be used to mimic solar PV. PV is similar to the phrases "photo" and "voltaic", which denote the conversion of photonic energy into electrical energy and, respectively, photonic and electrical energies [48]. There are p-n semiconductor diodes in [49]. The solar PV system is intended to change its output in response to changes in temperature and weather [50]. The solar cell has internal resistances such as R_S and R_{sh} that are combined in series and parallel with the diode, as shown in

the corresponding circuit in Fig. 2. The PV output voltage and current are denoted by V_{PV} and I_{PV}, respectively. These are obtained from the parallel and series connections of multiple PV modules as indicated in (1)

$$I_{PV} = \left\{ I_{ph} - I_0 \left[exp\left(\frac{q(V_{PV} + R_{SE} I_{PV})}{AKT\, N_{SE}} \right) - 1 \right] - \frac{(V_{PV} + R_{SE} I_{PV})}{N_{SE} R_{SH}} \right\}, \quad (1)$$

where N_{SE} and N_{SH} are the numbers of solar arrays in series and shunt, R_{SE} is the series resistance, and R_{SH} is the shunt resistance. A is the semiconductor ideality factor, K is the Boltzmann constant ($1.3806503X10^{-23}$ J/K), and T is temperature. I_p is the current produced and is based on the temperature and irradiation shown in (2)

$$I_p = \left[I_{SK-STM} + k_i \left(T - T_{STM} \right) \right] - \left(\frac{G}{G_{STM}} \right), \quad (2)$$

where $I_{SK\text{-}STM}$ is a short-circuited current in standard testing cases (STM), K_i is the solar control center (SCC) coefficient, G (W/m^2) is the irradiance on the cell surface, the cell temperature is T_{STM}, and G_{STM} is the irradiance in STM, [51].

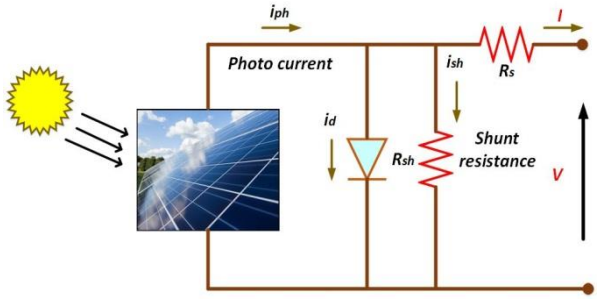


Fig. 2. Equivalent circuit for solar cells.

$$I_O = \left\{ \frac{I_{SK-STM} + K_i (T - T_{STM})}{exp\left[\left(V_{OK-STM} + K_{OV} \left(T - T_{SKC} \right) / AV_{Sth} \right) \right]} \right\}, \quad (3)$$

where $V_{OK\text{-}STM}$ is an open-circuit voltage at STM, K_{OV} represents the open-circuit voltage coefficient, and V_{Sth} is the thermal voltage of the solar cell. Power produced by solar cells is measured by (4)

$$P_{PV} = V_{PV} \times N_{SH} \left(I_{ph} - I_O exp\left(\frac{qV_{PV}}{AKT \quad N_{SE}} \right) - \left(\frac{V_{PV}}{N_{SE}} \right) \right). \quad (4)$$

Figure 3 [52] displays the solar I-V/P-V characteristics. The curve makes it obvious that the PV operating point is unstable; it continuously changes from zero to open-circuit voltage. For the solar PV design at different irradiances, there is a single point in this process that generates peak power. With variations in climate change, solar PV production continues to change [53]. At changing irradiance, the V_{OC} and I_{SC} are measured using (5) and (6):

$$V_{OC} = V_{OC}{}' + a_2 (T - T') - (I_{SC} - I'_{SC}), \quad (5)$$

$$I_{SC} = I_{SC}{}' \left(\frac{G}{G'} \right) + a_1 (T - T'). \quad (6)$$

The temperature coefficients of the PV cell are a_1 and a_2, respectively, according to the above calculations [54].

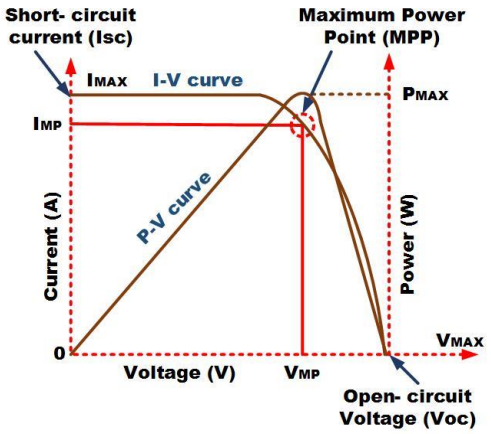


Fig. 3. I-V characteristics of solar cells.

B. DC-DC Step-Up Converter

Figure 1 depicts a DC-DC step-up converter with a single input and several outputs fixed between the solar panels and the recommended inverter. Three independent DC sources are available from this converter in the ratio 4:1:3:9. To minimise inconsistent voltages and step size fluctuations caused by various climatic circumstances, the converter runs off a single solar PV panel [55]. Using the relationship, it is possible to determine the magnitude of the inductance

$$L = \frac{mV_{dc}}{4af_s I_r}, \quad (7)$$

where m is the modulation index, V_{dc} is the DC voltage, f_s is the switching frequency, I_r is the ripple current, and a is the overloading factor, which is usually 1.25. The capacitor value can be determined using the relationship

$$C = \left(\frac{DI_{dc}}{V_{dc} r f_s \times 0.5} \right), \quad (8)$$

where I_{dc} is the DC current, r is the ripple voltage, and D is the duty cycle. The relationship shown below can be used to determine the converter duty cycle

$$D = \left(\frac{V_0}{V_0 + V_{dc}} \right). \quad (9)$$

III. PROPOSED CONVERTER

The design of a 17-level MLI with two SC units coupled in cascade and fewer components is depicted in Fig. 4. Two asymmetric DC sources make up the proposed MLI architecture, which is devoid of inductors. An asymmetrical configuration is created by the two different voltage values. With this MLI technique, the number of issues related to power quality is reduced, including voltage stress, cost

factor, total standing voltage (TSV), and cost per unit with varying weight factors. Compared to other topologies, this topology provides a lower TSV.

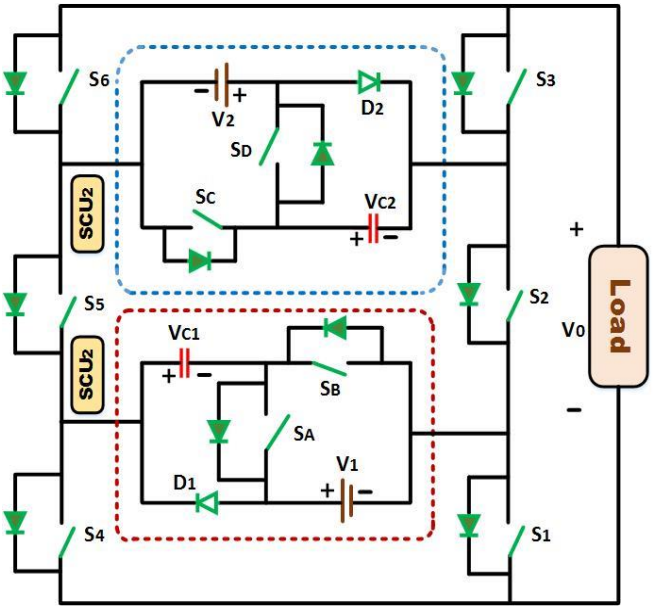


Fig. 4. Proposed converter of 17-level MLI.

Table I shows the state of operation, as well as the direction of the load current through the switches.

TABLE I. CREATION OF VOLTAGE LEVELS BASED ON THE CONDUCTIVITY OF SWITCHES FOR 17-LEVEL MLI.

States	Load current path	Output Voltage (V)		
1	S_A, S_5, S_D, S_3, S_1	$8V_{dc}$	$V_1 + V_{C1} + V_2 + V_{C2}$	+400
2	D_1, S_5, S_D, S_3, S_1	$7V_{dc}$	$V_1 + V_2 + V_{C2}$	+350
3	S_D, S_3, S_6, S_5	$6V_{dc}$	$V_2 + V_{C2}$	+300
4	S_A, S_5, D_2, S_3, S_1	$5V_{dc}$	$V_1 + V_{C1} + V_2$	+250
5	D_1, S_5, D_2, S_3, S_1	$4V_{dc}$	$V_1 + V_2$	+200
6	D_2, S_3, S_4, S_5	$3V_{dc}$	V_2	+150
7	S_A, S_5, S_6, S_1	$2V_{dc}$	$V_1 + V_{C1}$	+100
8	D_1, S_5, S_6, S_1	V_{dc}	V_1	+50
9	S_1, S_2, S_3	0	0	0
10	D_1, S_4, S_3, S_2	$-V_{dc}$	V_1	-50
11	S_A, S_4, S_1, S_2	$-2V_{dc}$	$-(V_1 + V_{C1})$	-100
12	D_2, S_2, S_1, S_2	$-3V_{dc}$	$-V_2$	-150
13	D_2, S_2, D_1, S_4, S_6	$-4V_{dc}$	$-(V_1 + V_2)$	-200
14	D_2, S_2, S_A, S_4, S_6	$-5V_{dc}$	$-(V_1 + V_{C1} + V_2)$	-250
15	S_D, S_2, S_1, S_5	$-6V_{dc}$	$-(V_2 + V_{C2})$	-300
16	S_D, S_2, D_1, S_4, S_6	$-7V_{dc}$	$-(V_1 + V_2 + V_{C2})$	-350
17	S_D, S_2, S_A, S_4, S_6	$-8V_{dc}$	$-(V_1 + V_{C1} + V_2 + V_{C2})$	-400

Figure 5 shows a few operating modes and switching pulses.

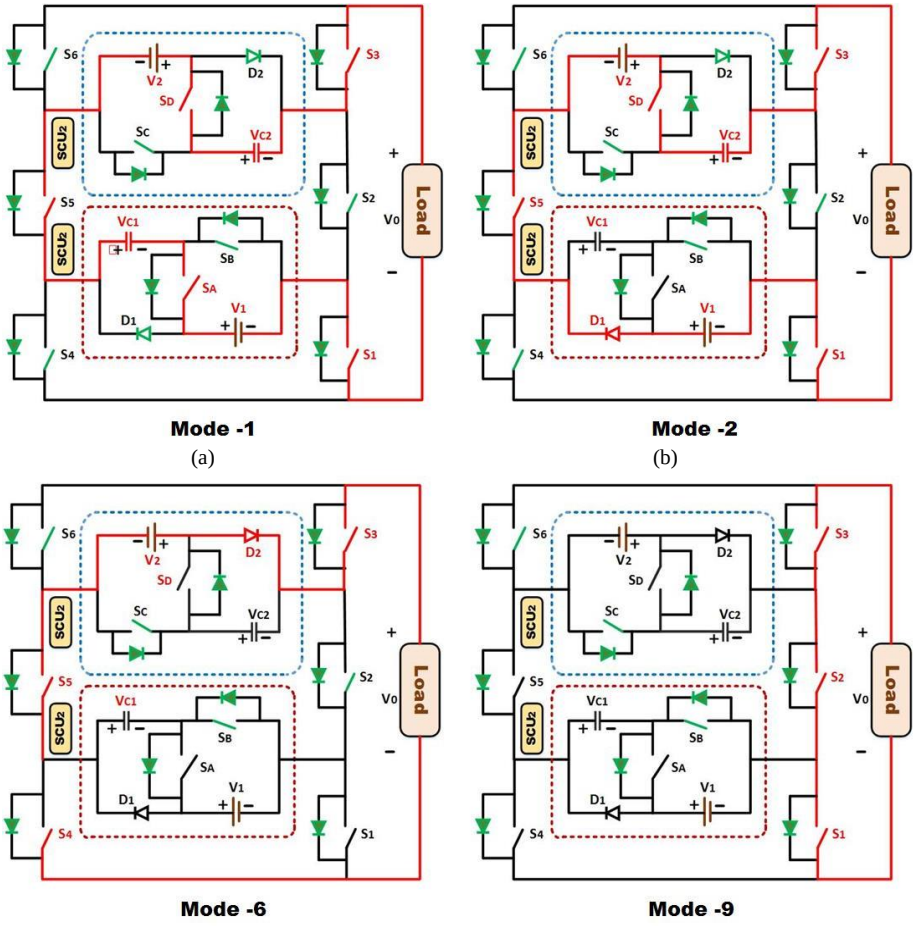


Fig. 5. Proposed converter operation modes: (a) Mode-1, (b) Mode-2, (c) Mode-6, and (d) Mode-9.

– *Mode-1*

To run the circuit, the S_A, S_5, S_D, S_3, S_1, and V_{C2} switches must be turned on. This creates a load current path where the sources V_1, V_{C1}, V_2, and V_{C2} act to produce voltages of 50 V, 150 V, 50 V, and 150 V, accordingly, to reach a maximum value of 400 V. In Table I, the relevant switching pulses, switching states, and current routes are shown.

– *Mode-2*

To operate the configuration switches D_1, S_5, S_D, S_3, and S_1, the sources V_1, V_2, and V_{C2} must produce voltages of 50 V, 50 V, and 150 V, accordingly. This produces a voltage of $7V_{dc}$ = 350 V.

– *Mode-3*

When the circuit is in operation, the switches S_D, S_3, S_6, and S_5 turn on to create a load current route where the sources V_2 and V_{C2} act in the circuit to produce voltages of 50 V and 150 V, accordingly, and receive a voltage of $6V_{dc}$ = 300 V.

– *Mode-4*

During operation, the S_A, S_5, D_2, S_3, and S_1 switches are activated by the V_1, V_{C1}, and V_2 sources acting in the configuration, producing voltages of 50 V, 150 V, and 50 V, accordingly, and obtaining a voltage of $5V_{dc}$ = 250 V.

– *Mode-5*

As the V_1 and V_2 voltage sources operate in the circuit during operation, the switches D_1, S_5, D_2, S_3, and S_1 turn on, producing voltages of 50 V and 150 V, accordingly, and $4V_{dc}$ = 200 V.

– *Mode-6*

During this mode, the switches D_2, S_3, S_4, and S_5, which are activated by the V_2 voltage source, provide a voltage of 50 V and receive a voltage of $3V_{dc}$ = 150 V.

– *Mode-7*

To operate the circuit, the switches S_A, S_5, S_6, and S_1 must be turned on. This produces voltages of 50 volts and 150 volts, accordingly, and results in a voltage of $2V_{dc}$ = 100 volts.

– *Mode-8*

During operation, the switches D_1, S_5, S_6, and S_1 activate when the V_1 voltage source is present in the configuration, producing a voltage of 50 V in each case and a voltage of V_{dc} equivalent to 50 V.

– *Mode-9*

When the circuit is operating, the switches S_1, S_2, and S_3 turn on and provide a voltage of 0 V. Thus, the constructive cycle is established. The switching states are given in Table I and the negative operating modes are used to construct the negative cycle.

IV. MPPT CONTROLLER

An MPPT controller is used to operate solar PV systems so that the PV module can generate a greater amount of power. If the controller is capable of monitoring and supplying greater power from the PV array during all of the disturbances stated above, the efficiency and lifespan of the PV are boosted. Providing the most electricity under different climatic conditions can be accomplished by the source of the load. To get the most electricity from a solar panel, there are two methods. Both mechanical and electrical tracking is involved. Solar panels that use mechanical tracking adjust their direction in accordance with climate variation patterns. The I-V characteristics are compelled to determine the maximum power operation point of the PV array when using electrical tracking [56]. The system's internal component system that supplies the greatest power to the load is the MPPT controller. An appropriate method is used to track the highest power generated while the PV module is operating. The P-V graph of a solar cell illustrates this. The modified perturb and observe algorithm in this study offers a number of benefits.

To achieve MPPT, the modified P&O technique is based on a change in the output voltage of a PV array, followed by an observed change in power that results [57]. The real operating point is located on the left side of the MPP and causes the voltage to rise if the perturbation increases the PV output power; otherwise, it causes the voltage to fall and is on the right side of the MPP. It is maintained in this manner until MPP is achieved [58]. The typical P&O algorithm, represented by the P-V characteristics [58], as illustrated in Fig. 6, may be used to explain the improved version. The following equations are related to this approach and describe it [59]

$$\begin{cases} \dfrac{dP_{PV}}{dV_{PV}} = 0 \quad \textit{at MPP}, \\ \dfrac{dP_{PV}}{dV_{PV}} > 0 \quad \textit{at the left side of MPP}, \\ \dfrac{dP_{PV}}{dV_{PV}} < 0 \quad \textit{at the right side of MPP}. \end{cases} \tag{10}$$

It is impossible to achieve precise MPP $\left(\dfrac{dP_{PV}}{dV_{PV}} = 0\right)$. Therefore, the more investigating format is $\left(\dfrac{dP_{PV}}{dV_{PV}} < \varepsilon\right)$ allowed with a small marginal error which will limit the sensitivity of the tracker.

The sensitivity of the system depends on the magnitude of this permitted error (ε) [60]. In [61], where SF is the scaling factor to change the step size and adopt the performance of MPPT, a VSS is used to increase the performance of PV systems as described in (12) and (13). The power-to-voltage derivative of a PV system determines the variable step size. It is provided as follows

$$VSS = \left|\frac{dP_{PV}}{dV_{PV}}\right| \times SF. \tag{11}$$

Following equation provides the converter duty cycle at instant *k*, *D*(*k*)

$$D(k) = D(k-1) \pm VSS. \tag{12}$$

Equation (12) can be written as

$$D(k) = D(k-1) \pm \left|\frac{dP_{PV}}{dV_{PV}}\right| \times SF. \tag{13}$$

However, the use of PV power to the voltage derivative $\left(\dfrac{dP_{PV}}{dV_{PV}}\right)$ in (13) would have several problems, which can be mentioned below as follows:

1. If the change in PV voltage (dV_{PV}) is low, the

derivative $\left(\frac{dP_{PV}}{dV_{PV}}\right)$ will be large. The power oscillations consequently increase;

2. If the change in PV voltage (dV_{PV}) is large, the derivative $\left(\frac{dP_{PV}}{dV_{PV}}\right)$ will be low. As a result, the power oscillations are reduced, but the response time of the tracking process would take longer to achieve MPP.

Therefore, the proposed MPPT technique can overcome these problems. In this method, a VSS is utilised, which depends solely on changes in PV power (dP_{PV}) instead of the derivative $\left(\frac{dP_{PV}}{dV_{PV}}\right)$. In this case, the VSS can be calculated as follows

$$VSS = \left|dP_{PV}\right| \times SF. \tag{14}$$

The converter duty cycle at instant k, $D(k)$ is obtained using the preceding equation

$$D(k) = D(k-1) \pm \left|dP_{PV}\right| \times SF. \tag{15}$$

The flow chart shown in Fig. 7 describes the steps of the modified P&O technique to evaluate D for switching the converter. In this approach, PV values are absorbed in instant k and compared to the previous values at instant k-1 to calculate dV_{PV}, dV_{PV}, and $\left(\frac{dP_{PV}}{dV_{PV}}\right)$. The accompanying block diagram, depicted in Fig. 6, will describe the necessary processes to estimate the converter duty cycle.

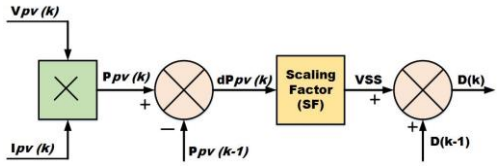


Fig. 6. Block diagram of the modified P&O algorithm.

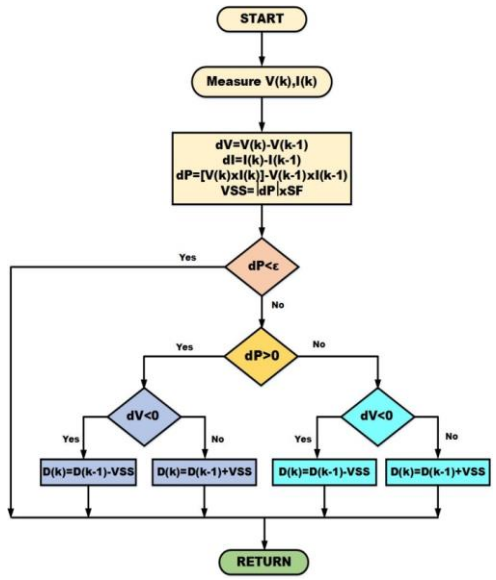


Fig. 7. Flow chart of the modified P&O technique.

The design of a 17-level MLI with two SC units coupled in cascade and fewer components is depicted in Fig. 4. Two asymmetric DC sources make up the proposed MLI.

V. SIMULATION ANALYSIS AND DISCUSSION

The aforementioned topology was developed, simulated, and both linear and non-linear loads were checked on it in MATLAB/Simulink. Static and dynamic analyses of the performance of the circuit are conducted for linear loads. The simulation analysis uses 100 V and 300 V as the values of the DC sources. As switches, insulated gate bipolar transistors (IGBTs) were employed. Nearest level control (NLC) [61] is operated in this design despite the fact that there are numerous other switching strategies for switching and control that are accessible due to the ease of implementation in the literature. The NLC algorithm and switching strategy are depicted in detail in Fig. 8 [62].

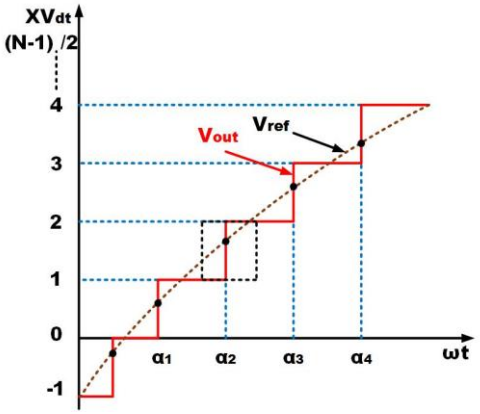


Fig. 8. NLC waveform synthesis.

The analysis under various loading situations and the results that were obtained are presented and thoroughly described in the following part.

A. Fixed Loading Condition

Fixed R and RL loads are taken into account for fixed loading conditions. Heating devices, which simulate changing constant R and RL loads, are a common example of this type of load in domestic applications. Figure 9 shows the output voltage and current waveforms that were produced using a fixed resistive load of R = 100 ohm. Figure 10 shows the output voltage and current waveforms that were produced with a constant L load of 80 mH. The THD of the output voltage is 4.83 %, according to the fast Fourier transform (FFT) analysis. The lower-order harmonics in both situations are under 5 %.

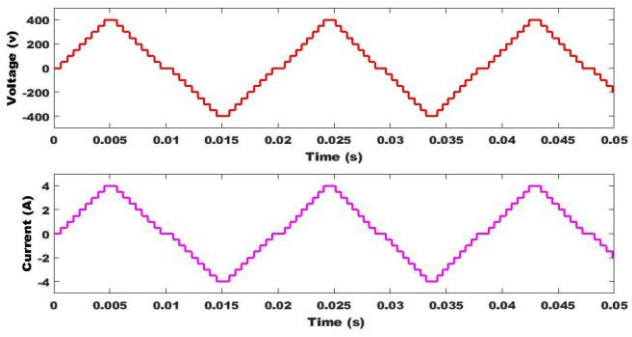


Fig. 9. Simulation output voltage and current for R load.

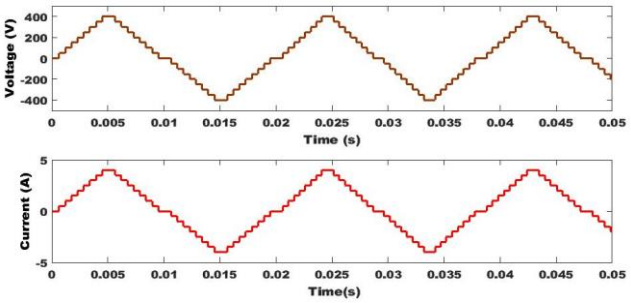


Fig. 10. Simulation output voltage and current for L load.

B. *Varying R and RL Load*

Dynamic load modification is a frequent occurrence in practical applications. Both R-type and RL-type loads can alter under dynamic loads. Heating loads, e.g., might be categorised as R loads along with heating appliances such as furnaces and room heating elements. When the temperature changes, the heating element R must also vary. Therefore, home heaters can function as an R-type load with a variety of characteristics. A fault may result in an abrupt change in load. Additionally, by controlling the motor speed, the varying load of the RL can be simulated. Due to these types of dynamic loading conditions, it is now essential to validate the effectiveness of the advised inverter topology.

Performance is measured by the change of loads from a without-load situation to a steady increase. The obtained voltage and current waveforms for the RL and LR loads are displayed in Fig. 11 and Fig. 12. Both instances show that the voltage stays constant while only the current waveform changes in response to the load. Additionally, seamless is the transition waveform.

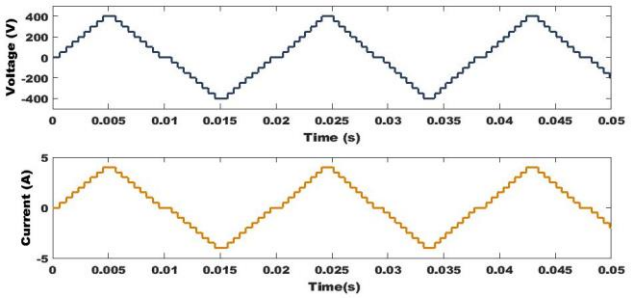


Fig. 11. Simulation output voltage and current for RL load.

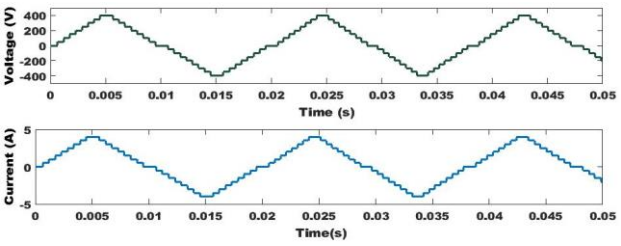


Fig. 12. Simulation output voltage and current for LR load.

C. *Non-Linear Load*

The inverter is frequently needed to supply non-linear loads like rectifiers, computers, variable speed control drives, switched mode power supply (SMPS), etc. In contrast, linear and non-linear loads draw non-sinusoidal currents. Additionally, there is no proportional relation between voltage and current. Therefore, it is essential to verify the performance of the inverter under non-linear conditions. This section evaluates the inverter's performance under various non-linear load scenarios. First, the load is assumed to be a basic switched resistive load, and is implemented using a resistance (R = 100 ohm) coupled in series with an AC controller. The second load taken into consideration is a variable speed drive, which is implemented as an inductive impedance (RL = 100 ohm & 80 mH) interconnected in series with an AC controller. The analysis verifies the effectiveness of the proposed topology and correct operation in both linear and non-linear loading scenarios.

VI. EXPERIMENTAL VERIFICATION

In the laboratory, a testing procedure is created for the recommended 17-level MLI to ensure that it is suitable for real-time adaptability. A 100 V is the initial setting for a programmable DC supply. The load voltage rms value is around 280 V as the voltage output is increased to 4 times the input voltage. Two MUR860 are used as D_1 and D_2, and switches with embedded antiparallel diodes, 12N60A4D, are taken into account for S_1 through S_n. With internal resistances of 36 m, 18 m, and 54 m, accordingly, certain capacitance values (C_1-C_2) are the same as in the simulation. The switching pulses (0–5) V are generated by a DSP controller that interfaces with Simulink. Figure 13 shows the experimental setup of the proposed converter.

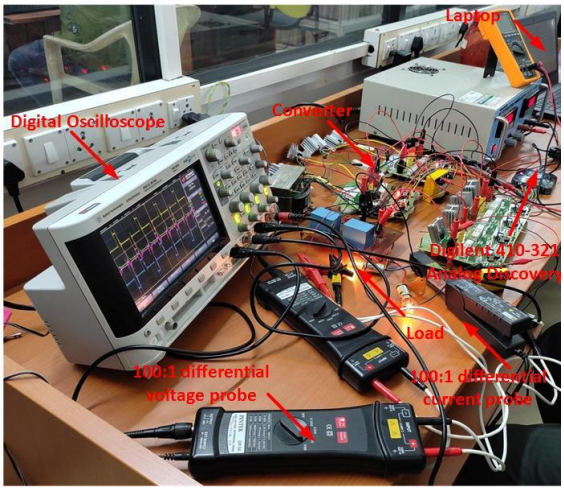


Fig. 13. Experimental setup of the proposed converter.

These pulses are then amplified (to around 20 V) by an isolated driver circuit created utilising TLP250, which drives the switches. The driver circuit also offers sufficient isolation between the control and power circuits. Current-voltage waveforms are collected using a Scope Coder (DL850E), and performance characteristics are acquired using a WT1800 power analyser. Figure 14 shows the experimental output voltage and current.

The MLI is put through an R-load test and is shown in Fig. 15. The voltage and currents that were achieved were 400 V and 4 A, accordingly. The results of the experiment

for the L load are shown in Fig. 16.

Where the appropriate current and voltage are 400 V and 6.8 A, accordingly, Fig. 17 displays the outcome for RL load. Figure 18 shows the experimental results for the LR load.

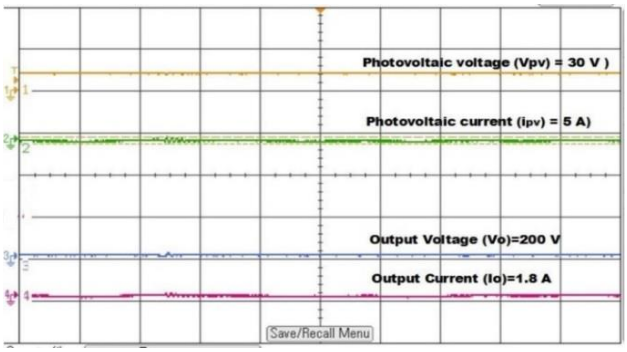


Fig. 14. The PV and step-up converter voltage and current.

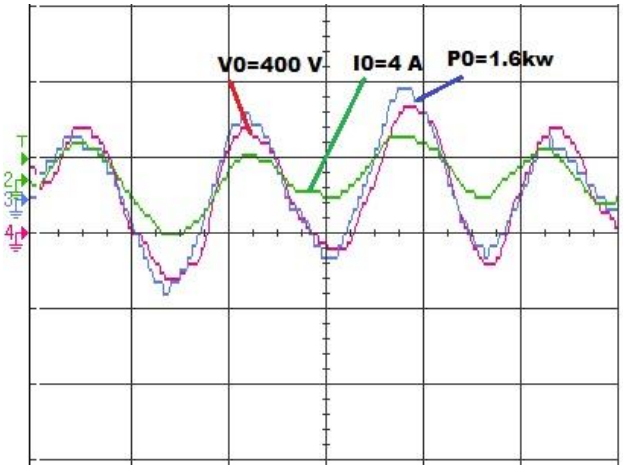


Fig. 15. Experimental output voltage, current, and power for R load.

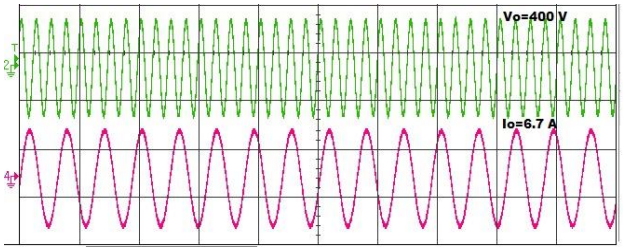


Fig. 16. Experimental output voltage and current for L load.

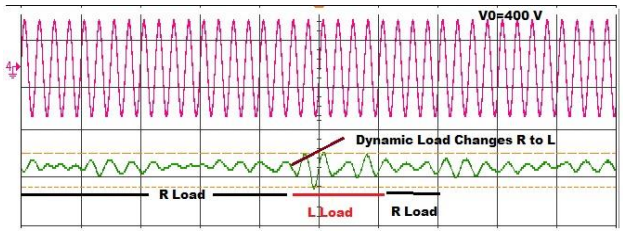


Fig. 17. Experimental output voltage and current for RL load.

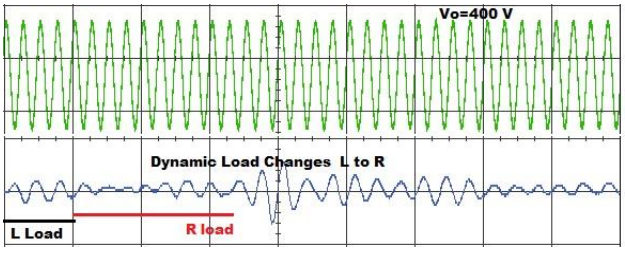


Fig. 18. Experimental output voltage and current for LR load.

The experimental THD shown in Fig. 19 is 4.9 %.

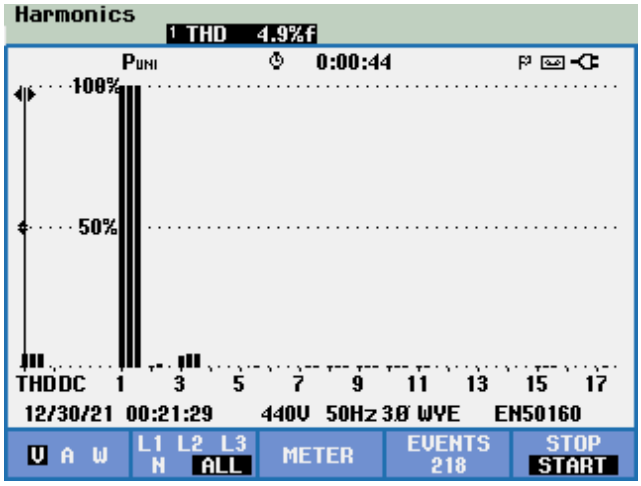


Fig. 19. Experimental THD.

VII. POWER LOSS AND EFFICIENCY EVALUATION

Switching and conduction losses related to switches are separated from overall losses. It is possible to use the equation to calculate the conduction losses of the switch (16)

$$P_{cls} = \left[V_S + R_S i^{\beta}(t)\right] i(t), \tag{16}$$

where V_S is the voltage drop from the switch, and R_S is the equivalent resistance of switch. Conduction power (P_{cl}) losses can be estimated using a modified equation at the "t" instant of time given in (17)

$$\Delta VC = \frac{1}{2\pi f_S C}\int_{\theta}^{\pi-\theta} I_0 \sin(2\pi f_S t - \varphi) d\omega t, \tag{17}$$

where θ represents the angle of discharge of the capacitor, and the discharge stopping point of the capacitor is indicated by the angle $\pi\theta$. The conduction losses are calculated from (18)

$$P_{Cl} = \frac{1}{2\pi}\int_0^{2\pi}\left[N_{IGBT}(t) P_{Cl,IGBT}(t) dt\right]. \tag{18}$$

Equation (19) allows for the calculation of switching losses:

$$TSV = 2(V_{S1} + V_{S3} + \ldots\ldots\ldots\ldots V_{S(2n+1)}), \tag{19}$$

$$P_{Sl} = f\sum_{j=1}^{N_{on,k}} En_{on,kj} + \sum_{j=1}^{N_{off,k}} En_{off,kj}, \tag{20}$$

where E_{on} and E_{off} are the energy utilised by the switches, and the total power losses ($P_{total\ loss}$) are determined as follows

$$P_{total\ loss} = P_{cl} + P_{sl}. \tag{21}$$

Efficiency is determined by the relationship shown below

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}, \tag{22}$$

where P_{out} and P_{in} are the output and input power. Estimating the output power

$$P_{out} = V_{rms} * I_{rms}. \quad (23)$$

VIII. COMPARISON STUDIES

On the basis of the various factors stated below, a comparison of the created 17-level MLIs may be made. It is noted that the parameters of the 17-level MLI technique are more affordable than of the other recent topologies. The proposed MLI is compared to various techniques in Table II, taking into account important factors such as the quantity of the switch, DC sources, gate driver circuits, capacitors, TSV, and the number of elements per level. These comparisons are shown graphically in Fig. 20. Compared to the other topologies, Fig. 20(e) shows a lower full-standing voltage. Figure 20(f) compares the cost functions for several topologies and identifies the most cost-effective one. The MLI presented in [63] uses more DC sources at the expense of fewer switches and drivers. Discrete diodes are not necessary for single-DC SC MLIs [38], [37], but there are many switches involved. On the contrary, the proposed 17-level structure employs only two diodes. Although the use of capacitors facilitates voltage increase, the inrush current increases as the capacitor count increases. The recommended design minimises the current inrush and improves the reliability of the system by using a minimal capacitor. The power loss increases as there are more switches in the conducting circuit.

Additionally, assessed for MLI topologies are maximum standing voltage (MSV) and TSV. TSV is calculated taking into account the voltage stress on each switch. The traditional full bridge is eliminated while generating the AC output, greatly minimising the TSV. Minimum TSV has been proposed for MLI in [33] and [29]. But the latter is a multiple-DC technique without the potential to boost, while the former needs approximately twice as many switches as the proposed MLI. With the least number of switches possible, the proposed MLI has a quadruple boosting gain. Additionally, the cost factor (C_f), which is described as

$$C_f = \frac{(N_{SW} + N_{dr} + N_{dd} + N_{cap} + N_{ms} + \delta.TSV_{pu})N_{dc}}{N_l}. \quad (24)$$

The various values of the weighting coefficient are taken into account when evaluating C_f. Under both parameters (δ = 0.5 and 1.5), the suggested MLI has the lowest C_f of the other MLIs. As a result, the proposed MLI is possesses high-quality output with the fewest switches. When the capacitors are connected in series with the load and parallel with the source at various times, all of the capacitors are able to self-balance to the desired voltage levels. Due to the topology's primarily diode, switch, and capacitor charging circuit, load characteristics have no impact on the capacitors' charging interval. Because of this, the capacitor charging and discharge intervals for each cycle are equal. As a result, regardless of the loading condition, all capacitors retain their self-voltage balance. Calculating the ideal value of capacitors takes into account factors such nominal frequency, lowest amount of voltage ripple, longest discharge period (LDP), maximum fundamental load current, and all other relevant factors. The maximum discharge rate for this time period is indicated

$$\Delta Q_{C1} = \frac{1}{2\pi f}\int_{t_3}^{T_2-t_3} i_L(t)dt, \quad (25)$$

where f is the output voltage frequency and i_L is the load current.

Hence, the maximum discharge amount during this interval can be expressed as, the largest discharge period for C_2 is [t_5, T/2 - t_5]. Hence, the maximum discharging amount during this interval can be expressed as

$$\Delta Q_{C2} = \frac{1}{2\pi f}\int_{t_5}^{\frac{T}{2}-t_5} i_L(t)dt. \quad (26)$$

From (25) and (26), the values of C_1 and C_2 can be determined:

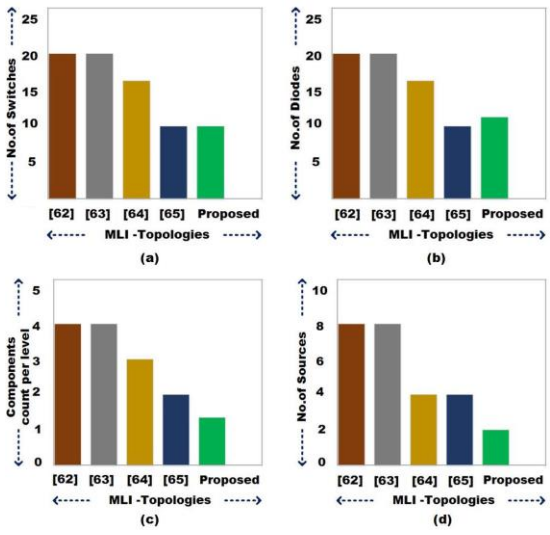
$$C_1 = \frac{\Delta Q_{C1}}{\Delta V_{C1}} = \frac{1}{2\pi f \times \Delta V_{C1}}\int_{t_3}^{\frac{T}{2}-t_3} i_L(t)dt, \quad (27)$$

$$C_2 = \frac{\Delta Q_{C2}}{\Delta V_{C2}} = \frac{1}{2\pi f \times \Delta V_{C2}}\int_{t_5}^{\frac{T}{2}-t_5} i_L(t)dt. \quad (28)$$

Thus, taking the maximum allowable ripple voltage (ΔV_C) equal to 10 % of the corresponding capacitor voltage, the solution of (27) and (28) gives the optimum value of all the capacitors.

TABLE II. THE PROPOSED 17-LEVEL MLI IS COMPARED WITH DIFFERENT MULTI-LEVEL INVERTERS.

Components required	[62]	[63]	[64]	[65]	Proposed
Number of switches	20	20	16	10	10
Number of diodes	20	20	16	10	12
Number of capacitors	0	0	4	0	2
DC sources	8	8	4	4	2
Components per level	4	4	3.17	2	1.35
Total standing voltage	36	36	11	36	16
THD	4.12	3.7	-	7.1	4.9
α = 0.5	4.97	5.05	3.5	4.94	1.98
α = 1.5	2.94	7.17	4.14	9.18	2.89



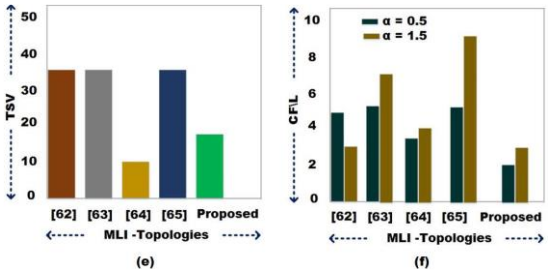


Fig. 20. Comparison of various 17-level MLI: (a) number of switches, (b) number of diodes, (c) number of DC sources, (d) number of elements per level, (e) TSV, and (f) number of cost function level.

IX. CONCLUSIONS

The recommended MLI can generate a 17-level output and can be utilised in PV energy with fewer semiconductor components, which reduces the cost and size of the inverter while increasing system efficiency and reliability. Using a modified P&O algorithm-based MPPT approach, a steady output is always obtained. The proposed MLI is implemented using several SC connection configurations. With just two basic units, a 17-level MLI setup can be created by cascading them. Based on the number of devices, TSV, THD, and cost functions per level, all MLIs are created and contrasted with different topologies. The comparison study reveals that the recommended MLI is more effective and has lower power losses. The recommended MLI is tested using a variety of dynamic load changes. The electric vehicle and also renewable energy applications benefit from this topology the most.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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