A New Design for a BiCMOS Controlled Current Conveyor

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***Abstract*—A new second generation BiCMOS Controlled Current Conveyor (CCCII) is introduced in this paper. The main advantages of the proposed circuit are high bandwidth and tunable resistance with a wide range. Compared with the corresponding existing CCCII, the proposed CCCII offers the advantages of low power dissipation and simple circuit structure. Also, due to the absence of PNP transistors in the designed circuit, its performance is reasonable in terms of the maximum frequency of operation.**

***Index Terms*—BiCMOS integrated circuits, current mode circuits, current conveyor, intrinsic resistance.**

I. INTRODUCTION

There are two basic technologies, known as bipolar and CMOS technology, for integrated circuit implementations. Bipolar technology maintains an advantage over CMOS in noise performance and higher transconductance. Also, it has better high frequency performance than its CMOS counterparts. On the other hand, CMOS transistors have low power consumption, high input resistance, and require a small silicon area compared with bipolar transistors. By combining these circuit technologies, the main advantages of each technology can be used. This technology is called BiCMOS and is useful in high frequency and low power analogue applications [1].

Second generation current conveyors (CCIIs) were introduced in 1970 [2]. Since their introduction, they have been used in numerous applications in the field of analogue electronics such as in filters, amplifiers, inductance simulators and, in particular, signal processing circuits. In 1995, the current controlled conveyor (CCCII) was introduced in bipolar technology [3] and later in BiCMOS [4] by Fabre. Parasitic resistance is essentially a disadvantage in electronic circuits. However, this intrinsic resistance, seen at port X, is used to advantage in current controlled conveyor circuits, because it can be easily controlled by biasing current. This advantage allows the design of numerous tunable functions [3], [5].

Second generation current conveyors designed using only CMOS technology has been proposed in the literature [6]–[8]. However, they are only able to operate at low frequencies. Therefore, the capability of applications is limited and these circuits exhibit severe frequency limitations.

A CCCII based on the mixed translinear loop using bipolar technology has also been described in the literature [3]. The CCCII is composed of NPN and PNP transistors. The use of PNP transistors in BiCMOS circuits offers reduced performance compared with NPN transistors. When PNP transistors are not used in CCCII, the frequency performance of the controlled current conveyor is better. This is because NPN transistors have higher electron mobility than PNP transistors. In the literature, current conveyors are designed by using PNP transistors for handling ac signals [9], [10]. However, the operating frequency of these circuits is highly low. These studies suffer from narrow bandwidth and circuit complexity. In order to avoid these problems, BiCMOS current conveyors using only two NPN transistors are proposed in this paper. In the designed circuits, the required bias current is achieved by employing only NMOS transistors and NPN transistors used for realizing the resistance R_X. Also, the proposed circuit is eminently suitable for IC realization. In order to keep circuit complexity low and the design simple, fewer components are used in the circuit.

In this work BiCMOS controlled current conveyors, whose negative and positive parasitic resistance at port X can be controlled by biasing current, will be reviewed by this article. First, the theoretical analysis of the proposed circuits is presented. Then, the circuit analyses of the conveyors are presented. The performances of the proposed circuits are illustrated by Spice simulations. They show good agreement for all characteristics. To demonstrate the proposed circuit's easy applicability, it was used in a grounded inductance simulator and a bandpass filter.

II. PROPOSED BICMOS CCCII REALIZATION

In this section, the proposed controlled current conveyor with both positive resistance (R_x^+) and negative resistance (R_x^-) will be investigated.

A. CCCII with positive resistance

The proposed CCCII with R_x^+ realization is shown in Fig. 1, where transistors Q_1 and Q_2 act as a transconductance amplifier to convert input voltage to output current.

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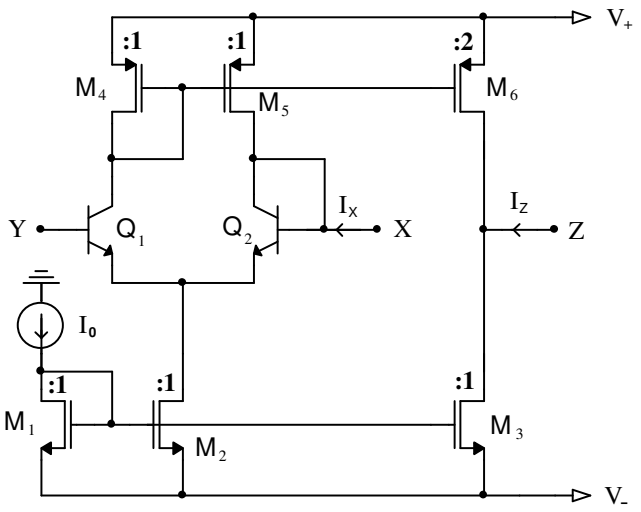

Fig. 1. Proposed CCCII with R_x^+.

M_1 and M_2 act as a simple current mirror where I_0 is the input bias current. The choice of MOS transistors to constitute the current mirrors is not arbitrary, since they allow a very weak consumption of power and dense integration, when V_y and V_x are applied from port Y and port X, respectively. According to the translinear principle, the difference between input voltages V_y and V_x of the transconductance amplifier is given by

$$V_y - V_x = V_{BE1} - V_{BE2} = V_T\left(\ln\frac{I_{C1}}{I_S} - \ln\frac{I_{C2}}{I_S}\right), \tag{1}$$

As shown in Fig. 1, I_{C1} and I_{C2} are the collector currents of the Q_1 and Q_2 transistors, respectively. In addition, V_T is the thermal voltage, V_{BE} is the junction voltage of the transistors and I_S is the reverse saturation current of the transistors.

In this case, the collector currents of the transistors can be written by

$$I_0 \cong I_{C1} + I_{C2}, \tag{2}$$

where:

$$I_{C1} = \frac{I_0}{1 + e^{\frac{-(V_y - V_x)}{V_T}}}, \tag{3}$$

$$I_{C2} = \frac{I_0}{1 + e^{\frac{V_y - V_x}{V_T}}}. \tag{4}$$

The relationship of I_x and input voltages of the transconductance amplifier is given by

$$I_x = I_{C2} - I_{C1} = I_0 \tanh\left(\frac{V_x - V_y}{2V_T}\right). \tag{5}$$

If $V_x - V_y << 2V_T$ is assumed from (5), then the function $\tanh[(V_x - V_y)/2V_T]$ is approximately equal to $(V_x - V_y)/2V_T$. The expression of this input current is

$$I_x = I_0 \frac{V_x - V_y}{2V_T}. \tag{6}$$

When port Y of the CCCII is grounded and port X constitutes the input of the circuit (Fig. 1), the resistance R_x of port X is the intrinsic resistance for the CCCII. R_x is written as follows

$$R_x = \frac{2V_T}{I_0}. \tag{7}$$

Derivations of the small-signal analysis can be expressed as

$$i_x = v_x \cdot g_{m2} - v_y \cdot \left(\frac{g_{m4} \cdot g_{m1}}{g_{m5}}\right). \tag{8}$$

Since all transistors are operating at the same bias current, $g_{m5} = g_{m4}$ and $g_{m1} = g_{m2} = g_m$ where

$$i_x = g_m\left(v_x - v_y\right), \tag{9}$$

thus, from (4) and (7) it can be seen that

$$R_x = \frac{1}{g_m}. \tag{10}$$

B. CCCII with negative resistance

The proposed CCCII with R_x^- realization is shown in Fig. 2.

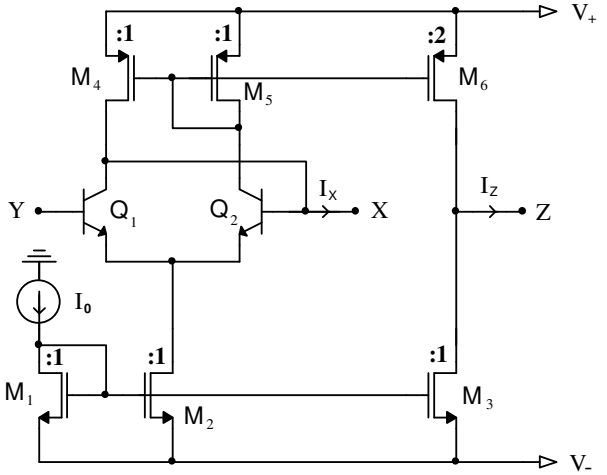

Fig. 2. Proposed CCCII with R_x^-.

As shown in Fig. 2, the CCCII with negative intrinsic resistance structure is the same as the other proposed CCCII with R_x^+ structure in terms of components, but it uses different connections between the components in the circuit.

The same process formulated for CCCII with R_x^+ is repeated for CCCII with R_x^-. An analysis of the circuit which operates as CCCII with R_x^-, assuming all other transistors are matched, shows that the current I_x is given by

$$I_x = I_0 \frac{V_y - V_x}{2V_T}. \tag{11}$$

When port *Y* of the CCCII with R_x^- is grounded and port *X* constitutes the input of the circuit (Fig. 2), the intrinsic resistance R_x is written as follows

$$R_x = -\frac{2V_T}{I_0}, \tag{12}$$

As shown in (7) and (12), both positive and negative intrinsic resistance can be easily controlled by biasing current I_0.

CCCIIs with negative resistance realizations were introduced in [11], [12]. It is obvious that these circuits have complex circuit structures compared with the proposed circuit here.

C. Area mismatch of the CCCII

The effect of the differential pair mismatch of the CCCII in Fig. 1 can be defined as an inequality in the base-emitter areas of the transistors Q_1 and Q_2. Such a mismatch between transistors can be given as:

$$\begin{cases} I_{S1} = I_S + \dfrac{\Delta I_S}{2}, \\ I_{S2} = I_S - \dfrac{\Delta I_S}{2}. \end{cases} \tag{13}$$

A proportional mismatch in the collector transport saturation current I_S is defined in (13). Thus, the biasing current I_0 obtained by using the MOS current mirror will be split between the Q_1 and Q_2 transistors in proportion to their I_S values. If voltage V_y and V_x are grounded, the collector currents of the transistors will be found as follows:

$$\begin{cases} I_{C1} = \dfrac{I_0}{2}\left(1 + \dfrac{\Delta I_S}{2I_S}\right), \\ I_{C2} = \dfrac{I_0}{2}\left(1 - \dfrac{\Delta I_S}{2I_S}\right). \end{cases} \tag{14}$$

The input current I_x can be given by the following equation if the condition is $V_x - V_y > 0$

$$I_x = g_m(\mathrm{V_x} - \mathrm{V_y}) - \left(\frac{I_0 \Delta I_S}{2I_S}\right), \tag{15}$$

where I_S is the collector transport saturation current of the Q_1 and Q_2 transistors. From the above equations, R_x is written as follows

$$R_x = \frac{(\mathrm{V_x} - \mathrm{V_y})}{I_x} = \frac{2V_T}{I_0} + \frac{V_T \Delta I_S}{I_S I_x}. \tag{16}$$

III. SIMULATION RESULTS

To validate the theoretical analysis, the circuits in Fig. 1 and Fig. 2 were simulated using models for the transistors of the type AMS S35 BiCMOS 0.35 μm process. They were supplied under ±1.5 V.

The parasitic resistance of the proposed CCCII with R_x^+ and CCCII with R_x^- for different biasing currents are shown in Fig. 3. The biasing current I_0 changes between 1 μA and 50 μA for both circuits.

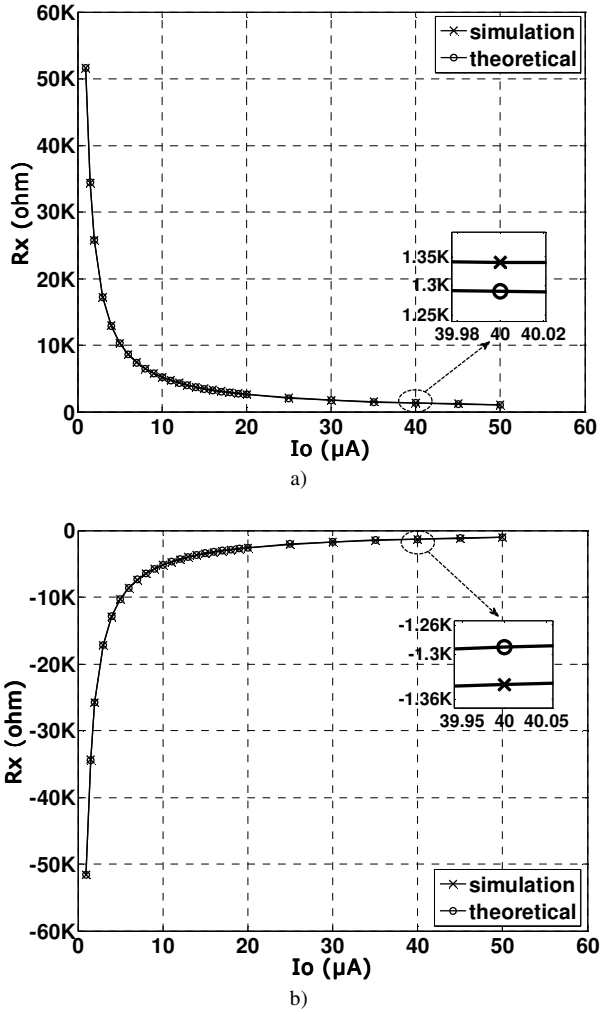

Fig. 3. The parasitic resistance of the CCCII with R_x^+ for different biasing currents (a); the parasitic resistance of the CCCII with R_x^- for different biasing currents (b).

This figure depicts the theoretical and simulation results. The theoretical calculation was performed using (7). As shown in Fig. 3, the simulation results approximately verified the theoretical consideration. The small difference between the curves is caused by a mismatch between transistors. Parasitic resistance can be approximately tuned from ±1.032 KΩ to ±51.6 KΩ for different biasing currents. In the literature, electronically tunable intrinsic resistance was used to advantage in CCCII [8], [12]. If the proposed circuit is compared with references [8], [12], it can be seen that this is better and preferable than these circuits. Although Zouaoui-Abouda's conveyor has ultra-high frequency response, the controllable range of the intrinsic resistance in the conveyor is limited between 0.58 KΩ and 2.8 KΩ. It is shown from Psychalinos's paper [12] that when the biasing current varies from 1 μA to 50 μA, the intrinsic resistance of the conveyor decreases approximately from 25.8 KΩ to 0.51 KΩ. Also, Psychalinos's circuits have more complex circuit structure containing many transistors than the proposed circuits in Fig. 1 and Fig. 2.

The simulated frequency response of the current gain from port X to port Z for the CCCII has been plotted in Fig. 4.

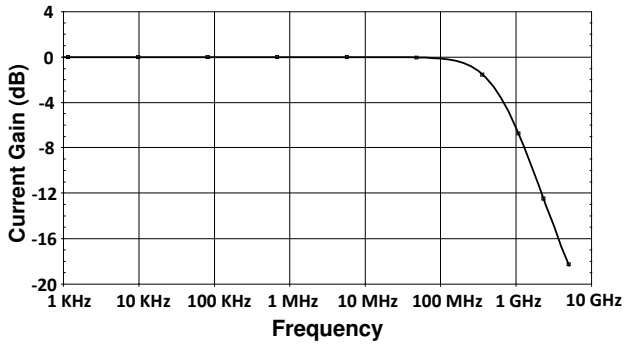

Fig. 4. The behavior in frequency of the CCCII.

The −3dB bandwidth of the CCCII is located at 554.3 MHz for I_0=10 μA.

Fig. 5 depicts the changing simulated percent total harmonic distortion (THD) plot versus peak to peak input current for the CCCII. THD % as a function of peak to peak magnitude of the input current is calculated for I_0 = 10 μA and frequency = 1 MHz.

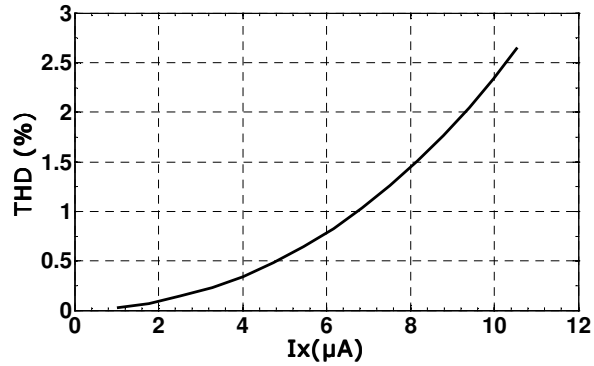

Fig. 5. Total harmonic distortion for a 1 MHz input signal at port X.

Fig. 5 shows that the THD % in the voltage at port X, when the peak to peak magnitude of the input current was changed from 1 μA to 10 μA, is found to vary from 0.026 % to 2.35 %. It is clear that the THD is within reasonable values. The input signal amplitude for achieving THD equal to 1% is 6.8 μA. The signal quality remains excellent, as shown by the low values of the THD (simulated with a signal frequency of 1 MHz).

The power dissipation of the proposed circuit is found as 75.1 μW for the biasing current 10 μA. It has a good overall performance. BiCMOS is seen to have a clear advantage in power dissipation over bipolar technology.

IV. APPLICATIONS

A. *Electronically tunable grounded inductance simulator*

As an application, the proposed BiCMOS CCCIIs are used to build an electronically tunable grounded inductance simulator as shown in Fig. 6.

The circuit consists of a CCCII with R_x^+, CCCII with R_x^- and a grounded capacitor. Based on the property of the proposed CCCIIs corresponding to (7) and (12), analysis of Fig. 6 shows that currents belonging to circuit are equal to

$$I_1 = -\frac{V_{in}}{R_{x1}}, \tag{17}$$

$$I_2 = \frac{V_{in}}{sCR_{x1}(-R_{x2})}, \tag{18}$$

where R_{x1} and R_{x2} are the intrinsic resistances of the CCCII with R_x^+, and CCCII with R_x^-, respectively. As shown in Fig. 6, the input current of the simulator is relative to current I_2 as follows

$$I_{in} = -I_2. \tag{19}$$

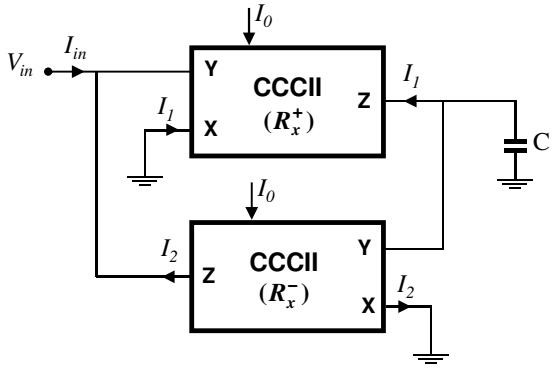

Fig. 6. Electronically tunable grounded inductance simulator.

From (18) and (19), the input impedance of the simulator can be written as

$$Z_{in} = \frac{V_{in}}{I_{in}} = sCR_{x1}R_{x2}. \tag{20}$$

As shown in (20), the equivalent inductance of the application circuit can be obtained as follows

$$L_{eq} = CR_{x1}R_{x2}. \tag{21}$$

The impedance values of the simulator relative to frequency for different I_0 are shown in Fig. 7, where C=50pF.

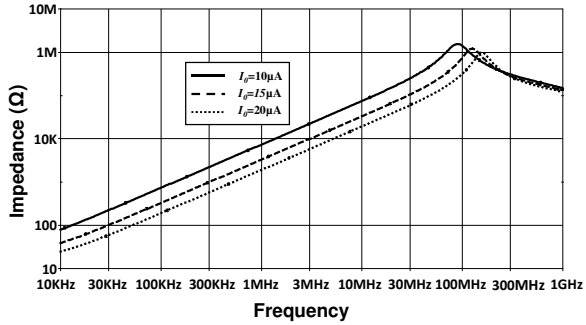

Fig. 7. The impedance values of the simulators for different biasing currents.

Fig. 7 depicts that the impedance of the circuit can be easily controlled by the biasing current of the conveyors and the inductance simulator contains only a grounded capacitor. Simulation results verify the theoretical background.

B. *Bandpass filter*

In order to present the applicability of the proposed circuits, a bandpass filter is used as an application. The tunable second order bandpass filter circuit shown in Fig. 8

consists of two CCCIIs and two capacitors [13].

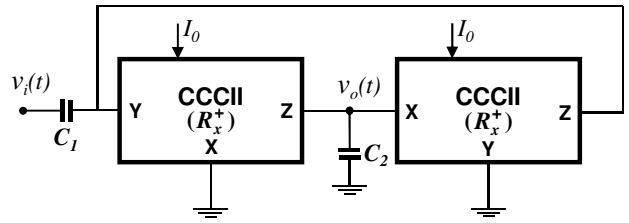

Fig. 8. Bandpass filter based on CCCII.

When the two conveyors are dc biased by identical biasing current, the intrinsic resistances of the two conveyors are in consequence equal to R_x. The transfer function of the bandpass filter with a gain equal to unity is characterized by:

$$\frac{v_0(t)}{v_{in}(t)} = \frac{sC_1R_x}{1 + sC_1R_x + s^2C_1C_2R_x^2}, \tag{22}$$

$$\omega_0 = \frac{1}{R_x\sqrt{C_1C_2}}. \tag{23}$$

Fig. 9 shows the simulated transfer response obtained for the filter with the different values of the biasing currents. These values are 20 µA, 30 µA and 40 µA.

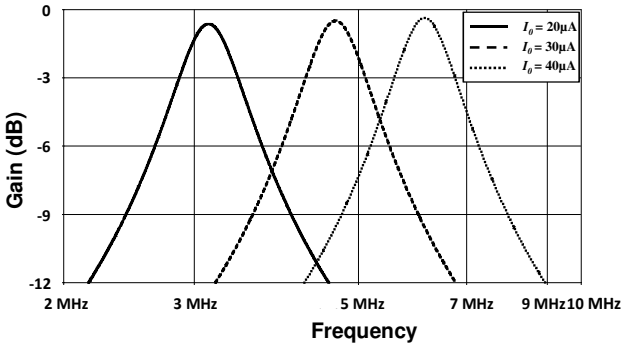

Fig. 9. Frequency response of the bandpass filter.

The values for the passive components in Fig. 8 are: C_1=4 pF and C_2=100 pF. The bandpass filter can be easily controlled by biasing current I_0. Note that these simulated results are well correlated with the theoretical ones, especially for these high operating frequencies. The main advantages of the conveyor based bandpass filter are electronically tunability in a wide range and low power dissipation.

V. CONCLUSIONS

In this paper, new second generation BiCMOS CCCIIs were designed and their application to a grounded inductance simulator and a bandpass filter were tested. The proposed circuits were implemented in standard 0.35 µm BiCMOS technology with no passive component, which is attractive for IC implementations. One of the reasons we used the BiCMOS technology is that it has the advantages of both bipolar and CMOS technologies.

Both CCCII with R_x^+ and CCCII with R_x^- are the same in terms of having components, but different connections are used between the components in the circuit. Therefore the intrinsic resistance of the conveyor can be obtained as either positive or negative by using different connection structures. The proposed circuits were simulated using a Spice simulation program. The circuits' theoretical analysis was carried out, and the performance of the block circuit was confirmed through the Spice simulation results. The intrinsic resistance value of the proposed CCCII can be varied from ± 1.032 KΩ to ± 51.6 KΩ for different biasing current, with excellent correspondence between the theoretical and simulation results. Also, the proposed circuits have high frequency performance and low power dissipation.

Finally, such adjustable behavior in the proposed circuit, which has no passive component, is a good feature in general electronic circuit designs and we believe the circuit is rather convenient for BiCMOS IC realizations.

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