Class-E Power Amplifier with Novel Pre-Distortion Linearization Technique for 4G Mobile Wireless Communications

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***Abstract*—A new method to improve the battery life span of a 4G handset power amplifier (PA) is proposed. This technique is realized by employing a novel passive linearization topology on a class-E PA. Implemented in a 2 µm InGaP/GaAs Hetero-Junction Bipolar Transistor (HBT) technology, the PA delivers 49 % of power added efficiency (PAE) at output power of 28 dBm while complying with the Long Term Evolution (LTE) regulation at Band 1(1920 MHz–1980 MHz) with corresponding supply voltage headroom of 4 V. The performance enhancement is achieved at LTE channel bandwidth of 20 MHz. To the best of the author's knowledge, this is the first class-E PA which meets adjacent channel leakage ratio (ACLR) specifications at 20 MHz LTE bandwidth.**

***Index Terms*—Linearization, LTE, PAE, power amplifier.**

I. INTRODUCTION

Long Term Evolution (LTE) protocol is a prominent solution to fulfill the continuous demand for high data rate transmission. LTE is capable in establishing a downlink peak data rate up to 326.4 Mbps and maximum data rate of 86.4 Mbps for the uplink [1]. Therefore, the demand of high output data rate results in an increased signal complexity nurturing towards the employment of multicarrier modulation standards. Owing to this signal complexity, the transmitter system, especially the power amplifier is regulated to maintain a linear operating region [2]. In fulfilling this criterion, the PA is operated at a back-off output power level from its 1 dB compression point. The operation is subjected to the degradation in the efficiency of the PA.

Several optimization methods have been reported in the effort to achieve a desired PAE for the designated PA. The most prominent is the envelope tracking method, which is reported to deliver a PAE of up to 39 %, thus complying the linearity specification for LTE signal with 10 MHz of channel bandwidth. However, in order to meet the stipulated performance criterion, a hybrid, cost ineffective dual technology has to be employed, which is a merger of CMOS and GaAs HBT [3]. An alternative approach is in realizing a RF CMOS only PA, which proves to deliver 25.8 % of PAE at a corresponding output power of 29.4 dBm [4].

In this work, a class E PA has been designed and realized in an objective to achieve a high PAE, which is measured to be 49 %. A class-E PA is categorized as a non-linear PA due to its operation at the cut-off region of the I-V curve. Hence, in order for the PA to meet the LTE linearity requirement as regulated in the 3GPP specifications [5], a novel passive linearization technique has been proposed and integrated. The linearization technique cancels out the third order intermodulation (IMD3) at high output power, thus confirming to the ACLR specifications.

This paper is organized as follows. Section II reviews the operation principle of the proposed circuit. Section III explains the theory of operation of the linearized class-E PA. In Section IV, the measured results are presented, followed by the conclusion in Section V.

II. PRINCIPLE OF OPERATION

Figure 1 illustrates the topology of the proposed PA, which integrates a Class-E PA, passive pre-distorter linearizer and an output matching network ensuring a maximum linear output power at the designated PAE. The Class-E PA encapsulates a HBT transistor and a shunt capacitor, C_1. The passive pre-distorter is connected at the input of the Class-E PA, prior to the parallel RC network. The parallel RC network protects the PA from thermal runaway phenomenon [6]. The output matching network is tasked upon to transform the 50 ohm output impedance to a desired impedance point, which delivers the maximum output power. The methodology in obtaining this impedance point is explained in section III. The G_m compensation technique [7] is adapted in the development of the biasing circuit. This technique helps to stabilize the base-emitter voltage of the biasing circuit, ensuring insensitivity towards an abrupt change of the supply voltage. The collector and base of transistor Q_{b3} is shorted realizing a diode and further connected to the base of Q_{b2}. Transistor, Q_{b3} acts as temperature compensator alleviating significant changes in the biasing current across temperature variation.

The proposed PA is fabricated using GaAs HBT technology due to its superior electrical characteristics at high frequency operation [8]. Its inherent characteristics of low collector-emitter offset voltage and low resistance

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contributes to an efficient operation at low operating voltages [9]–[11].

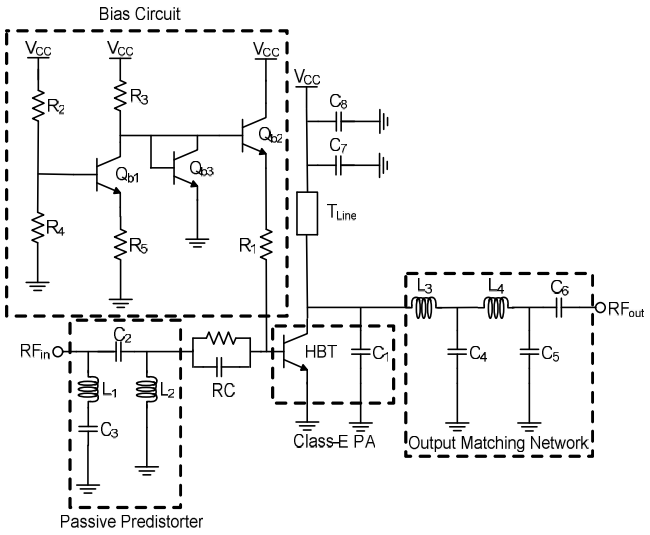

Fig. 1. Schematic of the proposed LTE PA.

III. THEORY OF OPERATION

A. Optimum Load Resistance

An overhead of maximum linear output power is essential in a handset design to compensate the antenna path loss. The overall maximum linear output power is determined by the load resistance of the main stage amplifier. For LTE, the desirable linear output power essential for reliable transmission by the transmitter system is 23dBm [5]. Hence, the power amplifier needs to have at least 27.5dBm of maximum linear output power overhead to compensate the path loss [12]. The optimum load resistance for a single HBT unit cell can be calculated from the following equation

$$R_{opt} = \frac{V_{dc} - V_k}{\mathrm{I}_{\max}}, \tag{1}$$

where V_{dc} is the desired operating voltage, V_k is the I-V curve knee voltage and I_{max} is the maximum current as the device is biased at a class-A operating point. In order to determine the optimum load resistance for the desired maximum linear output power delivered by the PA, scaling techniques are adapted. Scaling can be realized by

$$R_{loadopt} = \frac{R_{opt}}{N}, \tag{2}$$

where N represents the number of HBT cell. I_{max} and V_k is determined from the I-V curve of a single cell HBT transistor, as described in Fig. 2.

From (1) and (2), the optimum load resistance for the PA in this design is computed to be 6.7 Ω. Based on the $R_{loadopt}$ location on the Smith Chart an output matching network, as illustrated in Fig. 1 is designed and integrated to transform 50 ohm load impedance to $R_{loadopt}$. The inherent relationship between $R_{loadopt}$ and the delivered output power is expressed in the following equation [12]

$$P(dBm) = 10\log\left[\left|\frac{(2V_{CC} - V_{sat})^2}{8 \cdot R_{loadopt} \cdot 10^{-3}}\right|\right], \tag{3}$$

where V_{sat} is the saturation voltage.

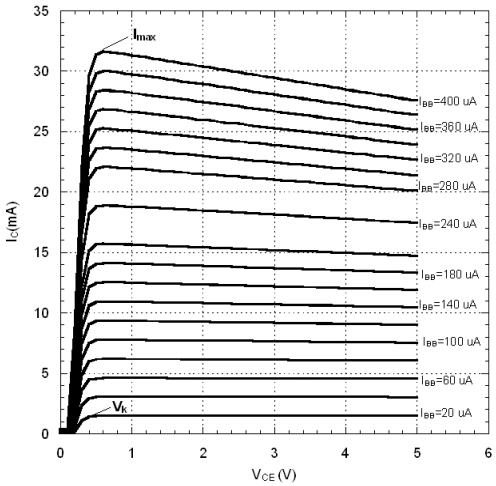

Fig. 2. I-V Curve of a single cell HBT transistor.

B. Principle Operation of Class-E PA

In an ideal class-E PA, the transistor operates as a switch by shaping the current and voltage response not to overlap each other. This results in high efficiency, since the power dissipation has been minimized. The desirable characteristic is achieved by biasing the PA close to the cut-off region on the I-V curve. In reference to Fig. 3, the voltage and current waveform of a class-E PA when the switch is turned ON can be represented as [13]:

$$v_{sw} = 0, \tag{4}$$

$$i_{sw}(\mu t) = i_{out}\left[\sin(\mu t + \sim) - \sin \sim\right], \tag{5}$$

on the other hand, when the switch is OFF, the voltage and current is given by:

$$v_{sw} = \frac{1}{\mu C_1}\int_{\circledR}^{\mu t} i_c(\mu t)\, d\mu t, \tag{6}$$

$$i_{sw} = 0, \tag{7}$$

where α represents the incurred phase shift.

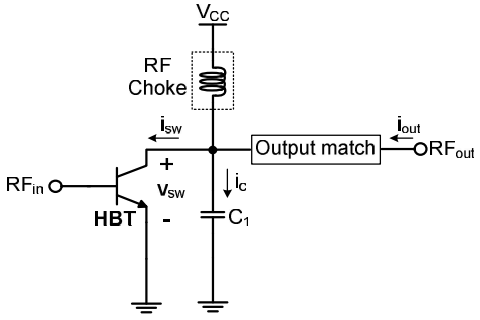

Fig. 3. Current and voltage representation in class-E PA.

The result of (4) to (7) is illustrated in the transient response of Fig. 4, which evidently a class-E operation.

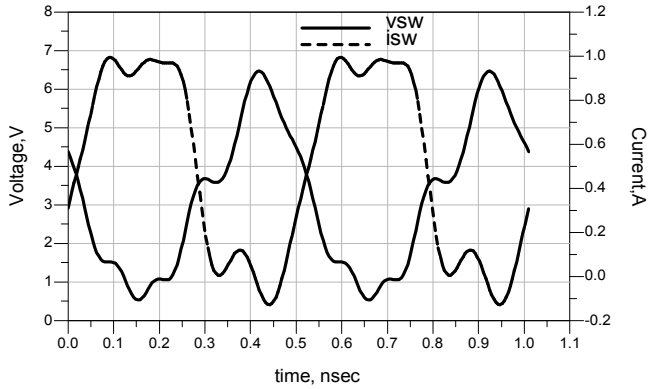

Fig. 4. Simulated Class-E waveform at maximum linear output power of 28 dBm.

C. Passive Pre-distortion Linearization Technique

Linearity is an essential performance parameter in power amplifier design. It defines the ability of the PA to process an input signal [14]. In this work, pre-distortion linearization technique is proposed and adapted. A pre-distorter works such that it produces anti-phase input sideband signals which tends to cancel off the unwanted sideband produced by the power amplifier. This is quantified through the amount of gain expansion and phase compression produced at the input of the PA in order to cancel out the respective gain and phase response at the desired output power.

In this work, to meet the ACLR specification at high output power, a passive pre-distorter is integrated at the input of the class-E PA to provide third order intermodulation (IMD3) cancellation. IMD3 cancellation occurs when there is a 180° phase shift [15] between the output of the pre-distorter and output of the class-E PA. This cancellation is dominant at higher output power. This phenomenon can be described from the following simplified Volterra series [16]

$$v_{out} = a_1 v_{in} + \left(a_1 b_3 - a_3\right) v_{in}^3 - 3a_3 b_3 v_{in}^5 - 3a_3 b_3^2 v_{in}^7 - a_3 b_3^3 - v_{in}^9, \quad (8)$$

where a_1 and a_3 represents the amplitude at fundamental frequency and IMD3 produced by the PA, respectively while b_3 is the IMD3 amplitude produced by the pre-distorter. In order to obtain an IMD3 cancellation at specific output power, the third degree terms need to have opposite signs, in the condition of $b_3 > a_3/a_1$, [16].

The relationship between IMD3 and adjacent channel power ratio (ACPR) can be described as [17]–[23]

$$ACPR_{dBc} = IMR_{2dBc} + 10\log\left[\frac{n^3}{2\times\left(8\sum_{r=1}^{n-1} N_1(n,r) + 2\sum_{r=1}^{n-1} M_1(n,r)\right)}\right], \quad (9)$$

where $£ = \mathrm{mod}\left(\frac{n}{2}\right)$, n represents number of tones, IMR is the multi-tone IMD to carrier ratio,

$$\sum_{r=1}^{n-1} M_1(n,r) = \frac{n^2 - £}{4} \text{ and } \sum_{r=1}^{n-1} N_1(n,r) = \frac{2n^3 - 3n^2}{24} + \frac{£}{8}.$$

Figure 5 illustrates the simulated AM-AM responses of the PA prior and after linearization. The proposed novel passive pre-distorter linearizer eradicates the severe gain expansion of the class E PA and flattens it up to 28 dBm of output power.

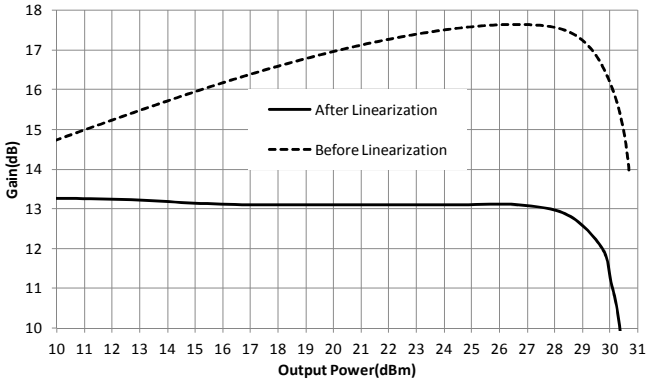

Fig. 5. Simulated AM-AM responses of the Class-E PA before and after linearization.

IV. RESULTS AND DISCUSSION

The fabricated PA with a chip dimension of 1 mm x 1mm is depicted in Fig. 6. Figure 7 illustrates the simulated and measured S-parameter plot of the proposed PA. At 1.95 GHz, S11 and S22 are observed to be less than -10 dB. The power gain exhibited by the PA at the above mentioned frequency is 13 dB.

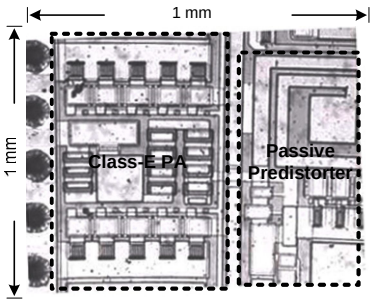

Fig. 6. Photomicrograph of the fabricated LTE PA.

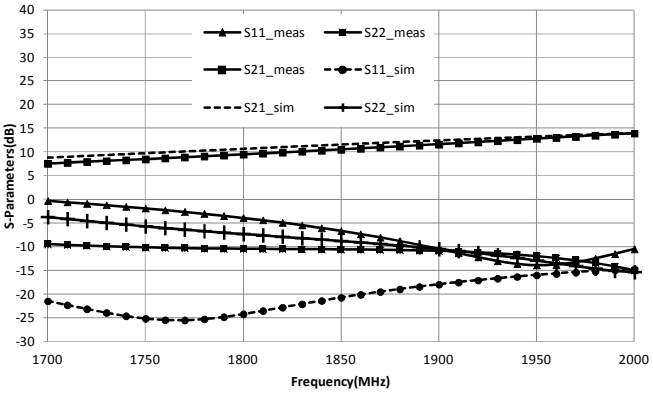

Fig. 7. S-parameter performance of the designed PA.

The measured ACLR and PAE performance at centre frequency of LTE Band 1, 1.95 GHz is depicted in Fig. 8. From Fig. 8, the third order distortion cancellation initiates at an output power of 21 dBm. Maximum cancellation is

observed at 25 dBm output power. This technique helps to push the maximum linear output power to 28 dBm. The PAE measured at this power level is 49 %.

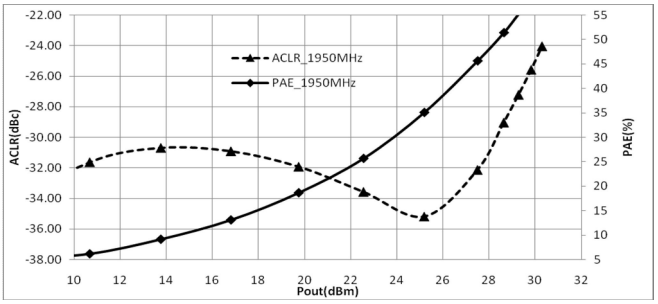

Fig. 8. Measured ACLR and PAE for LTE Band 1.

The performance of the linearized class-E PA has been summarized in Table I.

TABLE I. MEASURED PERFORMANCE SUMMARY AT 1.95 GHz.

Quantity	Result
Technology	2 um InGaP/GaAs HBT
Supply Voltage	4 V
Operating Frequency	1.92 GHz–1.98 GHz
LTE Channel Bandwidth	20 MHz
Max Linear Output Power	28 dBm @ ACLR -30 dBc
PAE	49% @ 28 dBm

Table II summarizes the performance comparison of the proposed PA, respective to other recent reported work. It could be deduced that the proposed architecture observes an optimum PAE while satisfying the ACLR requirement in the 3GPP specification.

TABLE II. PERFORMANCE COMPARISON OF LTE PAS.

Ref	LTE Chan BW (MHz)	Max Linear Pout (dBm)	PAE (%)	Max Pout (dBm)	Chip Area (mm2)	Process
[3]	10	27.8	39	30.1	-	2 µm GaAs HBT+65 nm CMOS
[4]	10	21.6	9	29.4	3	90 nm CMOS
[18]	5	31.8	37	39	6.3	2 µm GaAs HBT
[19]	10	27.5	36.3	-	1.96	2µm GaAs HBT
[20]	10	27.2	34.5	29	2.9	2µm GaAs HBT+0.5µm GaAs PHEMT
This Work	20	28	49	30.7	1	2µm GaAs HBT

V. CONCLUSIONS

In this paper, a novel linearization technique has been implemented on a class-E PA. This linearization technique drives the PA to meet stringent linearity specifications for LTE compliance with 20 MHz channel bandwidth. With a PAE of 49 %, this PA serves as a good candidate in the effort increasing the battery life time of mobile phones intended for 4G wireless communications.

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