http://dx.doi.org/10.5755/j01.eee.20.8.2949 ELEKTRONIKA IR ELEKTROTECHNIKA, ISSN 1392-1215, VOL. 20, NO. 8, 2014

A High Efficiency 1.8W Power Amplifier for Wireless Communications

U. Eswaran[1], H. Ramiah[1], J. Kanesan[1]
[1]*Department of Electrical Engineering, Faculty of Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia*
hrkhari@um.edu.my

***Abstract*—A power amplifier, implemented in 2µm InGaP/GaAs Heterojunction Bipolar Transistor (HBT) is presented. The size of the fabricated chip is 700 µm × 700 µm. With an integrated input matching network, the PA observes an input return loss (S_{11}) of -22 dB. Biased at low quiescent current of 65 mA, it delivers a maximum output power of 1.8 W with 71 % efficiency at 1.85 GHz. The output return loss (S_{22}) of the PA is -15.2 dB. The output matching network is designed to reduce the mismatch loss between the power amplifier and the antenna without compromising the output power and efficiency. The PA also exhibits a K-factor greater than 1 from DC up to 5 GHz, ensuring unconditional stability. The power gain of the PA is 14.9 dB. The measured results verify that the PA is capable to operate at high efficiency and to deliver high output power with a good output return loss.**

***Index Terms*—Heterojunction bipolar transistor (HBT), power amplifier, power added efficiency (PAE), return loss.**

I. INTRODUCTION

Power amplifier (PA) is tasked upon in the amplification of low level signal to a desired output power in a transmitter system. This is accomplished by converting a dc input power to a significant amount of microwave/RF output power [1]–[5].Therefore an efficient transmission is always desired [6]–[10].

Several technologies are utilized in designing PA for various applications in wireless communications. For low voltage application, the HBT technology appears to be prominent. This is due to its inherent characteristic of low collector-emitter offset voltage and low resistance [11]–[13]. Moreover, it has superior electrical characteristics at high frequencies [14], which helps to transmit high output power with minimum parasitic loss. The HBT technology inherits low leakage current, thus eliminating the need to have an extra dc switch to turn off the power supply, which is a common practice in GaAs MESFET amplifiers [15].

An efficient power conversion is always desired in realizing a good PA. Often, power losses in HBT PA are due to thermal effect and mismatch loss in the transmitter system. In HBT technology, the former effect is minimized with ballasting technique. In this technique, a resistor is implemented at the base or emitter of a HBT to prevent the collapse of the collector current in the event one of the HBT unit cell operates at a higher temperature [16]–[19]. The solution to the latter effect is usually found by designing an antenna respective to the output impedance of the PA. Hence a custom antenna design is always needed. This imposes a great inconvenience to the transmitter system designers.

This paper presents the design of a PA which observes less than -12 dB input and output return loss with maximum output power of 1.8 W. The PA has highest PAE of 71 % and power gain of 14.9 dB, while maintaining a broadband stability factor from DC to 5 GHz.

II. POWER AMPLIFIER DESIGN METHODOLOGY

Figure 1 depicts the schematic of the designed PA, encapsulating the HBT transistor, input matching network, output matching network and bias circuit.

The PA employs common emitter structure in order to achieve reasonable trade-off between gain, output power and efficiency [20]. An accurate input impedance matching network is an important criterion since it allows maximum power transfer under a prescribed load condition [21]. Hence, the input matching network integrating C_2, L_1, C_4, L_3 and C_6 has been designed based on the following equation [22]

$$P_{IN} = P_{AVS} M_S, \tag{1}$$

where

$$M_S = \frac{(1-|\Gamma_S|^2)(1-|\Gamma_{IN}|^2)}{|1-\Gamma_S \Gamma_{IN}|^2}, \tag{2}$$

P_{IN}, P_{AVS} and M_S denotes input power to the amplifier, available power from the signal source and mismatch loss between signal source and input of the PA, respectively. If $M_S = 1$, then all the available power from source will be transferred to the input of the PA. This is quantified by a very low input return loss (S_{11}) in the measurement. The objective of $M_S = 1$ is achieved when the condition is satisfied to be

$$\Gamma_{IN} = \Gamma_S^*. \tag{3}$$

The relationship between $_{IN}$ and S_{11} is given by

$$\Gamma_{IN} = S_{11} + \frac{S_{12} \cdot S_{21} \cdot \Gamma_L}{1 - S_{22} \cdot \Gamma_L}, \tag{4}$$

where S_{12}, S_{21}, S_{22} and $_L$ represents the isolation between

Manuscript received November 11, 2013; accepted July 23, 2014.

input and output port of the PA, gain of the PA, output return loss of the PA and load reflection coefficient, respectively. If S_{12} = 0, which translates to a perfect isolation, then $_{IN} = S_{11}$.

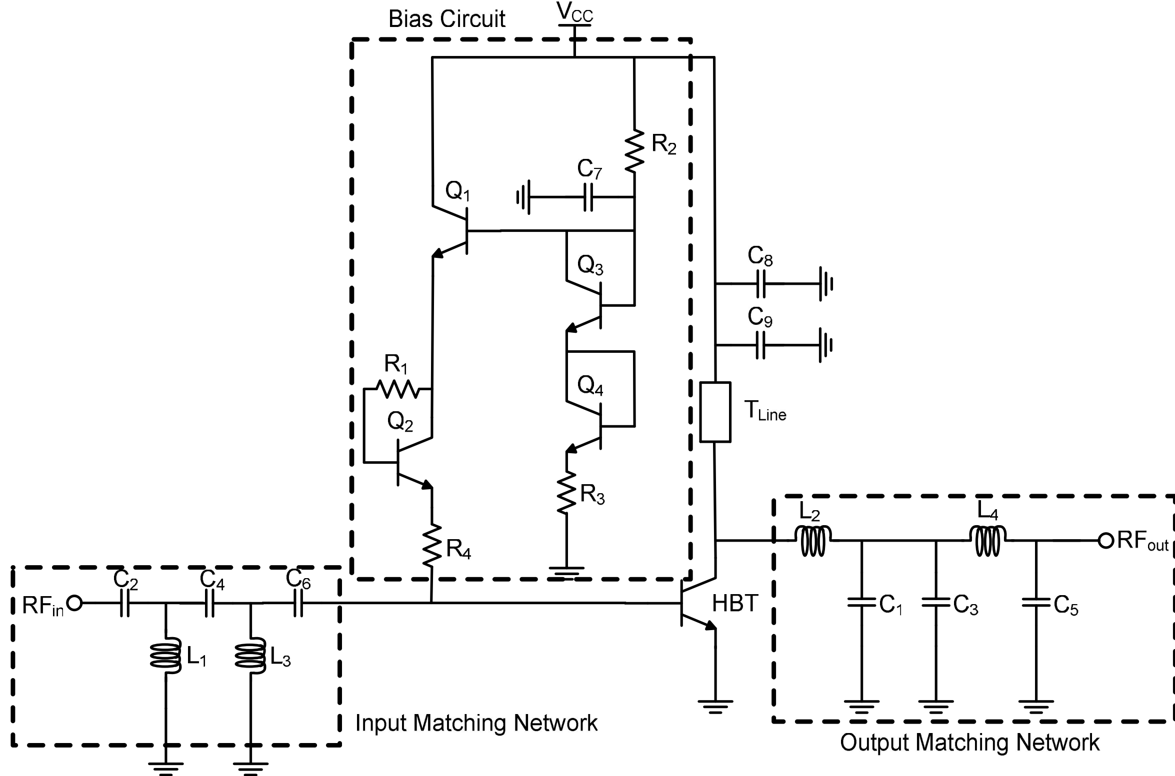

Fig. 1. Schematic of the HBT based PA.

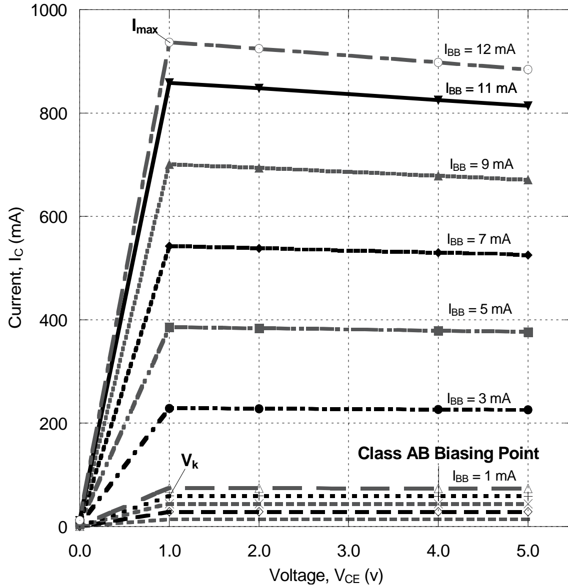

Fig. 2. Deep Class-AB biasing point in the IV curve.

The maximum output power delivered by the PA is determined by its load resistance R_{load}, defined as

$$R_{load} = \frac{V_{dc} - V_k}{I_{\max}}, \tag{5}$$

where V_{dc} is the desired operating voltage, V_k is the I-V curve knee voltage and I_{max} is the maximum current obtained if the device is biased at class-A biasing point. In order to achieve a high PAE with low quiescent collector current, a deep class-AB biasing point is executed, as illustrated in Fig. 2. A deep class-AB bias point reflects a bias point closer to Class-B operation. For V_{CE} = 5 V and I_{bb} = 9 mA, V_{be} = 1.31 V.

R_{load} represents the load resistance of a single unit cell HBT. Since in HBT, the amplifier is built with multiple unit cells, the load resistance is scaled accordingly to the number of unit cell required to deliver the desired maximum output power. Hence the optimum load resistance, $R_{load\text{-}opt}$ is given by [14]

$$R_{load-opt} = \frac{R_{load}}{N}, \tag{6}$$

where $R_{load\text{-}opt}$ defines the HBT device size. The appropriate device dimension ensures minimum tradeoff between maximum output power, PAE and output return loss. In Fig. 1 the proposed output matching network transforms 50 load impedance to $R_{load\text{-}opt}$. Referring to Fig. 1, L_2 is the bondwires which connects the die to the PCB. L_4 is a SMT coil which is capable of holding current up to the level of 2 A. L_2, C_1 and C_3 ensure a maximum output power and PAE is delivered by the PA. The PAE is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \times 100\%. \tag{7}$$

P_{out} represents the output power, whereas P_{in} and P_{dc} reflects the input power and DC power, respectively.The maximum output power transferred can be expressed as [23]

$$P(dBm) = 10\log\left[\left|\frac{(2V_{CC} - V_{sat})^2}{8.R_{load-opt}.10^{-3}}\right|\right]. \tag{8}$$

Referring to Fig. 1, L_4 and C_5 help to deliver PA's output return loss to be less than -10 dB.

Another important parameter which has been given due priority in this work is the unconditionally stability factor, which known as the Rollett factor, K [24]. The power amplifier has been designed to meet this criterion, which is conditioned as [25]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11} \cdot S_{22} - S_{12} \cdot S_{21}|^2}{2|S_{12}||S_{21}|} > 1. \tag{9}$$

In the effort to design the biasing circuit for the PA, current mirror technique is adapted. In Fig. 1, Q_1 acts as a single current mirror to bias up the amplifier. Transistor Q_2 has been added in a cascode integration with Q_1 in order to present a high output resistance, which stabilizes the bias circuit over supply voltage variation. Resistor R_1 acts as a feedback resistor to stabilize Q_2. Transistor Q_3 and Q_4 are a diode connected HBT, which is integrated at the base of Q_1 to exhibit enhanced temperature compensation. Capacitor C_7 helps to mitigate the bias modulation effect. Bias modulation effect is a phenomenon where the bias circuit is modulated by the input modulating signal due to the presence of low impedance at bias circuit output, which is the output of Q_2 referring to the architecture in Fig. 1 [26], [27].

III. MEASUREMENT RESULTS

Figure 3 illustrates the fabricated 700 μm × 700 μm PA using the platform of 2 μm InGaP/GaAs Heterojunction Bipolar Transistor (HBT) technology.

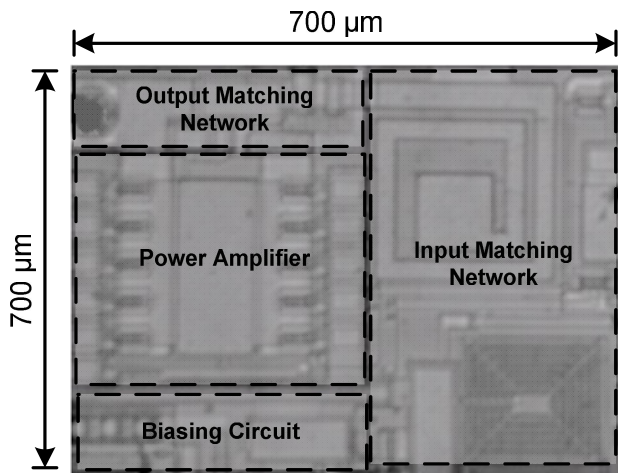

Fig. 3. Micrograph of the fabricated PA.

Figure 4 depicts the small signal performance of the PA. The PA exhibits good S_{11} which is -22.3 dB at 1.85 GHz. This enables the PA to be connected to the baseband-chip in the wireless transmitter line-up with a very minimum input mismatch loss. On the other hand, the S_{22} is -15.2 dB, which helps to reduce the mismatch loss between a 50 antenna and output of PA. The power gain of the PA is 14.9 dB at 1.85 GHz.

Figure 5 depicts the stability plot. It can be observed that the PA has a K-factor more than 1 from DC up to 5 GHz. The good out of band stability of the PA serves to be an added advantage, as the requirement to integrate a filter at the output of the PA is alleviated. The K-Factor greater than 1 indicates PA is unconditionally stable.

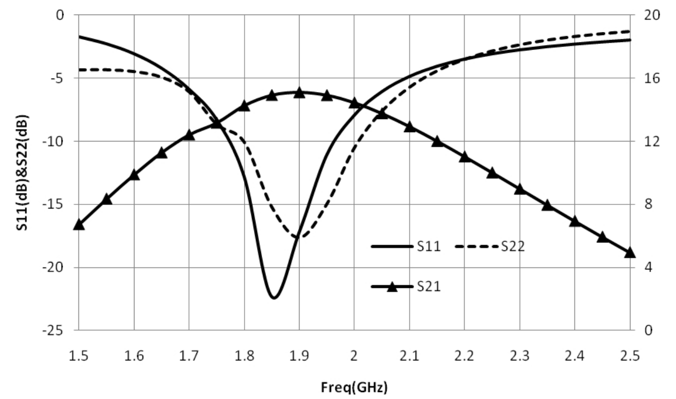

Fig. 4. Small signal plot of the PA.

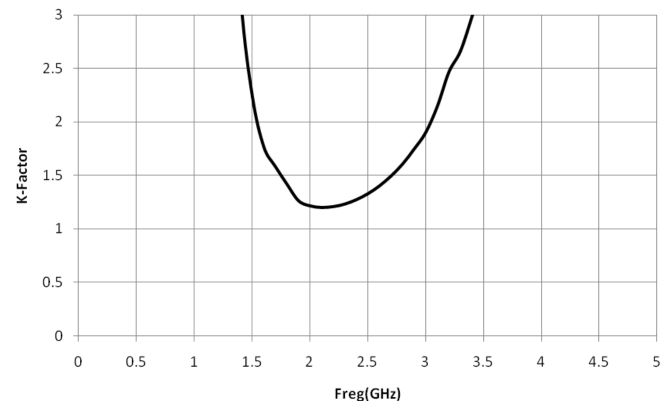

Fig. 5. K- Factor > 1 up to 5 GHz (From DC to 1.4 GHz and from 3.5 GHz to 5 GHz, K-Factor is more than 3).

Figure 6 illustrates the gain and PAE plot respective to the output power at operating frequency of 1.85 GHz. The maximum output power delivered by the PA is 32.5 dBm, which is equal to 1.8 W. The gain variation is observed to be less than 1 dB up to PA's 1 dB compression point which indicates a linear transmission. The 1 dB compression point is 31.5 dBm. The highest efficiency is 71 %, thus approximates close to an ideal Class-B PA's efficiency.

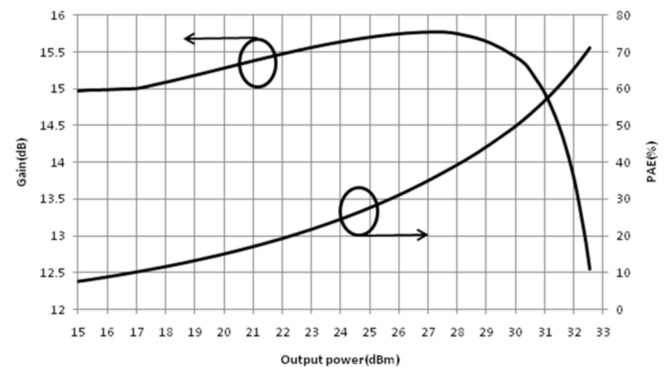

Fig. 6. Gain and PAE vs output power plot at 1.85 GHz.

The performance of the fabricated PA is summarized in Table I.

TABLE I. PA PERFORMANCE SUMMARY.

Quantity	Result
Technology	2 µm InGaP/GaAs HBT
Operating frequency	1.85 GHz
Operating voltage	4 V
Quiscent current	65 mA
Power Gain	14.9 dB
S11	-22.3 dB
S22	-15.2 dB
Max output power	32.5 dBm
PAE	71 %
Stability Factor, K	> 1(DC to5 GHz)

IV. CONCLUSIONS

In this work, the design of a 1.8 W PA for 1.85 GHz operating frequency is demonstrated. Materialized in an InGaP/GaAs HBT technology with an active chip area of 700 µm × 700 µm, the PA delivers a maximum PAE of 71 %, thus enhancing the battery life. On the other hand, the PA exhibits a respective S_{11} of -22.3 dB and S_{22} of -15.2 dB. These results prove that the proposed PA serves to be a prominent solution in reducing the mismatch loss between PA and antenna in a wireless transmitter system while delivering a significant amount of output power and PAE.

REFERENCES

[1] H. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, N. Pothecary, J. Sevic, N. Sokal, "Power amplifiers and transmitters for RF and microwave", *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 814–826, 2002. [Online]. Available: http://dx.doi.org/10.1109/22.989965

[2] R. Gilmore, L. Besser, *Practical RF Circuit Design for Modern Wireless Systems Volume 2*. Norwood: Artech House, 2003, ch. 5.

[3] D. M. Pozar, *Microwave Engineering*. New Jersey: John Wiley &Sons, 2005, ch. 11.

[4] W. A. Davis, K. Agarwal, *Radio Frequency Circuit Design*. New York: John Wiley & Sons, 2001, ch. 9. [Online]. Available: http://dx.doi.org/10.1002/0471200689

[5] P. Colantonio, F. Giannini, E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*. West Sussex: John Wiley & Sons, 2009, ch. 1. [Online]. Available: http://dx.doi.org/10.1002/9780470746547

[6] I.Bahl, P. Bhartia, *Microwave Solid State Circuit Design*. New Jersey: John Wiley & Sons, 2003, ch. 10.

[7] M. Albulet, *RF Power Amplifiers*. Atlanta: Noble, 2001, ch. 1.

[8] B. Razavi, *RF Microelectronics*. New Jersey: Prentice Hall, 1998, ch. 9.

[9] J. Rogers, C. Plett, *Radio Frequency Integrated Circuit Design*. Norwood: Artech House, 2003, ch. 10.

[10] J. S. Love, *RF Front End, World Class Design*. Oxford: Newness, 2009, ch. 5.

[11] T. Miura, T. Shimura, K. Mori, Y. Uneme, H. Nakano, A. Inoue, R. Hattori, N. Tanino, "High efficiency AlGaAs/GaAs power HBT's at a low supply voltage for digital cellular phones", *IEEE GaAs IC Symp. Tech. Dig.*, pp. 91–94, 1996.

[12] Y. Tateno, H. Yamada, S. Ohara, S. Kato, H. Ohnishi, T. Fujii, J. Fukaya, "3.5 V, 1 W high efficiency AlGaAs/GaAs HBT's with collector launcher structure", *IEEE IEDM Tech. Dig.*, pp. 195–198, 1994.

[13] N. Hayama, C-W. Kim, H. Takahashi, N. Goto, K. Honjo, "High efficiency, small-chip AlGaAs/GaAs power HBT's for low voltage digital cellular phones", *IEEE MTT-S Int. Microwave Symp. Tech. Dig.*, pp. 1307–1310, 1997.

[14] A. A. Sweet, *Designing bipolar transistor radio frequency integrated circuits*. Norwood: Artech House, 2008, ch. 4.

[15] T. Yoshimasu, M. Akagi, N. Tanba, S. Hara, "An HBT MMIC power amplifier with an integrated diode linearizer for low voltage portable phone applications", *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1290–1296, 1998. [Online]. Available: http://dx.doi.org/10.1109/4.711326

[16] S. Maas, "Ballasting HBTs for wireless power amplifier operation", *ARMMS Conf.*, Steventon, 2006, pp. 1–9.

[17] W. Liu, A. Khatibzadeh, J. Sweder, H. F. Chau, "The use of base ballasting to prevent the collapse of current gain in AlGaAs/GaAs heterojunction bipolar transistors", *IEEE Trans. Electron Devices*, vol. 43, pp. 245–251, 1996. [Online]. Available: http://dx.doi.org/10.1109/16.481724

[18] J. Jang, E. C. Kan, T. Arnborg, T. Johansson, R. W. Dutton, "Characterization of RF power BJT and improvement of thermal stability with nonlinear base ballasting", *IEEE Journal of Solid State Circuits*, vol. 33, pp. 1428–1432, 1998. [Online]. Available: http://dx.doi.org/10.1109/4.711343

[19] J. D. Yue, Z. W. Rong, Q. J. Jun, G. Pan, X. Ying, "A simple method to optimize the base ballasting resistor of RF power HBT", *7th Int. Symposium on Antennas, Propagation and EM Theory*, Guilin, 2006, pp. 1–4.

[20] B. Zhang, Y. Z. Ziong, L. Wang, S. Hu, T. G. Lim, Y. Q. Zhuang, L. W. Li, "A D-band power amplifier with 30GHz bandwidth and 4.5 dBm P_{sat} for high speed communication system", *Progress In Electromagnetics Research*, vol. 107, pp. 161–178, 2010. [Online]. Available: http://dx.doi.org/10.2528/PIER10060806

[21] J. L. Jimenez-Martin, V. Gonzalez-Posadas, J. E. Gonzalez-Garcia, F. J. Arques-Orobon, L. E. Garcia-Munoz, D. Segovia-Vargas, "Dual band high efficiency class CE power amplifier based on CRLH diplexer", *Progress In Electromagnetics Research*, vol. 97, pp. 217–240, 2009. [Online]. Available: http://dx.doi.org/10.2528/PIER09071609

[22] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*. New Jersey: Prentice Hall, 1997, ch. 2.

[23] K. Walsh, J. Johnson, "3G/4G multimode cellular front end challenges; Impact on power amplifier design", *RFMD White Paper.*

[24] J. M. Rollett, "Stability and power gain invariants of linear two ports", *IRE Trans. Circuit Theory,* pp. 29–32, 1962.

[25] R. Ludwig, P. Bretchko, *RF Circuit Design Theory and Applications.* New Jersey: Prentice-Hall Inc., 2000, ch. 9.

[26] S. C. Cripps, *Advanced Techniques in RF Power Amplifier Design*. Norwood: Artech House., 2002, ch. 3.

[27] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood: Artech House, 2006, ch. 11.