A 5 V to 180 V Charge Pump for Capacitive Loads in a 180 nm SOI Process

Jakob K. Toft*, Ivan H. H. Jorgensen
Institute of Electrical Engineering, Technical University of Denmark,
Elektrovej 325, 2800 Kongens Lyngby, Denmark
jkto@elektro.dtu.dk

***Abstract*—This paper presents two variants of a high step-up ratio charge pump for high voltage micro electro-mechanical system and condenser microphones. The implementations are based on an additive charge pump topology where respectively 46 and 57 cascaded stages are used to generate an output voltage of 182 V from a supply voltage of 5 V. The two charge pumps have been fabricated in a 180 nm SOI process with a breakdown voltage of more than 200 V and respectively occupy an area of 0.52 mm^2 and 0.39 mm^2. The charge pumps can output up to 182.5 V and 181.7 V and are designed to drive a capacitive load with a leakage of 2 nA. When driven with a 100 kHz clock, their power consumption is respectively 40 µW and 20 µW. The rise time of the charge pumps output from 0 V to 182 V is less than 5 ms. The implemented charge pumps exhibit state-of-the-art performance for very high voltage dc-dc capacitive drive applications.**

***Index Terms*—Charge pumps; High voltage techniques; Microelectromechanical systems; Microphones; Silicon-on-insulator.**

I. INTRODUCTION

Micro Electro-Mechanical System (MEMS) based microphones are found in a wide range of consumer products, such as smart-phones, tablets, and smart assistants [1]. Since the first commercialized MEMS microphone was introduced into the market, MEMS microphones went to dominate the market for mobile devices. Before MEMS microphones, electret condenser microphones were used, but as the electret could not tolerate reflow soldering, MEMS became much more popular [2]. Non-electret condenser microphones were not used as they required hundreds of volts for bias voltage [3].

The introduction of smart assistants, e.g., Google Home and Apple Siri, has pushed for higher Signal to Noise Ratio (SNR) performance in microphones [1]. The higher performance is desired at no extra cost in terms of microphone package size nor power consumption. A MEMS microphone package can be less than 2 mm × 3 mm × 1 mm, leaving little volume for the MEMS module and Integrated Circuit (IC) inside the package. Often approximately 1 mm^2 is available for the IC.

The performance of MEMS microphones is limited by the air gap due to the thermal noise from the squeeze film damping effect. The noise can be reduced by increasing the air gap between the two plates in the capacitive microphone, [4] but it will require a higher bias voltage to maintain the sensitivity of the microphone [5]. A recent study investigated using voltages of several hundreds of volts [6] to improve the MEMS SNR.

Several approaches can be used to generate the high voltages desired. However, the only suitable approach for a MEMS microphone is a Charge Pump (CP) that is fully implemented in an IC, as discrete components occupy too much volume. The breakdown voltage of devices in technology processes pose a limitation to fully implemented high voltage charge pumps. In [7], the breakdown limitation is sought circumvented through placing devices on top of the field oxide. In other literature, multi-chip solutions are proposed [8], and a range of studies [9]–[11] have used Silicon-On-Insulator (SOI) processes which feature high breakdown voltages. In this work, a 180 nm SOI process with devices having a breakdown voltage up to more than 200 V is used. The intended application for the charge pumps developed in this work is to supply a bias voltage of 180 V to a MEMS microphone from a 5 V supply, but they may be applicable to condenser microphones as well. Because the load of the charge pump will be capacitive, the charge pump will only need to supply a current equal to the leakage current of the load at 180 V. Condenser microphones can feature insulation resistances of > 10^{15} Ω [12]. A conservative estimate is that the insulation resistance is only 10^{11} Ω, which results in a current of 1.8 nA when 180 V is applied, which when rounded up becomes a current of 2 nA.

A review of the prior art showed that in no other work something with sufficient voltage gain given the area and power restrictions of mobile applications has been implemented. In [10] and [13], high voltage gains were achieved, but at the cost of using an extremely large area. In [14], a small area was used for a charge pump, but the voltage gain was much lower than the required voltage gain of this work. This paper presents our implementation of multiple charge pumps that exhibit very high voltage gain and low area.

The remainder of this paper is organized as follows. Section II presents the used charge pump topology. Section III describes the implementation. Section IV presents simulations and measurements. Section V discusses and compares the results of this work with the prior art. The conclusions are presented in section VI.

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II. CHARGE PUMP TOPOLOGY

The goal for the charge pumps in this work is to supply 180 V to a microphone from a 5 V supply, while maintaining the implementation small with a low power consumption. The target specifications were an implementation smaller than 0.5 mm^2 for the charge pump, Electro Static Discharge (ESD) protection, and output filter, and a power consumption below 20 µW. In addition to the area and power consumption goals, the 0 V to 180 V rise time should be less than 10 ms. A limitation to the implementation is that the clock frequency should not be less than 100 kHz to avoid leakage into the audio band 20 Hz–20 kHz.

In [10], a voltage gain of 80.0 was achieved using a modified Pelliconi topology [15], where a 4-phase clock scheme was implemented to control the 4 transistors of the Pelliconi topology individually. This results in a significantly more complicated topology compared to [15], where the number of transistors and capacitors is more than doubled. The increased number of transistors results in more parasitic capacitance, which affects the voltage gain and power consumption. The reduced voltage gain due to parasitic capacitance can be compensated in two ways, either the pumping capacitance can be increased in size, or more charge pump stages can be added, both approaches increase the area. The ideal output voltage V_{out} of the Pelliconi topology, when parasitic capacitances are included, is given by

$$V_{out} = V_{supply} \times (1 + N \times \alpha), \tag{1}$$

where N is the number of stages, V_{supply} is the supply voltage, and α is given by

$$\alpha = \frac{C_{pump}}{C_{pump} + C_{par}}, \tag{2}$$

in which C_{pump} is the pumping capacitance and C_{par} is the parasitic capacitance. The parasitic capacitance is a combination of top plate parasitics on the pumping capacitor and the parasitic capacitances of the transistors connected to the top plate of the capacitor. To maximize the voltage gain, α must be maximized, which is done by minimizing C_{par} or maximizing C_{pump}. Maximizing C_{pump} will increase the area, whereas minimizing C_{par} is a question of topology and available devices.

The topology with fewest active devices connected to the top plate of the pumping capacitor is the Dickson topology [16]. A shortcoming of the Dickson topology is that the voltage stress on the active devices is two times the supply voltage. Higher voltage rated devices can be used, but the 10 V transistors featured in the used process technology can sustain 10 V only between drain and source, from gate to source the voltage cannot be more than 5.5 V. To control the gate voltage, additional circuitry is needed, and the parasitic capacitances on the top plate of the pumping capacitor will be increased. Alternatively, 10 V diodes from the process could be used, but these have a parasitic capacitance which is 20 times higher than that of 5 V and 10 V transistors. Furthermore, the Dickson topology will suffer from a relatively longer settling time compared to the Pelliconi topology. As when the output voltage nears its maximum in the Dickson topology, the voltage across diodes becomes small, reducing the current passing through the diode. The transistors in the Pelliconi topology will be in the triode region when the drain source voltage is low, which maintain decent conductivity. Alternatively, the Dickson topology could be driven by a 2.5 V supply and implemented using 5 V devices with less parasitic capacitance, but this would increase the required voltage gain by a factor of two, increasing the charge pump size by the same factor. Furthermore, thereby increase the rise time significantly.

A review of the Pelliconi topology revealed that the topology is often modified to overcome latch-up challenges [10], [17], [18]. These modifications require a significant amount of extra transistors and capacitors, which increase the parasitics and the area of the implementation. The added cost of modifications is small when the charge pumps are designed for higher power applications where hundreds of µW or mW are to be supplied by the charge pump. To supply these power levels, the pumping capacitors must be large, which means C_{pump} is maximized instead of C_{par} minimized. For the application in this work, the output power to be supplied is 360 nW, which can be supplied by very small capacitors, which means that maximizing the pumping capacitance will cost an unacceptable amount of area.

By adding a single capacitor and two transistors to the Pelliconi topology, the Favrat [19] topology, as illustrated in [20], Fig. 1, can be realised. In the Favrat topology the capacitor C_{bulk} is used to keep the bulk voltage high during transitions and thereby avoid latch-up. The Favrat topology has the same voltage scaling as the Pelliconi (1), and a minimum of added devices to avoid latch-up. The Favrat topology is the topology we use for the charge pump implementations presented in this work.

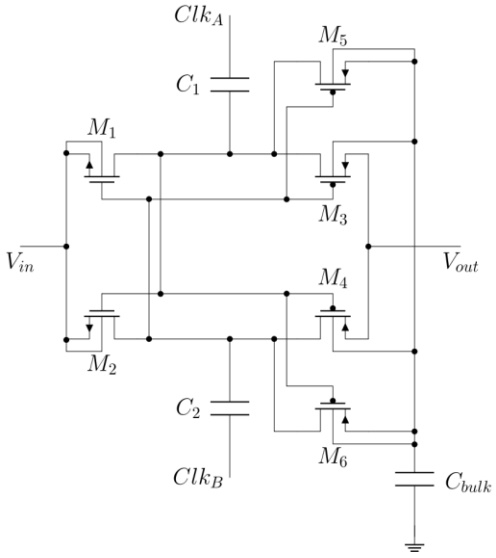

Fig. 1. The Pelliconi based Favrat charge pump topology as illustrated in [20].

III. IMPLEMENTATION OF CHARGE PUMP

In Fig. 2, a block diagram of the charge pump implementation is depicted, illustrating the connection of the different blocks of the charge pump. The ESD protection is

located before the output filter such that charge pump output ripple due to leakage in the ESD is filtered. Not depicted in Fig. 2 is the low voltage ESD protection on Clk_{in}, V_{dd}, and ground.

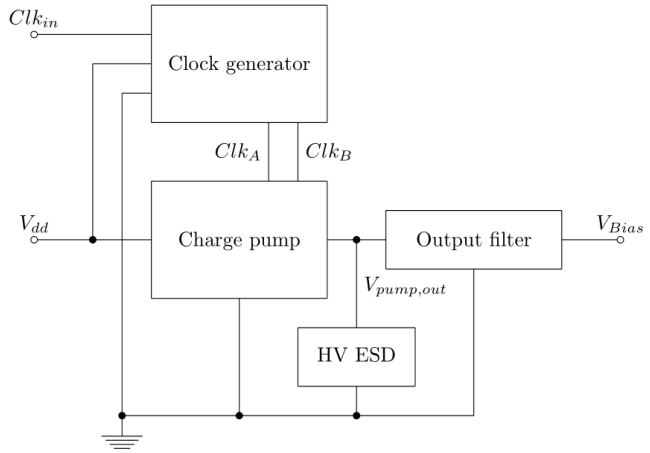

Fig. 2. System overview of charge pump implementation with assisting circuitry.

A. Charge Pump Core

Two charge pump variants were implemented in this work: one variant has a pumping capacitor of 75 fF and the other variant has a capacitor of 300 fF. The 75 fF variant was implemented to achieve a minimum area and minimum power implementation, and the 300 fF variant was implemented for comparison and to have a variant that is less sensitive to parasitic capacitances.

As the Favrat topology features low voltage stress across every transistor, a stress of V_{supply}, the charge pumps were implemented using 5 V transistors given the 5 V supply. The transistors were chosen to be minimum size, as the on resistance of minimum size transistors was low enough for complete charge transfer, which is also a contribution of the small pumping capacitors. Larger transistors would introduce more parasitic capacitance, decreasing the voltage gain.

The 75 fF pumping capacitor size was chosen based on the available capacitor cells in the used technology process and Process Design Kit (PDK). The capacitor unit cells of sufficient voltage rating had a capacitance of 37.5 fF, which proved to be too small with regard to the parasitic capacitances of the transistors. Two unit cells had to be used to form capacitors of 75 fF to minimize the area of the charge pump. Using larger capacitances, increased the voltage gain, which reduced the number of stages required to reach 180 V, but increased the area of the charge pump. The size of the bulk-biasing capacitor was chosen based on the simulation results, with a goal of making it as small as possible.

The 75 fF variant was implemented as 57 cascaded charge pump stages, and the 300 fF variant - as 46 stages. The final number of stages to use for each variant was determined through simulations. The charge pump chains were sized such that the simulated output voltage is approximately 190 V with parasitic capacitances included in the simulation. The 190 V goal was used to achieve some margin. The 300 fF variant requires less stages as the larger pumping capacitance achieve a higher α, see (2). The pumping capacitors themselves have parasitic capacitances that scale with the size of the capacitor, so it is not possible to achieve $\alpha = 1$, but the parasitic capacitances of the transistors are smaller relative to the pumping capacitor of 300 fF than to the capacitor of 75 fF.

Due to the sensitivity to parasitic capacitances, a lot of effort was spent during layout on minimizing the parasitic capacitances between nodes and metal routed in higher metal layers to avoid coupling with the substrate and ground.

B. Clock Generator

The charge pump is clocked using a crossing clock scheme, instead of the non-overlapping clock scheme used in literature [15], [19], as the crossing clocks, Clk_A and Clk_B in Figs. 1–3, reduce the reverse currents and thereby achieve a higher voltage gain [20].

To generate the crossing clock signals, the clock generator depicted in Fig. 3 was used. The last inverter in each lane is larger than the other inverters to achieve the drive capability. The clock signals were verified in simulations to cross at half supply voltage across process corners.

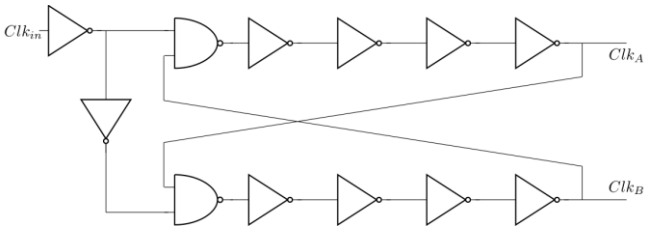

Fig. 3. Clock generator topology.

C. Charge Pump Output Filter

To reduce ripple on the output of the charge pump, an output filter was implemented as depicted in Fig. 4 as illustrated in [20], Fig. 2. The filter was implemented as two shunted RC-filters in series, where the resistors are realized as diode coupled PMOS transistors. An inherent property of the filter is that voltages across the diodes that are larger than the forward voltage of the diodes will result in a small filter time constant, which enables faster settling. The diodes serve as a path for Electro Static Discharge (ESD) protection.

The capacitors C_1, C_2, and C_3 in Fig. 4 are 200 V capacitors and their sizes are respectively 1.7 pF, 6.9 pF, and 14.8 pF, which results in a -3 dB cut-off frequency of 0.052 Hz.

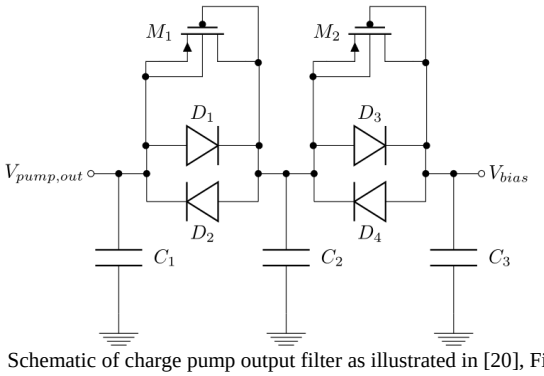

Fig. 4. Schematic of charge pump output filter as illustrated in [20], Fig. 2.

D. ESD Protection on Charge Pump Output

Because the minimum sized 5 V transistors are used for

the implementation of the charge pump, the ESD protection is required. The used ESD protection was implemented using modules from the PDK. The modules are based on stacked PMOS transistors as depicted in Fig. 5 and are rated for a maximum voltage, at which the leakage is approximately 10 pA.

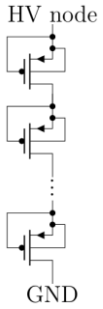

Fig. 5. Stacked PMOS transistors for HV ESD protection.

The multiple ESD versions were implemented to investigate the effect of the ESD protection. Both the 75 fF and 300 fF variants were implemented with ESD rated for a maximum voltage of 210 V and 285 V, furthermore the 75 fF variant was also implemented in a version without ESD.

IV. Simulation and Measurement Results

A. Implementation Area

The area of the charge pump variants implemented in this work is listed in Table I with a breakdown of the size of the different modules. The clock generator area is included in the area of the charge pump core. A micrograph of the physical IC is shown in Fig. 6, where four of the charge pump implementations are highlighted in colour.

TABLE I. AREA OF IMPLEMENTED CHARGE PUMP VARIANTS.

Pump variant	ESD version	Core area [mm^2]	ESD area [mm^2]	Filter area [mm^2]	Total area [mm^2]
300 fF	210 V	0.260	0.093	0.145	**0.498**
300 fF	285 V	0.260	0.119	0.145	**0.524**
75 fF	None	0.125	-	0.145	**0.270**
75 fF	210 V	0.125	0.093	0.145	**0.363**
75 fF	285 V	0.125	0.119	0.145	**0.389**

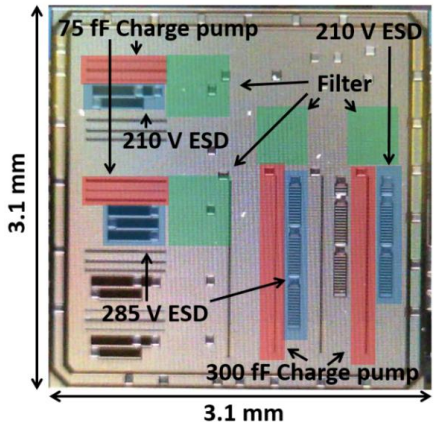

Fig. 6. Micrograph of IC with charge pumps highlighted.

B. Measurement Setup

For the measurements, each of the charge pump variants and versions were bonded in three samples, referred to as IC1, IC2, and IC3. More samples were not bonded due to a limited availability of silicon dies. The silicon dies were bonded in ceramic packages where leakage was measured to be less than 20 pA at a 200 V potential difference between two pins.

The measurements were carried out using a test-board with a voltage follower such that instruments would not unintentionally load the charge pump output. The operational amplifier used for the voltage follower is an OPA129 by Texas Instruments, and it features an input bias current of less than 250 fA. Leakage in the test-board was measured to be less than 30 pA at a potential differences of 200 V.

The instruments used for the measurements of the charge pumps are listed in Table II along with the application of the instrument. The Keithley 2450 SourceMeter was used as an electronic load for the charge pump to ensure consistent loading of the charge pumps in all measurements. The test-board along with the instruments is depicted in Fig. 7, not including the oscilloscope.

TABLE II. INSTRUMENTS USED FOR MEASUREMENTS.

Instrument	Application
Keithley 2450	Power supply for charge pump
Keithley 2450	Electronic load for charge pump
Keysight 33622A	Clock generator for charge pump
Rigol DP832	Power supply for test-board
SM400-AR-4	HV power supply for test-board
Rigol DS 4024	Oscilloscope

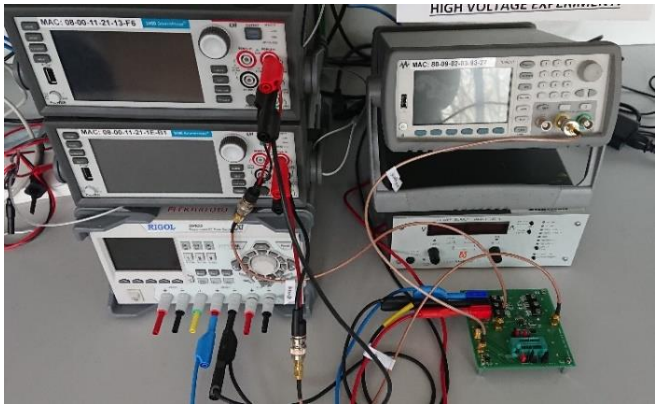

Fig. 7. Test setup used for measurements of the bonded charge pumps.

C. Output Voltage and Power Consumption

The steady-state output voltage and power consumption of the charge pump variants and their ESD versions were measured on each sample at an output load of 2 nA, the measurement results are listed in Table III. From the table, a maximum of 0.7 % variation in output voltage and 1.8 % in power consumption across the samples can be observed. Across the temperature range of -20 °C–70 °C, the output voltage of each chip varied by a maximum of 0.8 %.

Due to the low variation in measurements, it was decided to use only the 285 V ESD versions of the two charge pump variants for the remainder of the measurements.

In Table IV, the measured output voltages and power consumption of the two charge pump variants are listed together with simulation results. Three samples of each variant were measured and averaged.

TABLE III. MEASURED STEADY-STATE OUTPUT VOLTAGE AND POWER CONSUMPTION FOR IC1, IC2, AND IC3 OF THE DIFFERENT CHARGE PUMP VARIANTS AND VERSIONS @ 2 MHZ AND 5 V SUPPLY.

Pump variant	ESD version	Output voltage [V]			Power consumption [µW]		
		IC1	IC2	IC3	IC1	IC2	IC3
300 fF	210 V	182.5	182.8	182.4	624.9	629.0	628.1
300 fF	285 V	182.4	182.8	182.4	616.1	621.0	618.3
75 fF	None	182.6	182.1	181.7	324.5	322.7	324.1
75 fF	210 V	182.4	181.8	181.5	338.2	337.9	334.1
75 fF	285 V	181.6	181.9	181.5	325.3	328.7	323.0

TABLE IV. OUTPUT VOLTAGE AND POWER CONSUMPTION OF MEASURED AND SIMULATED CHARGE PUMPS WITH 285 V ESD @ 2 MHZ AND 5 V SUPPLY.

	Output voltage [V]	Power consumption [µW]
300 fF charge pump:		
Measured (average)	**182.5**	**618.5**
Simulation w/PEX	(+3.1 %) **188.2**	(+8.7 %) **672.5**
Simulation w/o PEX	(+20.3 %) **219.5**	(- 83.3 %) **103.3**
75 fF charge pump:		
Measured (average)	**181.7**	**325.7**
Simulation w/PEX	(+5.7 %) **192.1**	(+1.0 %) **328.8**
Simulation w/o PEX	(+30.3 %) **236.8**	(-67.9 %) **104.5**

As it can be observed from Table IV, there are significant differences between the measurement and the simulation. It can also be observed that Parasitic Extraction (PEX) has a large impact on output voltage and power consumption, up to an 83.3 % difference. It can also be seen that the output voltage of the 75 fF variant is more heavily impacted by parasitics. The charge pumps are very susceptible to parasitics and a slight deviation between PEX and reality might have a significant impact. Therefore, the difference between PEX simulations and measurements is deemed reasonable.

In Fig. 8, the output current as a function of output voltage is plotted for the 75 fF and 300 fF charge pump variants. From Fig. 8, it can be observed that the 300 fF charge pump variant has a significantly higher supply capability at lower voltages than the 75 fF variant, approximately 3 to 4 times higher, as expected given the pump capacitor sizes. An interesting point is that the 300 fF variant is not able to reach a significantly higher output voltage than the 75 fF charge pump, which indicates that the output voltage is limited by the parasitic capacitances in the charge pumps.

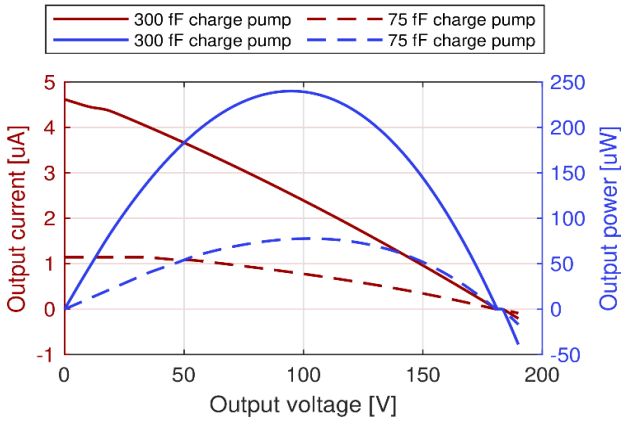

Fig. 8. Measured IV-curve and output power of charge pump outputs @ 2 MHz and 5 V supply.

In Fig. 8, the output power is plotted as a function of the output voltage, and the maximum power delivery at output voltages is around 98 V–102 V. The maximum output power is respectively 243 µW and 78 µW for the 300 fF and 75 fF variant. If the charge pumps were run at higher frequencies, they would be able to deliver more power, but that is not the intended application of this work.

When the charge pumps are run with a 2 MHz clock and the output voltage is approximately 182 V, the output power is around 364 nW, and the power efficiency of the charge pumps is 0.06 % for the 300 fF variant and 0.11 % for the 75 fF variant. This is a low output power and low efficiency, but high output power and high efficiency is not the focus of the charge pumps implemented in this work.

D. Rise Time

The 0 % to 95 % rise time was measured for the charge pumps across multiple frequencies. The start-up transient for the 75 fF variant with 285 V ESD is shown in Fig. 9, and the measured rise times are listed in Table V.

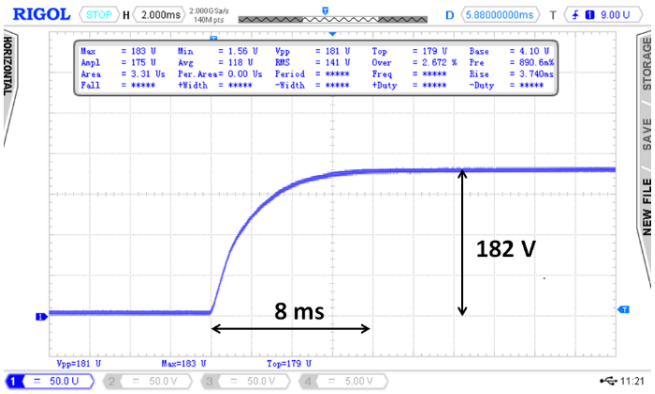

Fig. 9. Measured start-up transient of 75 fF charge pump @ 2 MHz and 5 V supply.

TABLE V. MEASURED RISE TIMES OF THE 75 FF AND 300 FF CHARGE PUMPS WITH 285 V ESD AND 5 V SUPPLY.

Charge pump variant	1 MHz	2 MHz	4 MHz
300 fF	4.94 ms	2.47 ms	1.29 ms
75 fF	15.0 ms	7.44 ms	3.67 ms

From Table V, it can be observed that the 300 fF charge pump variant has a faster rise time than the 75 fF variant, which is due to the higher pumping capability of the 300 fF variant. It can be observed that a faster clock reduces the rise time, and for the measured range, the rise time and the clock frequency are close to being directly proportional.

E. Voltage and Current Scaling with the Clock Frequency

In Fig. 10, the output voltage as a function of the clock frequency is depicted for the 75 fF and 300 fF charge pumps at a load of 2 nA. The output voltage for the 300 fF charge pump can maintain an output voltage of over 180 V down to a frequency of 50 kHz, where the 75 fF charge pump around 200 kHz is beginning to drop below 180 V.

Additionally, the measurements show the same trend as the simulations, although with the same difference (approximately 6 V–10 V) observed in other measurements.

The measurements of the input current across different clock frequencies were carried out, and it was observed that the input current, and thereby the power consumption, are

directly proportional to the clock frequency in the frequency range of 500 kHz–16 MHz.

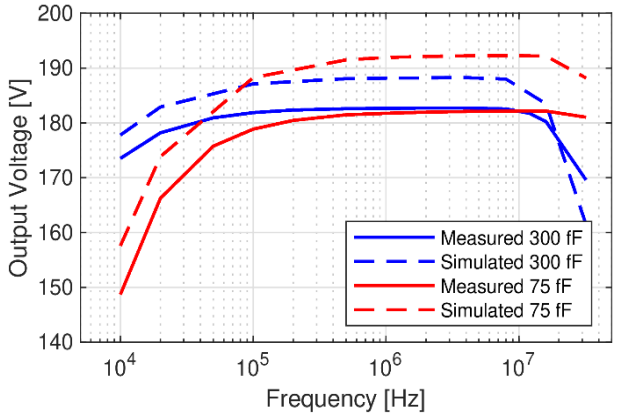

Fig. 10. Measured and simulated output voltage vs charge pump clock frequency.

F. Output Ripple

The measurements of the output ripple from the 300 fF charge pump are depicted in Fig. 11, where the ripple is not detectable as it is below the noise floor of the used instrument setup. The measurements were carried out for the 75 fF charge pump as well, and no ripple was detectable there either.

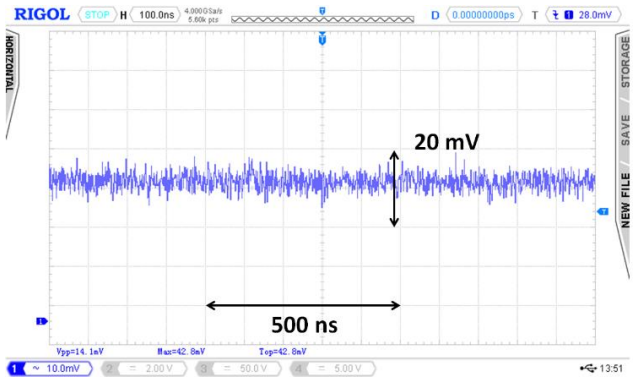

Fig. 11. Measured ripple on the output of the 300 fF charge pump running at 2 MHz and 5 V supply.

In the simulations, small voltage spikes of 100 µV were present at clock transitions for the 300 fF charge pump variant, and spikes of 25 µV were present for the 75 fF charge pump variant.

V. DISCUSSION

A. Area and Power Consumption

The charge pumps presented in this work were developed for MEMS and condenser microphones with a target specification of a 180 V output voltage from a 5 V supply, an area smaller than 0.5 mm^2, a power consumption of less than 20 µW, and a secondary goal of a rise time less than 10 ms.

The 75 fF charge pump was implemented on less than the 0.5 mm^2, use 20.8 µW, and reach 178.5 V when running at a clock frequency of 100 kHz. To summarize, the 75 fF variant charge pump is very close to meet the target specifications. The 300 fF variant is a bit further from the target, as it is larger than 0.5 mm^2 and use almost 40 µW when run at 100 kHz. The 300 fF variant could be run at lower frequencies, but at the risk its switching frequency will be more likely to leak into the audio band.

None of the variants can reach a rise time of less than 10 ms when run with a 100 kHz clock. However, since the start-up time is short compared to the operating time of the microphones in mobile applications, a 2 MHz clock can be used during the start-up, and the system can then change to a 100 kHz clock to save power.

B. Comparison with Prior Art

Table VI presents a summary of the specifications of the presented charge pumps and the specifications of the relevant prior art for the comparison.

If the size of the ESD protection and output filter is not considered, the implementations in [9], [14], [20] are of similar area as the charge pump cores of this work, but only achieve step-up ratios of respectively 3.2, 19, and 13.1, while also having a significantly higher input power. In [9], where no input power or efficiency specification was available, it must be assumed that the input power is at least the same as the output power, which is up to 44 times higher than the input power in this work.

The implementations in [10] and [13] achieve step-up ratios of 80.0 and 32.4 compared to the step-up ratio of 36.4 achieved in this work, however, those implementations use an area that is respectively 286 and 61 times larger, and an input power which is up to 17,690 and 5,225 times higher.

TABLE VI. COMPARISON WITH FULLY INTEGRATED STEP-UP CONVERTERS IN PRIOR ART.

Specification	Unit	[21]	[9]	[10]	[13]	[22]	[14]	This work			
								300 fF		75 fF	
Technology		0.18 um bulk CMOS	0.6 um SOI w/MEMS	1 um SOI	0.35 um HV CMOS	130 nm bulk CMOS	65 nm bulk CMOS	180-nm SOI		180-nm SOI	
Topology		Boost	CP	CP	CP	CP	CP	CP		CP	
V_{supply}	[V]	1.0	5.0	5.0	3.7	0.4	2.75	5.0		5.0	
V_{out}	[V]	3.2	95.2	400	120	1.5	36	182.5	181.5	181.7	178.5
Clock freq.	[MHz]	118	20	-	10	0.01	4	2	0.1	2	0.1
Voltage gain	[V/V]	3.2	19	80	32.4	3.75	13.1	36.5	36.3	36.3	35.7
Efficiency		56 %	-	2.5 %	12.6 %	2.56 %	22 %	0.06 %	0.9 %	0.11 %	1.7 %
Output power		64 mW	906 µW	9.2 mW	13.7 mW	-	144 µW	365 nW	363 nW	363 nW	357 nW
Input power		114 mW	-	368 mW	108.7 mW	-	655 µW	618.5 µW	39.7 µW	325.7 µW	20.8 µW
Area	[mm^2]	0.52	0.29	103.06	21.84	0.005	0.18	0.52		0.39	

In [22], a very small implementation is achieved, but the operating voltage and voltage gain is also small compared to what is achieved in this work, and the used topology does not scale well.

As stated in Section II, if the topologies of prior art with high voltage gain are used, the capacitors and transistors can be scaled down in size due to the low output power requirement of MEMS microphones. But the topologies contain more parasitic elements, requiring more area to compensate, and thereby result in implementations that would be larger than the ones presented in this work. The exception is the Dickson charge pump topology used in [9], which may be possible to implement on less area, but it has the downside of larger voltage stresses and settling time. If a Dickson topology with a 2.5 V supply was implemented, it could be smaller while keeping voltage stresses within device ratings, but it would require twice as many stages as the charge pump implemented in this work, thereby resulting in a settling time which is much longer.

VI. CONCLUSIONS

In this paper, the implementation of two charge pumps for high voltage biasing of microphones in mobile applications were presented. The implemented charge pumps are able to generate bias voltages of approximately 182 V, for capacitive loads with a leakage of 2 nA. Both charge pumps exhibit a state-of-the-art performance for high voltage capacitive drive charge pumps, as the 182 V is generated from a supply voltage of 5 V. This results in a step-up ratio of 36.4, which is unprecedented compared to charge pumps with comparable size and power consumption in prior art.

Furthermore, the two charge pump variants illustrated the impact of parasitic capacitances, as the implementation with larger pumping capacitors achieved a higher voltage gain per stage. The 300 fF charge pump variant only required 46 cascaded stages to output 182.5 V from a 5 V supply, whereas the 75 fF variant required 57 cascaded stages to output 181.7 V.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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