Design and Implementation of a Hybrid UWB Pulse Generator for Automotive Radar

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***Abstract*—The design of a hybrid pulse generator that supports a variable pulse width and a pulse repetition interval (PRI) is proposed and demonstrated for an ultra-wide band (UWB) pulse-Doppler radar. UWB pulse-Doppler radar is required for implementing full digital systems for reliability and flexibility regardless of temperature. It is difficult to apply existing analog components and digital pulse generators with broadened pulse widths. To overcome these limitations, the pulse generator is developed using a digital pulse generator and a 24 GHz RF transmitter. The digital pulse generator is composed of a narrow bandwidth (NB) pulse generator and a pulse chopper based on a serializer-deserializer (SerDes) block on a field-programmable gate array (FPGA). The 24 GHz RF transmitter adopts a homodyne architecture. The digital pulse generator required 1 % of the FPGA Slice registers and 1 % of the FPGA Slice LUTs on a Xilinx Virtex-5 lx50. Using a 2 ns pulse width resolution and an 8 ns PRI resolution, we were able to change the pulse width and the PRI. The pulse width can be measured over the duration of 2 ns to 10 ns.**

***Index Terms*—UWB, digital impulse generator, SerDes, FPGA.**

I. INTRODUCTION

Vehicle radar has received much attention in recent years as a means of short distance vehicle detection for Intelligent Transport Systems (ITS) [1]. In fact, Short-Range Radar (SRR) [2], [3] is very popular in surveillance and vehicle detector systems. Because SRR is used in vehicles, the Federal Communications Commission (FCC) has dedicated the spectrum from 22 to 29 GHz for UWB radar with a power limit of –41.3 dBm/MHz [4]. Here, the UWB signal is defined as an absolute bandwidth larger than 500 MHz or a relative bandwidth up to 20 %. Therefore, UWB radar needs to implement a pulse generator with a 2 ns pulse width to satisfy the regulations of the FCC. The short pulse signal leads to many advantages, such as high spatial resolution for radar systems, high fading margin for communication systems in multipath environments, and high ranging capability for wireless sensor network terminals [5]–[6]. Over the past few decades, many approaches have been designed and implemented to generate such a pulse signal. Analog High Frequency (HF)-based pulse generators are less tunable for the pulse width and pulse repetition interval (PRI); these generators also exhibit reduced variation according to temperature. CMOS-based pulse generators have received much attention for single chip applications. However, because the flexibility of conventional CMOS pulse generators has decreased, these devices are limited for various applications. FPGA-based pulse generators have great flexibility. Due to the critical path of the FPGA, FPGA-based digital pulse generators yield a broadened pulse width with a narrow bandwidth. To avoid this problem, we use a narrow bandwidth (NB) pulse generator with a low clock (LC) and a pulse chopping technique with a high clock (HC) based on a serializer-deserializer (SerDes) block. To improve the performance and flexibility, this paper proposes a hybrid UWB pulse generator with a wave design. The hybrid UWB pulse generator is composed of a digital pulse generator and a 24 GHz RF transmitter. Table I shows the HF component design and CMOS-based pulse generator from related studies.

TABLE I. RELATED STUDIES.

	Characteristics	**References**
Analog HF-based pulse generator	These analog pulse generators are less tunable for the pulse width and pulse repetition interval (PRI); they reduce variation according to temperature.	As an analog pulse generator, ref. [7] represents a monocycle pulse generator that was developed using a Schottky diode, step-recovery diode (SRD), and coplanar waveguide. In [8], the analog monocycle pulse generator is composed of an SRD, Schottky diode, and dual resistive loaded shunt stubs.
CMOS-based digital pulse generator	Due to the presence of a fixed gate circuit, these CMOS digital pulse generators cannot allow the pulse width to vary.	As a digital pulse generator, ref. [9] and [10] propose a CMOS pulse generator using a digital gate, such as an XOR or NOT. In [11], a CMOS pulse generator is proposed through a combination of flip-flop and multiphase clocks. In [12], the CMOS pulse generator consists of a glitch generator, a pulsed oscillator, and a pulse-shaping filter.

II. IMPLEMENTATION OF A HYBRID UWB PULSE GENERATOR

A. UWB Pulse Signal

In the transmitter, pulses are initiated by a pulse generator that generates rectangular monocycle pulses with sub-nanosecond duration. The transmitted signal can be

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expressed as

$$s(t) = A_T \cdot \sum_{n=0}^{N} p(t - n \cdot T_{PRI}), \quad (1)$$

where *p(t)* is the rectangular pulse, given by:

$$p(t) = [U(t) - U(t - \tau_p)], \quad (2)$$

$$U(t - t_0) = \begin{Bmatrix} 1 & t \geq t_0 \\ 0 & t \leq t_0 \end{Bmatrix}, \quad (3)$$

where A_T is the amplitude of the transmitted signal, τ_p is the pulse width, *U(t)* is the unit step function, and T_{PRI} is the pulse repetition interval (PRI) obtained from the pulse repetition frequency (PRF), which is given as $T_{PRI} = 1/f_{PRI}$. Fig. 1 shows the time domain signal for a UWB pulse signal.

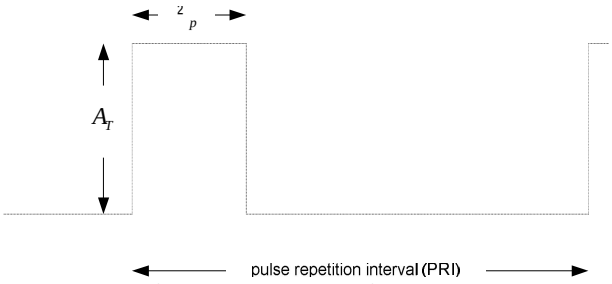


Fig. 1. Schematic of the time domain signal for a UWB pulse signal.

B. UWB Digital Pulse Generator

We designed a digital pulse generator that supports a variable pulse width and PRI for UWB radar. The FPGA-based pulse generator has great flexibility. However, due to the critical path of the FPGA, the FPGA-based digital pulse generator yields a broadened pulse width with a narrow bandwidth. To avoid this problem, we use an NB pulse generator with an LC and a pulse chopping technique combined with an HC based on a serializer-deserializer (SerDes) block. Figure 2 provides a block diagram of the hybrid UWB pulse generator. Figure 3(a) provides a block diagram of the UWB digital pulse generator. Figure 3(b) provides a specific block diagram of the UWB digital pulse generator.

First, the procedure of the developed UWB digital pulse generator is as follows. Using a phase-locked loop (PLL) block, an external clock with a frequency of 50 MHz is converted to the LC and the HC. The LC and HC clock signals have frequencies of 100 MHz and 500 MHz, respectively. The LC determines the pulse width of the NB pulse generator (NBPG) block. A counter block serves to control the length of the PRI. The counter block generates a PRI_START signal when the counter in the PRI_CNT reaches zero. Here, CNT stands for the counter. The NBPG block produces a data output, with the low clock (DOLC) signal as the pulse signal, of 10 ns whenever the PRI_START signal from the counter block is activated. To change the pulse width, we use a 5 bit-mux block and 1 selected register block. Each bit-mux block chooses either the DOLC signal or the zero signal, according to the selected register block. When the selected register block selects a code of 10000, a pulse signal that has a 2 ns pulse width is generated through the SerDes block. In the case where a code of 11111 is selected, a 10 ns pulse signal is generated. Data out with a high clock (DOHC) signal is selected for the 2 ns/4 ns/6 ns/8 ns/10 ns pulse widths with a 2 ns resolution. The SerDes block is parallel in the serial out (PISO). The SerDes has a single shift register that receives the DOLC and zeros the signal once per LC; this shifts the DOLC and zeros out at the HC clock rate. Table II shows the interface signal of the UWB digital pulse generator.

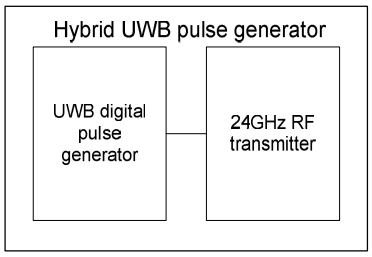


Fig. 2. Block diagram of the hybrid UWB pulse generator.

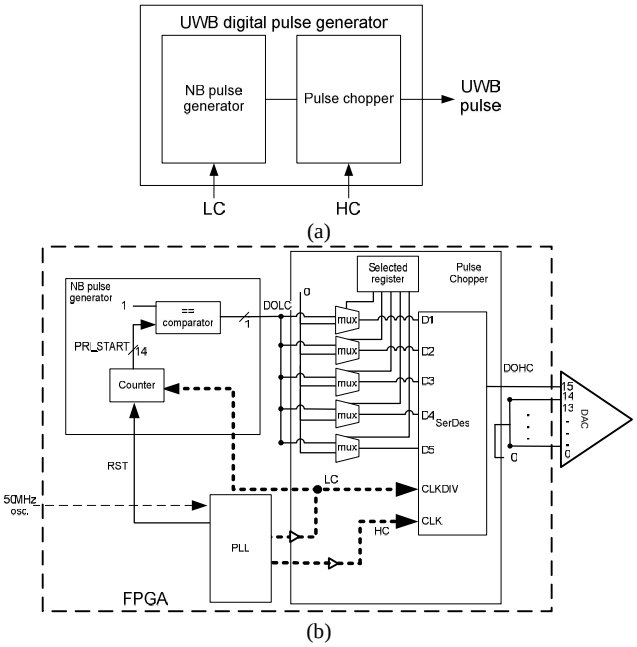


Fig. 3. Block diagram of the hybrid UWB pulse generator: (a) block diagram of the UWB digital pulse generator; (b) specific diagram of the UWB digital pulse generator.

TABLE II. NAMES AND DEFINITIONS IN THE UWB DIGITAL PULSE GENERATOR.

Name	Definition
LC/HC	Clock signals of the PLL block to convert the 50 MHz external clock into a 100 MHz clock and a 500 MHz clock
RST	Reset signal to control the NBPG block
RST DOLC	RST Data output signal at which the NBPG block generates a pulse signal with a 10 ns pulse width on every PRI
RST DOHC	RST PG data output signal generated by the SerDes blocks of a 2 ns/4 ns/6 ns/8 ns/10 ns pulse width

Figure 4 shows the timing diagram of the digital pulse generator in the case of variable pulse width on the FPGA. The FPGA transmits the DOHC signal using the SerDes block and the PLL block. The NBPG block uses the counter block to determine the PRI using the LC clock signal. The counter

block acts as the counter during the PRI.

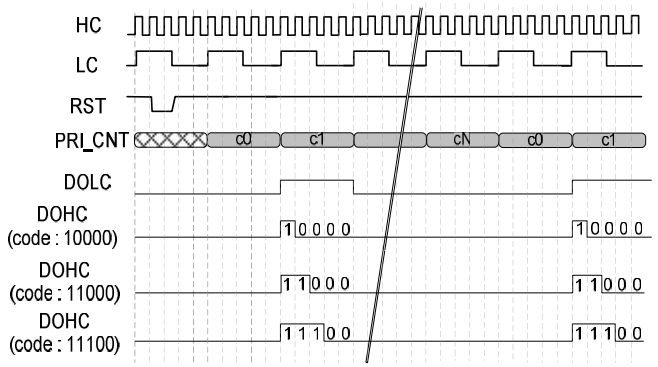


Fig. 4. Timing diagram of the hybrid UWB pulse generator, according to the selected register block code.

When the counter reaches zero, the DOLC signal is generated as a one signal on the next clock of the zero counter and a zero signal on the other counter number during PRI. As the NBPG block generates the DOLC signal, the SerDes block transmits the 2 ns pulse signal using the parallel-to-serial converter through the DAC module.

C. UWB RF Transmitter

To apply the UWB digital pulse generator to the 24 GHz center frequency, we develop a homodyne 24 GHz RF transmitter. Using a digital-analog converter (DAC), a digital pulse signal with a 2 ns signal width is generated in the intermediate frequency (IF). Next, to produce the UWB pulse signal with a 24 GHz center frequency, the digital pulse signal is mixed with a 24 GHz oscillator and is passed to a 24 GHz LNA and antenna. The tapered slot antenna used in the 24 GHz RF system has been widely used in wideband applications due to its low profile, low weight, easy fabrication, broad bandwidth, relatively high gain, and symmetrical E-and H-plane beam patterns [13]. The substrate for the antenna implementation is a Rogers RO4003 ($£_r$ =3.38), with a 20 mm thickness. It provides a 36 degree, 3 dB beamwidth in the E-plane and a 42 degree beamwidth in the H-plane at 24 GHz. Finally, the UWB impulse generator sends out a 2 ns pulse train at a 10 KHz rate, which is modulated by a 24 GHz LO signal through the mixer.

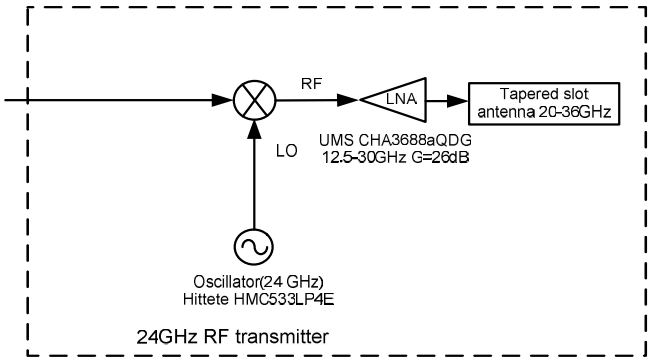


Fig. 5. Block diagram of the developed 24 GHz RF transmitter.

Figure 5 provides a block diagram of the developed 24 GHz RF transmitter. Table III summarizes the performance of our developed 24 GHz RF transmitter. Table IV shows the specifications of the important components used in the developed 24 GHz RF transmitter. The operating frequency and bandwidth are 24 GHz and 1 GHz, respectively. In the UWB RF transmitter, the gain, output LO leakage and input 1 dB compression point (P1 dB) are 10 dB, -5 dBm, and +4 dBm, respectively.

TABLE III. SUMMARY OF THE PERFORMANCE OF THE DEVELOPED 24 GHZ RF TRANSMITTER.

Transmitter	
LC/HC Gain	10 dB
LO leakage	-5 dBm
Input P1 dB	+4 dBm

TABLE IV. SPECIFICATIONS OF THE COMPONENTS USED IN THE DEVELOPED 24 GHZ RF TRANSMITTER.

Component	**Specification**
Oscillator (HMC533LP4E)	Frequency Range: 23.8 - 24.8 GHz Power output: +12 dBm
LNA (CHA3688QDG)	P1 dB: +15 dBm Gain: 16 dB Noise figure: 2.1 dB
Tapered slot antenna	E-plane: 36 degree (3 dB-beamwidth) @ 24 GHz H-plane: 42 degree (3 dB-beamwidth) @ 24 GHz

III. IMPLEMENTATION OF THE HYBRID UWB PULSE GENERATOR AND THE MEASURED RESULTS

We evaluate the performance of the hybrid UWB pulse generator for a 24 GHz UWB pulse-Doppler radar by combining a digital pulse and a 24 GHz RF transmitter. To evaluate the performance of the proposed digital pulse generator, an FPGA-based evaluation platform, including an AD9779 DAC module with a 1 G samples per second maximum sampling rate is developed. Figure 6 provides a functional block diagram of the digital impulse generator (Fig. 6(a)), a top-view image of the digital pulse generator (Fig. 6(b)) and the developed 24 GHz RF transmitter (Fig. 6(c)). In this work, the digital pulse generator is coded in a hardware description language using only the available standard logic elements. The digital pulse generator requires only 4 % of the memory block, 1 % of the Slice LUTs, and 1 % of the Slice registers on the Xilinx (Virtex-5 lx50). Table V shows the hardware resources of the digital pulse generator.

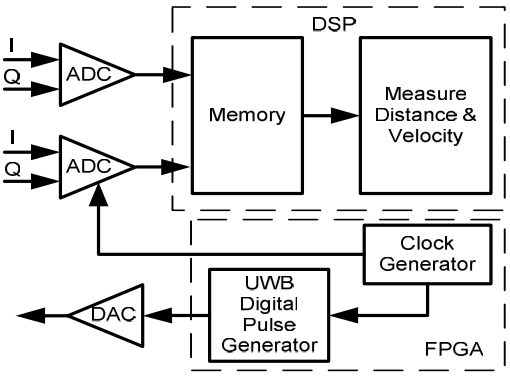
TABLE V. HARDWARE RESOURCES OF THE DIGITAL PULSE GENERATOR.

Parameter	**Proposed architecture**
Operating frequency	347.8 MHz
Number of Slice Registers	18
Number of Slice LUTs	42

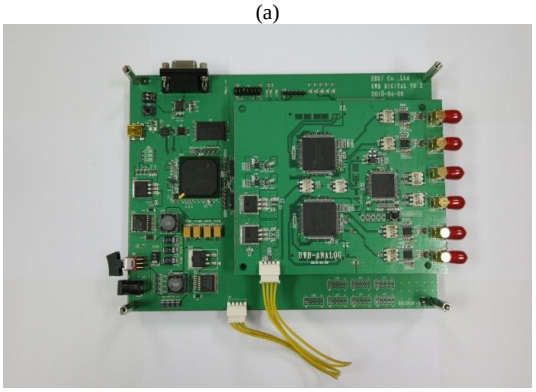
Figure 7 shows the measurement environments of the hybrid UWB pulse generator. We use a Tektronix TDS5104B oscilloscope with a 3 dB bandwidth at 1 GHz for the analysis of the IF and an Agilent E4448A spectrum analyser with a 50 GHz spectrum for the analysis of the RF.

Figure 8 shows the measured digital impulse signal of a 2 ns pulse width and 0.5 Vp-p in the time domain. The top image shows the 1 μs PRI; the bottom image shows the 2 ns

pulse width.



(a)



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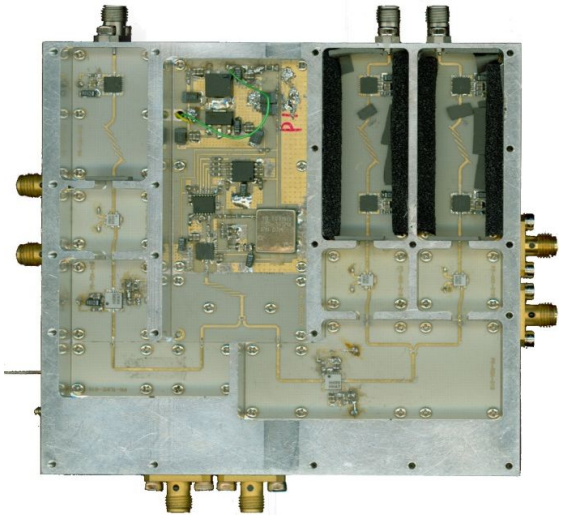

(c)

Fig. 6. Evaluation platform developed to verify the performance of our developed hybrid pulse generator: (a) functional block diagram of the digital pulse generator, (b) top-view image of the digital impulse generator; ADC, DAC, DSP and FPGA, (c) the developed 24 GHz RF transmitter

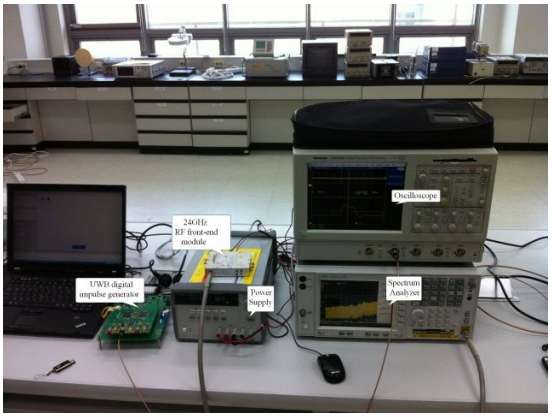

Fig. 7. Measurement environment of the hybrid UWB pulse generator.

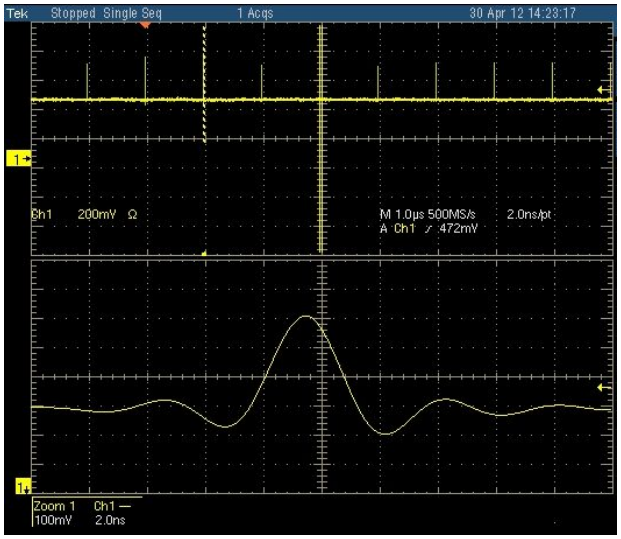

Fig. 8. Measured pulse signal with a 2 ns pulse width and a 0.5 Vp-p.

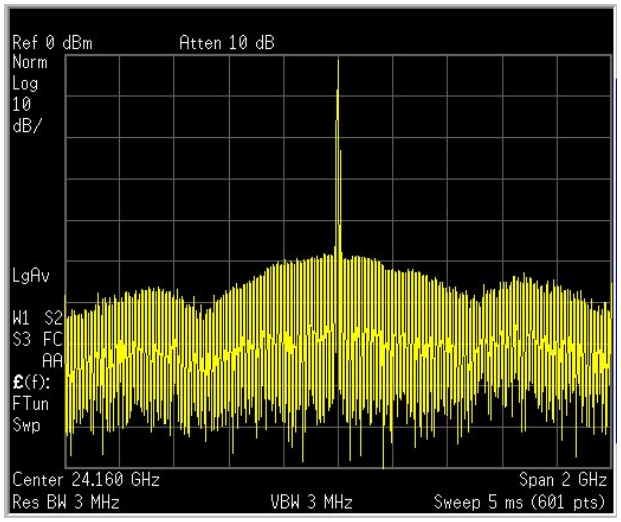

Fig. 9. Spectrum of the hybrid UWB pulse generator with a 500 MHz bandwidth at a 24 GHz centre frequency.

We evaluate the spectrum results from 23 GHz to 25 GHz in the RF. Figure 9 shows the spectrum characteristics of the hybrid UWB pulse generator at a 24 GHz centre frequency. Because the pulse generator has a 2 ns pulse width, the spectrum of the pulse generator has a 500 MHz bandwidth and 24 GHz centre frequency, as shown in Fig. 9.

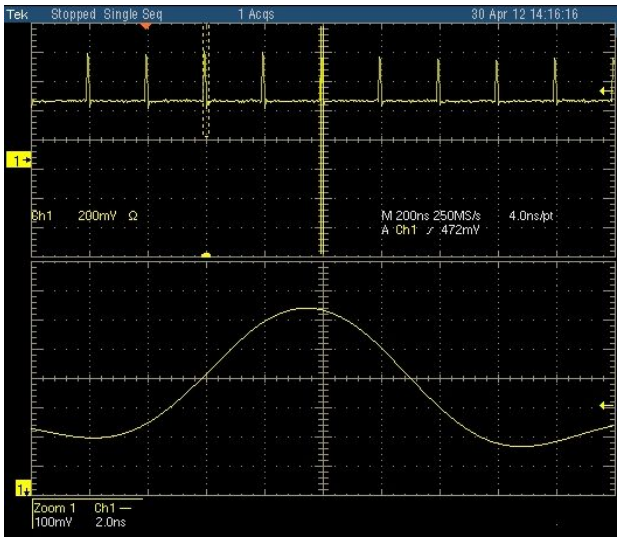

Fig. 10. Measured impulse signal with an 8 ns pulse width and a 0.5 Vp-p.

To evaluate the variable pulse width, we change the code parameters of the selected register block. In this section, we only evaluate the 8 ns pulse signal of the 200 ns PRI. Fig. 10 shows the measured digital pulse signal with an 8 ns pulse width and a 0.5 Vp-p in the time domain. The top image shows the 200 ns PRI; the bottom image shows the 8 ns pulse width. Figure 11 shows the spectrum characteristics of the hybrid UWB pulse generator with a 125 MHz bandwidth at a 24 GHz centre frequency. Because the pulse generator has an 8 ns pulse width, the spectrum of the pulse generator has a 125 MHz bandwidth, as shown in Fig. 11.

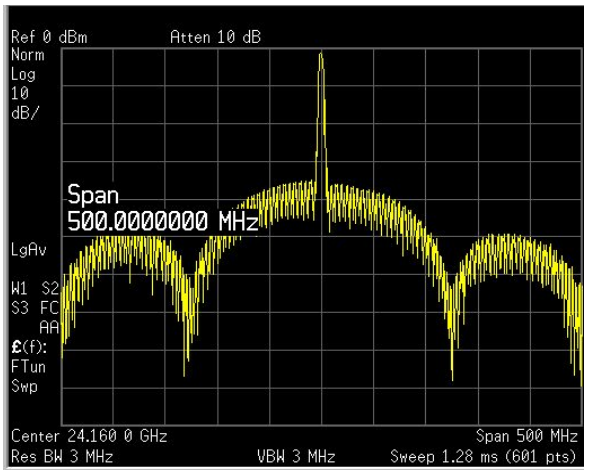

Fig. 11. Spectrum of the hybrid UWB pulse generator with a 125 MHz bandwidth at a 24 GHz centre frequency.

IV. CONCLUSIONS

In this paper, we presented and demonstrated the design of a hybrid UWB pulse generator with a variable pulse width and PRI for UWB pulse-Doppler radar. Conventional analog High Frequency (HF)-based pulse generators were less tunable for pulse width and PRI and show reduced variation according to temperature. Conventional CMOS-based pulse generators have received much attention for single chip applications. However, because the flexibility of conventional CMOS pulse generators has decreased, these devices have limitations for various applications. In contrast, FPGA-based pulse generators have great flexibility. However, due to the critical path of the FPGA, FPGA-based digital pulse generators yield a broadened pulse width and a narrow bandwidth. To avoid this problem, we used an NB pulse generator with an LC and a pulse chopping technique with HC based on a SerDes block. To improve the flexibility, this paper proposed a hybrid UWB pulse generator with a wave design. For the first time, a digital pulse generator was developed by combining an NB pulse generator and a pulse chopper based on a SerDes block. Using a 24 GHz RF transmitter, we demonstrated the feasibility of the hybrid UWB pulse generator. Finally, we designed a hybrid UWB pulse generator that supports variable pulse width and PRI for UWB radar. We expect that the proposed hybrid UWB pulse generator will be adopted for application in UWB radar systems.

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