Integer- and Fractional-Order VCO Using Non-Inertial Amplitude Stabilization and Modern Active Elements

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Abstract—This paper introduces design of the linearly tunable quadrature voltage-controlled oscillator (VCO) using modern off-the-shelf active elements suitable for the design of electronically adjustable applications. The simplified topology was achieved using non-inertial stabilization of amplitude. It allows targeting adjustability of the oscillation frequency only into lossless integrator part of the topology. This arrangement simplifies the design and the tenability also. Derived symbolical expressions indicate that gain adjustment of used amplifiers (that are still in single path) does not influence amplitude and phase shift ratio of generated waveforms, which is a beneficial feature. The performances of the circuit are tested experimentally in band of units of MHz and results confirmed expected behavior. Initial study of the oscillator with fractional-order capacitors is presented and discussed. Results are supported by laboratory measurements.

Index Terms—Diamond transistors; Electronic adjusting; Fractional-order; Modern active devices; Quadrature output; Tuning; Voltage controlled oscillator; Voltage-mode multipliers.

I. INTRODUCTION

Professional designers of electronic components and applications utilize various standard elements for their designs. Omitting the well-known devices, such as operational amplifier, the knowledge and awareness of practicians about many recently introduced active devices [1], [2] are usually limited. However, these devices allow interesting features suitable for circuit synthesis and parametric adjustment in applications in comparison to standard operational amplifiers. Our paper targets on synthesis of quite simple oscillator generating quadrature output waveforms with special off-the-shelf active elements.

These elements are used because of beneficial features of final application as described later.

Many designed topologies employ beneficially applicable components (e.g., highly linear and electronically controllable). However, some of them are featured as obsolete [3], [4]. Therefore, search for implementations expecting similar quality and tunable features based on novel commercially available elements is worth deeper research. The features of the newly proposed topology are: a) voltage driven linear adjustment of oscillation frequency, b) non-inertial wideband amplitude stabilization, c) grounded capacitors, d) simple principle using single loop for feedback and single loop for stabilization in comparison with previous concepts, e.g., [5], e) electronic adjustability implemented in lossless integrator only [3]–[7]. Moreover, the topology targets on employment of passive elements as core of lossy integrator in comparison to, e.g., [5], where both integrators are lossless. Standard solution of the oscillator includes amplitude gain control circuit (AGC) for amplitude stabilization also [3]–[9]. However, there are several ways of stabilization and they have different features (inertial: peak detection, integration, differential error amplifier controlling some parameter influencing condition for oscillation [3], [4], [6]; non-inertial: limiters [5], [10], opto-couplers [7], [8], and nonlinearities of active element itself [11]–[14]). Please note that some from active elements used in literature are just hypothetical and unavailable commercially [11]–[14]. The non-inertial stabilization is much simpler, but still sufficient for radio-communication applications as, e.g., voltage-controlled oscillator (VCO), especially when compared with slowly reacting inertial AGC [10]. However, distortion of output waveforms is expected to be higher [15].

II. PROPOSED TOPOLOGY OF VCO

The newly designed structure of the oscillator includes standard building blocks typical for single loop systems (lossy and lossless integrator) (see Fig. 1). Note that the

topology is general, particular features of partial blocks (inverting/non-inverting transfers) are discussed later. The lossy integrator should be designed as simple as possible because adjustability of the frequency of oscillation (FO) is not implemented in this part. Figure 2 shows the complete circuitry of the quadrature oscillator. The time constant τ_1 is not changed during the tuning process even in case of linear adjustment of FO. This is significant feature of this topology. The oscillator in Fig. 2 consists of special active elements, such as differential voltage buffer (DVB) [4] suitable for operation of voltage subtraction and sum ($V_{out} = V_+ - V_-$), so-called "diamond transistors" (DT) [1], [2], [10] behaving as current conveyor ($I_C = I_E$, $I_B = 0$, $V_B = V_E$) or voltage to current converter, and voltage-mode multipliers (MLTs) performing $V_{out} = (V_{x1} - V_{x2}) \times (V_{y1} - V_{y2}) \times k$, where k is constant given by the internal design of the particular MLT element. Multipliers bring significant advantages to the topology because of their simple electronic tuning by DC voltage as shown later.

The general topology in Fig. 1 can be analysed easily by signal flow graph approach (similarly to [5]), and resulting characteristic equation has the following form

$$\Delta = 1 - (L_1 + L_2) = 1 + H_1(s) \times H_2(s) - H_2(s) \times F = 0, \quad (1)$$

where L_1 and L_2 are loops of the topology and $H_1(s)$, $H_2(s)$, and F are partial transfers of branches (integrators and feedback amplifier/limiter). In fact, the feedback path of amplifier/limiter represents only closed loop of the band-pass transfer response [5], [10]. These partial transfers have the following symbolical representations:

$$H_1(s) = \frac{1}{s \times \tau_1} = \frac{A_1 A_2}{s C_1 R_1}, \quad (2)$$

$$H_2(s) = \frac{1}{1 + s \times \tau_2} = \frac{1}{1 + s C_2 R_2}, \quad (3)$$

$$F \cong \frac{R_4}{R_3}\bigg|_{V_{C1,2} \leq V_{th\_D1,2}}, \quad otherwise \quad F < \frac{R_4}{R_3}\bigg|_{V_{C1,2} > V_{th\_D1,2}}, \quad (4)$$

where A_1, A_2 are adjustable voltage gains created by MLTs controlling $\tau_1 = C_1 R_1 / (A_1 A_2)$. It means that both gains can reduce time constant of loss-less integrator. The condition for transfer F is valid for voltages below threshold voltage of diodes ($V_{th\_D1,2}$). Therefore, the amplitudes of $V_{C1,2}$ nodal voltages above $V_{th\_D1,2}$ have intentional limitation too. The feedback transfer of the limiting amplifier based on diamond transistor DT_2, R_3, R_4, and antiparallel connection of diodes $D_{1,2}$ ensures stabilization of amplitude level independent on inertial behavior because no AGC with peak detector and capacitors is used. On the other hand, the non-inertial AGC brings increased level of total harmonic distortion as already mentioned above.

When partial transfers (2)–(4) are inserted into (1), particular characteristic equation valid for circuit from Fig. 2 is obtained

$$s^2 + \frac{R_3 - R_4}{C_2 R_2 R_3} s + \frac{A_1 A_2}{R_1 R_2 C_1 C_2} = 0. \quad (5)$$

FO can be expressed as

$$\omega_0 = \sqrt{\frac{A_1 A_2}{R_1 R_2 C_1 C_2}}, \quad (6)$$

and condition for oscillation (CO) can be expressed as

$$R_4 \geq R_3. \quad (7)$$

The value of gain in the loop of limiting amplifier can be adjusted by R_4 to proper level. The voltage relation between output nodes V_{C1} and V_{C2} is expressed as

$$\frac{V_{C1}}{V_{C2}} = \frac{A_1}{s C_1 R_1}\bigg|_{\omega = \omega_0} = -j \sqrt{\frac{A_1 R_2 C_2}{A_2 R_1 C_1}}, \quad (8)$$

that confirms quadrature phase shift (90°) between generated waveforms and its immunity to FO tuning by $A_{1,2}$ given by the design when $A_1 = A_2 = A$ is ensured (as well as by $R_1 = R_2 = R$ and $C_1 = C_2 = C$). The amplitudes of output waveforms are then also independent on the tuning process.
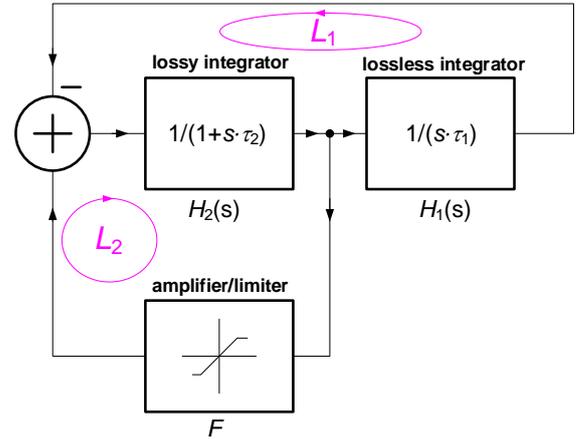

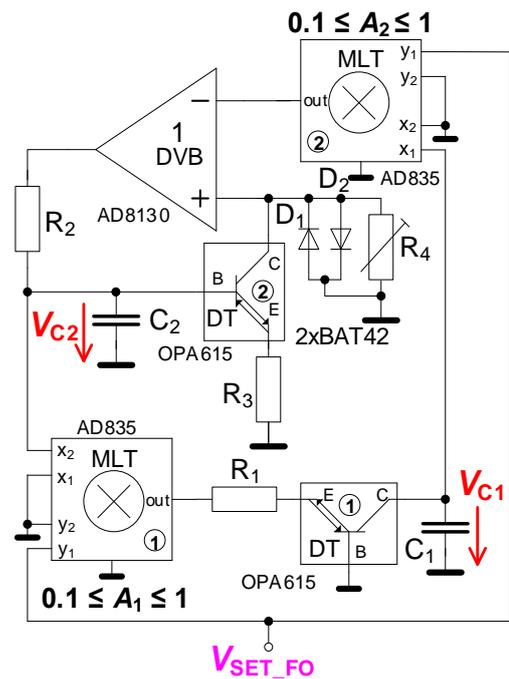Fig. 1. Block concept used for the oscillator design.

Fig. 2. Complete topology of newly proposed quadrature oscillator (VCO).

III. DESCRIPTION OF EXPERIMENTS

Two multipliers designated as AD835 are actually used as variable gain amplifiers in topology shown in Fig. 2. Their gain (considering particular interconnections in Fig. 2) can be expressed as $A_{1,2} \cong V_{SET\_A1,2}$. The linear tuning of the FO requires simultaneous driving of $A_{1,2}$ ($A_1 = A_2 = A$). This can be managed very simply by interconnection of driving terminals of MLTs to the single node marked as V_{SET_FO}. This design employs two OPA615 diamond transistors, AD8130 differential voltage buffer, and two BAT42 Schottky diodes (with $V_{th\_D} \cong 200$ to 400 mV).

Adjustability of V_{SET_FO} is limited by linearity of MLTs (AD835). Therefore, range of 0.1 V $\leq V_{SET\_FO} \leq 1$ V (and $0.1 \leq A_{1,2} \leq 1$) is considered. Our design deals with expected frequency range from 0.6 MHz up to 6 MHz. This is fulfilled by selection of $R_1 = R_2 = 180\,\Omega$ and $C_1 = C_2 = 150$ pF. Values used in stabilizing path (amplifier/limiter) were chosen as follows: $R_3 = 220\,\Omega$ and $R_4 = 1$ kΩ, value of R_4 should be adjustable (e.g., trimmer). The theoretical FO range yields 0.578 MHz $\rightarrow 5.898$ MHz. Experimentally gained dependence of FO on V_{SET_FO} driving voltage is shown in Fig. 3. The measured range of tunability starts from 0.80 MHz and ends at 6.291 MHz. The output levels reach voltage between 0.22 V$_{p-p}$ and 0.43 V$_{p-p}$ in this wide range of FO tuning as shown in Fig. 4.
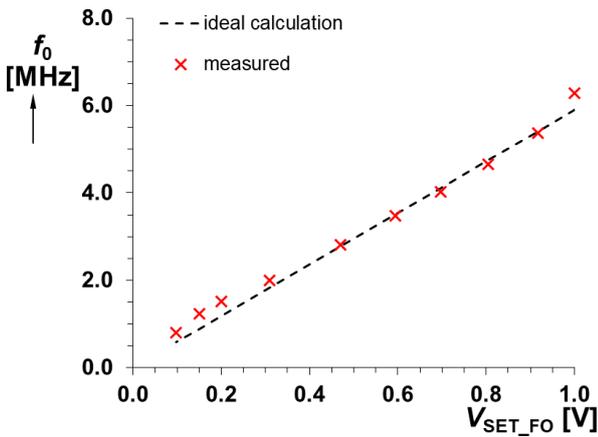

Fig. 3. Comparison of measured and calculated dependences of FO on the V_{SET_FO} driving voltage.
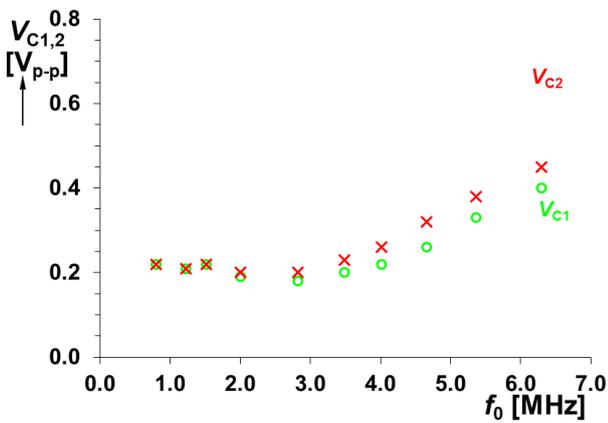

Fig. 4. Dependence of $V_{C1,2}$ on FO (measured results).

The total harmonic distortion (THD) fluctuates between

0.8 % and 4.5% (Fig. 5). These higher values of THD are probably unsuitable for audio electronics, but sufficient for communication systems. Note that THD in units of percent is expected for non-inertial amplitude stabilization based directly on intentional nonlinearity. Phase shift between V_{C1} and V_{C2} voltages can be found between $90\,°$ and $98\,°$ (Fig. 6). The deviation (9 %) at the highest observed FO is given by increased deviation of phase responses of active devices themselves in these bands, especially in case of AD835 and AD8130. Exemplary results for $V_{SET\_FO} = 0.47$ V ($f_0 = 2.817$ MHz) in time domain are shown in Fig. 7, and the spectral analysis of these waveforms is shown in Fig. 8. Power consumption reaches 700 mW (5 V$/70$ mA power supply per supply branch). Spectrum analyzer HP4395A and oscilloscope RIGOL DS1204B have been used for discussed analyses.
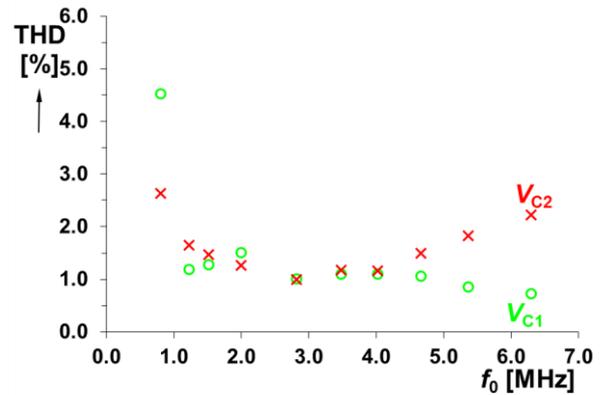

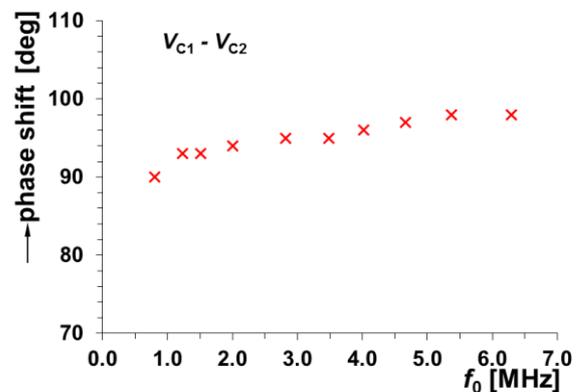Fig. 5. Dependence of THD on FO tuning (measured results).

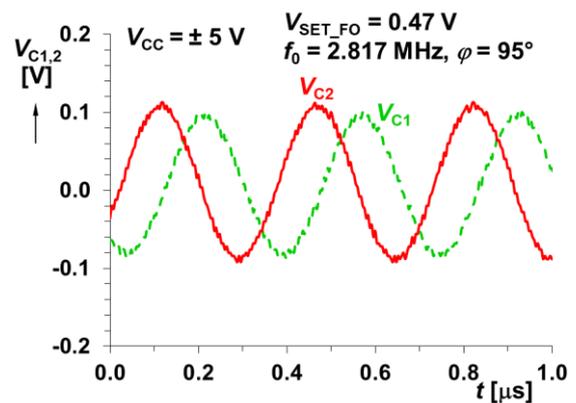Fig. 6. Dependence of phase shift on FO tuning (measured results).

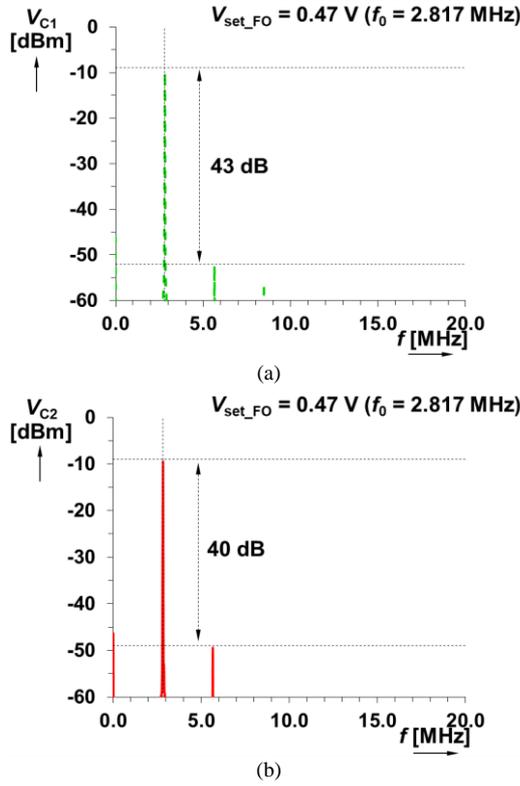Fig. 7. Examples of output responses in time domain (measured results).

(a)

(b)

Fig. 8. Spectrum of analysed signals in case of particular setting shown in Fig. 7 and for the case of: a) V_{C1}; b) V_{C2} (measured results).

IV. MODIFICATION FOR FRACTIONAL-ORDER OPERATION

Phase shifts available in standard integer-order approaches are not sufficient for many design cases. The fractional-order approach [16] offers interesting features in the field of an arbitrary phase shift generation between output signals [17], [18]. The implementation of two identical fractional-order capacitors (constant phase elements - CPEs) [19], [20] of α order in our topology instead of integer-order $C_{1,2}$ capacitors is the simplest solution in our case. Supposing identical order of both CPEs (α), the characteristic equation (5) modifies to the following form

$$s^{2\alpha} + \frac{R_3 - R_4}{C_\alpha R_2 R_3} s^\alpha + \frac{A_1 A_2}{R_1 R_2 C_\alpha^2} = 0 \qquad (9)$$

that includes real and imaginary part as follows, respectively:

$$\omega_0^{2\alpha} \cos(\pi\alpha) + \omega_0^\alpha \cos\left(\frac{\pi}{2}\alpha\right)\left(\frac{R_3 - R_4}{C_2 R_2 R_3}\right) + \frac{A_1 A_2}{R_1 R_2 C_\alpha^2} = 0, \ (10)$$

$$\left(\frac{R_3 - R_4}{C_\alpha R_2 R_3}\right) = -\omega_0^\alpha \frac{\sin(\pi\alpha)}{\sin\left(\frac{\pi}{2}\alpha\right)}. \qquad (11)$$

Generation of multiples of 45 ° in the oscillator presented in Fig. 2 can be chosen as a particular example of design. The following particular values were used: $R_1 = R_2 = R = 180 \ \Omega$, $R_3 = 1 \ k\Omega$, $C_1 = C_2 = C_\alpha = 56 \ \mu F/sec^{1/2}$ having order $\alpha = 0.5$, $A_1 = A_2 = A$, and $f_0 = 1 \ kHz$. The resulting equations for the design can be rewritten as follows

$$R_4 = R_3 \left[1 + \frac{\omega_0^\alpha RC_\alpha \sin(\pi\alpha)}{\sin\left(\frac{\pi}{2}\alpha\right)} \right], \qquad (12)$$

$$A = \omega_0^\alpha RC_\alpha. \qquad (13)$$

Equation describing the oscillation frequency can be obtained from (13)

$$\omega_0 = \left(\frac{A}{RC_\alpha}\right)^{\frac{1}{\alpha}}. \qquad (14)$$

The amplitude relation between voltage outputs (nodes with fractional-order capacitors) has a very simple form

$$\frac{V_{C1}}{V_{C2}} = \frac{A}{s^\alpha C_\alpha R}\bigg|_{\substack{A_1 = A_2 = A \\ R_1 = R_2 = R \\ \omega = \omega_0}} = \frac{1}{j^\alpha} \qquad (15)$$

that gives the resulting phase shift, such as follows

$$\frac{1}{j^\alpha} \Rightarrow \varphi_{12} = \frac{\pi}{2}\alpha. \qquad (16)$$

When $\alpha = 0.5$, the intended value of phase shift equal to 45 ° is obtained (absolute value).

It is clear that R_4 and A depends on the order of CPE, as well as on the frequency of oscillation. It is a typical issue of these implementations of the fractional-order elements. However, when R_4 will be adjusted in order to follow f_0 tuning changes caused by A, the amplitude stabilization system may keep CO fulfilled when oscillator is tuned. Substitution of real parameters to both formulas (12) and (13) yields $R_4 = 2.13 \ k\Omega$ and $A = 0.8$ ($V_{set\_FO} = 0.8 \ V$). The experiment was performed using discussed parameters in topology of the oscillator shown in Fig. 2 and capacitors replaced by the fractional-order capacitors. The example of results in time domain is shown in Fig. 9. Particular setting leads to the value of frequency of oscillation equal to 1.254 kHz and 46 phase shift between output voltages. The CPE used as a replacement of fractional-order capacitors was based on the design described in [21]–[23], and its particular setting is shown in Fig. 10.
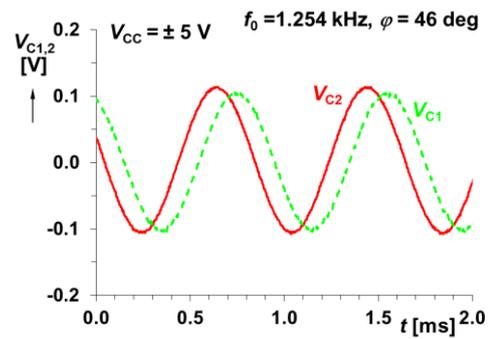

Fig. 9. Measured example of time domain waveforms for fractional-order example (CPEs having $\alpha = 0.5$, $C_\alpha = 56 \ \mu F/sec^{1/2}$ implemented in the design).
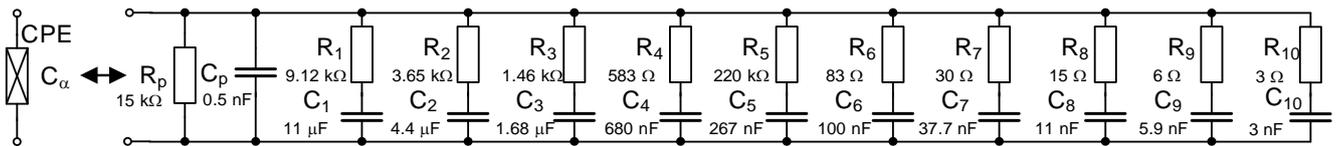
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Fig. 10. The RC realization of CPE ($\alpha = 0.5$, $C_\alpha = 56$ μF/sec$^{1/2}$) used in oscillator as replacement of C_α.

V. Conclusions

It was demonstrated that whole electronic adjustability of the oscillator (there are two amplifiers with A_1, A_2 gains) can be placed into lossless integrator without any effect on generated signals (amplitude and phase ratio) when simultaneous control of their gain is preserved. Non-traditional active elements with attractive features were used for experimental verification of the design targeting the units of MHz (tested between 0.8 MHz and 6.29 MHz). The slightly higher level of THD is typical for these designs using non-inertial AGC. It is caused by AGC nonlinearity itself, as well as by real features of active elements (especially, AD835) due to higher signal levels. Results also indicate phase shift with acceptable variation (up to 9 %) given by impact of real phase responses of the active parts (AD8130), as well as parasitic features of prepared printed circuit board. However, these results are sufficient for medium wave application of the oscillator in several systems (carrier generation in super-heterodyne receivers, carrier source for IQ modulation with low number of states, etc. - THD is less important parameter in cases of radio-communication systems; some RF VCOs are not providing pure harmonic signal [15]). It is given by the simplicity of the final circuit that is a key feature of this design with uncommon topology.

The operation of the presented oscillator with fractional-order elements replacing standard capacitors was verified also. Results confirmed the intended 45 ° phase shift between generated waveforms. This particular topology seems to be promising for both integer-order and fractional-order electronically tunable applications when compared with typical examples known from recent works including only non-adjustable active elements [17], [18], [23]. The number of used CPEs depends on a number of required particular values of phase shifts [17], [18]. Note that standard and very important parameters are frequently not studied in sufficient detail in common practice. Features, such as relation between generated output signals, their mutual phase shift, amplitude ratios, and dependence of these parameters on the tuning procedure, should be analysed carefully, and it is a goal of our future research for solutions addressing these aspects.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

References

[1] D. Biolek, R. Senani, V. Biolkova, and Z. Kolka, "Active elements for analog signal processing: Classification, review and new proposals", *Radioengineering*, vol. 17, no. 4, pp. 15–32, 2008.

[2] R. Senani, D. R. Bhaskar, and A. K. Singh, *Current Conveyors: Variants, Applications and Hardware Implementations*. Switzerland, Springer International Publishing, 2015.

[3] R. Senani, D. R. Bhaskar, V. K. Singh, and R. K. Sharma, *Sinusoidal Oscillators and Waveform Generators using Modern Electronic Circuit Building Blocks*. Switzerland, Springer International Publishing, 2016. DOI: 10.1007/978-3-319-23712-1.

[4] R. Sotner, J. Jerabek, N. Herencsar, and J. Petrzela, "Methods for extended tunability in quadrature oscillators based on enhanced electronic control of time constants", *IEEE Transactions on Instrumentation and Measurement*, vol. 67, no. 6, pp. 1495–1505, 2018. DOI: 10.1109/TIM.2018.2799058.

[5] J. Bajer, J. Vavra, D. Biolek, and K. Hajek, "Low-distortion current-mode quadrature oscillator for low-voltage low-power applications with non-linear non-inertial automatic gain control", *In proc. of 20th European Conference on Circuit Theory and Design (ECCTD)*, 2011, pp. 441–444. DOI: 10.1109/ECCTD.2011.6043381.

[6] A. Rodriguez-Vazquez, B. Linares-Barranco, J. Huertas, and E. Sanchez-Sinencio, "On the design of voltage-controlled sinusoidal oscillators using OTA's", *IEEE Transactions on Circuits and Systems*, vol. 37, no. 2, pp. 198–211, 1990. DOI: 10.1109/31.45712.

[7] D. Biolek, A. Lahiri, W. Jaikla, M. Siripruchyanun, and J. Bajer, "Realization of electronically tunable voltage-mode/current-mode quadrature sinusoidal oscillator using ZC-CG-CDBA", *Microelectronics Journal*, vol. 42, no. 10, pp. 1116–1123, 2011. DOI: 10.1016/j.mejo.2011.07.004.

[8] V. Biolkova, J. Bajer, and D. Biolek, "Four-phase oscillators employing two active elements", *Radioengineering*, vol. 20, no. 1, pp. 334–339, 2011.

[9] R. Sotner, J. Jerabek, L. Langhammer, and J. Dvorak, "Design and analysis of CCII-based oscillator with amplitude stabilization employing optocouplers for linear voltage control of the output frequency", *Electronics (MDPI)*, vol. 7, no. 9, pp. 1–20, 2018. DOI: 10.3390/electronics7090157.

[10] J. Jerabek, R. Sotner, N. Herencsar, and A. Kartci, "Importance of amplitude stability and spectral purity of produced signals in a quadrature oscillator", *In proc. of 16th International Conference on Computer as a Tool (EUROCON)*, 2015, pp. 351–355. DOI: 10.1109/EUROCON.2015.7313770.

[11] S. Summart, C. Thongsopa, and W. Jaikla, "OTA based current-mode sinusoidal quadrature oscillator with non-interactive control", *Przeglad Electrotechniczny*, vol. 88, no. 7a, pp. 14–17, 2012.

[12] A. Jantakun and W. Jaikla, "Current-mode quadrature oscillator based on CCCDTAs with noninteractive dual-current control for both condition of oscillation and frequency of oscillation", *Turkish Journal of Electrical Engineering and Computer Sciences*, vol. 21, no. 1, pp. 81–89, 2013. DOI: 10.3906/elk-1106-2.

[13] H. P. Chen, "Electronically tunable quadrature oscillator using grounded components with current and voltage outputs", *Scientific World Journal*, vol. 2014, pp. 1–8, 2014. DOI: 10.1155/2014/572165.

[14] S. Tuntrakool, M. Kumngern, R. Sotner, N. Herencsar, P. Suwanjan, and W. Jaikla, "High input impedance voltage-mode universal filter and its modification as quadrature oscillator using VDDDAs", *Indian Journal of Pure and Applied Physics*, vol. 55, no. 5, pp. 324–332, 2017.

[15] M. Daliri and M. Maymandi-Nejad, "Analytical model for CMOS cross-coupler LC-tank oscillator", *IET Circuits, Devices and Systems*, vol. 8, no. 1, pp. 1–9, 2014. DOI: 10.1049/iet-cds.2013.0087.

[16] A. S. Elwakil, "Fractional-order circuits and systems: An emerging interdisciplinary research area", *IEEE Circuits and Systems Magazine*, vol. 10, no. 4, pp. 40–50, 2010. DOI: 10.1109/MCAS.2010.938637.

[17] M. Fouda, A. Soltan, A. G. Radwan, and A. M. Soliman, "Fractional-order multi-phase oscillators design and analysis suitable for higher-order PSK applications", *Analog Integrated Circuits and Signal Processing*, vol. 87, no. 2, pp. 301–312, 2016. DOI: 10.1007/s10470-016-0716-2.

[18] L. A. Said, A. G. Radwan, A. H. Madian, and A. M. Soliman, "Three fractional-order-capacitors-based oscillators with controllable phase and frequency", *Journal of Circuits, Systems and Computers*, vol. 26,

no. 10, pp. 1750160–1750178, 2017. DOI: 10.1142/S0218126617501602.

[19] J. Valsa, P. Dvorak, and M. Friedl, "Network model of CPE", *Radioengineering*, vol. 20, no. 3, pp. 619–626, 2011.

[20] J. Valsa and J. Vlach, "RC models of a constant phase element", *Int. Journal of Circuit Theory and Applications*, vol. 41, no. 1, pp. 59–67, 2013. DOI: 10.1002/cta.785.

[21] O. Domansky, R. Sotner, L. Langhammer, J. Jerabek, C. Psychalinos, and G. Tsirimokou, "Practical design of RC approximants of constant phase elements and their implementation in fractional-order PID regulators using CMOS voltage differencing current conveyors", *Circuits, Systems, and Signal Processing*, vol. 38, no. 4, pp. 1520–1546, 2019. DOI: 10.1007/s00034-018-0944-z.

[22] R. Sotner, J. Jerabek, A. Kartci, O. Domansky, N. Herencsar, V. Kledrowetz, B. B. Alagoz, and C. Yeroglu, "Electronically reconfigurable two-path fractional-order PI/D controller employing constant phase blocks based on bilinear segments using CMOS modified current differencing unit", *Microelectronics Journal*, vol. 86, no. 4, pp. 114–129, 2019. DOI: 10.1016/j.mejo.2019.03.003.

[23] L. A. Said, A. G. Radwan, A. H. Madian, and A. M. Soliman, "Fractional order oscillators based on operational transresistance amplifiers", *AEU - International Journal of Electronics and Communications*, vol. 69, no. 7, pp. 988–1003, 2015. DOI: 10.1016/j.aeue.2015.03.003.