A Lossy Capacitance Measurement Circuit Based on Analog Lock-in Detection

Mehmet Demirtas[1, *], Mehmet Akif Erismis[1], Salih Gunes[2]

[1]*Department of Electrical and Electronics Engineering, Necmettin Erbakan University,*
42140 Konya, Turkey
[2]*Department of Electrical and Electronics Engineering, Konya Technical University,*
42250 Konya, Turkey
mdemirtas@erbakan.edu.tr

Abstract—**This paper presents a lossy capacitance measuring circuit which is based on analog lock-in detection technique. Lossy capacitance can be modelled as a pure capacitor connected in parallel with a resistor. The measurement circuit mechanism consists of an excitation signal to drive the lossy capacitance, a transimpedance amplifier to produce a voltage, and a lock-in detection circuit to extract lossy values of capacitance. The lock-in detector multiplies its input with a square wave using switches and filters out high frequencies to give a DC output that is actually in proportional to the measured values. A field programmable gate array is employed to generate direct digital synthesis based sinusoidal excitation signal to generate reference signals required for demodulation and to measure the output of lock-in detection. The phase shift between the excitation signal and reference signals is controlled accurately in digital domain. Thus, due to the phase mismatch, errors are properly reduced. Also, analog phase shifter and analog switch-driving circuits are no longer required. Three different lossy capacitors realized using discrete components are simulated and tested. The maximum relative error is 1.62 % for the resistance measurement and 6.38 % for the capacitance measurement.**

Index Terms—**Demodulation; Field programmable gate arrays; Lock-in detection; Lossy capacitance.**

I. INTRODUCTION

Capacitance measuring based sensing is an efficient method to detect many real-world parameters [1]. Capacitive sensors can be used in measurement of displacement [2], pressure [3], force [4], humidity [5], moisture [6] or liquid level [7]. Capacitances are inherently lossy [8] and they can be represented as an ideal capacitance C_x in parallel with a loss resistance R_x as shown in Fig. 1. The lossy capacitances can also be modeled as variable resistor and capacitors in parallel [9]. C_{p1} and C_{p2} represent stray capacitances, which arise from cables connected to the measured capacitance [10] and result from the input capacitance of the amplifier used [11]. The effect of C_{p1} can be reduced by exciting the lossy capacitance with a low-impedance input signal from terminal 1 in Fig. 1 [12]. The measuring circuit's insensitivity to C_{p2} can be assured by virtually grounding terminal 2 in Fig. 1 using an operational amplifier (op-amp). The potential difference over the parasitic capacitance is maintained at zero volts [13].
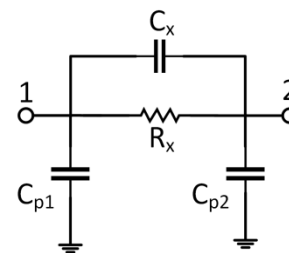
Fig. 1. Lossy capacitance model.

Driving the lossy capacitance with an AC voltage source creates a current which flows through R_x and C_x. A transimpedance amplifier (TIA) consisting of an op-amp and a feedback resistor converts this current into voltage. This voltage value contains information regarding the unknown resistance and capacitance. In order to extract capacitance and resistance values, a demodulation method called lock-in detection can be used [14]. Lock-in detection circuit gives a DC output voltage which is a function of its input signal's amplitude and the phase difference between the input and reference signal. Basically, lock-in detection rectifies its input signal and takes average of the rectified signal, and it is especially useful in the presence of noisy input signals [15]. The detection circuit comprises a multiplication unit and a low-pass filter (LPF). The multiplication unit can be realized using analog multipliers or switches. Although analog multipliers are better at being insensitive to harmonics introduced by the multiplication, they are expensive [16]. In this work, low cost analog switches are employed for the multiplication unit. Multiplication operation multiplies the input signal with +1 or -1 depending upon the positions of analog switches which are controlled by reference signals. A field programmable gate array (FPGA) can be used to provide both the driving signal and reference signals [17]. In FPGA fabric, the sinusoidal excitation input can be produced by direct digital synthesizer (DDS) method [18]. The excitation signal's amplitude and frequency can be controlled digitally using DDS which offers extra flexibility. Also, the phase shift between the driving signal and reference signals can be controlled precisely so that errors due to the phase shifts can be reduced [19]. The output of the multiplication is followed by a LPF that determines the DC level of the multiplied signal [20].

This DC output signal can be expressed as a function of unknown capacitance and resistance plus known parameters of the overall circuit. Unknown resistance and capacitor parameters can be calculated numerically after measuring the DC level.

II. THE CIRCUIT DESCRIPTION

The measurement circuit's overall design schematic is illustrated in Fig. 2. DDS methodology can be implemented on FPGA to generate the sinusoidal excitation signal [21], [22]. It provides fine frequency resolution, fast frequency switching between output signals, and continuous phase signal generation [20]. In this work, digital implementation of the excitation signal is accomplished by the means of Xilinx's DDS Intellectual Property (IP) [23]. A 12-bit digital-to-analog converter (DAC) is used to convert digitally generated sinusoidal samples into analog domain. In order to make DAC work properly, a DAC driver component is implemented on FPGA using hardware definition language (HDL). A passive LPF is added after the DAC to smooth the generated excitation wave. After lossy capacitance is driven by the smoothened sine wave, TIA converts the flowing current into a voltage value. TIA is simply designed with the help of an op-amp and a resistor. The resistor can be connected between the inverting input and output of the op-amp, whereas the non-inverting input is grounded. In this way, the effect of stray capacitances between the lossy capacitance and the input of the op-amp is greatly reduced [10]. TIA produces an output in the form of voltage that contains the values of unknown capacitance and

resistance in addition to the values of feedback resistance and excitation voltage. An analogously realized lock-in detector circuit is able to extract the values of lossy capacitance. Lock-in detector either inverts or directly transfers its input signal to the active LPF depending on the position and frequency of the switches. The switches are controlled by the reference signals. These reference signals are two non-overlapping square waves that are obtained by simply dividing the global clock signal; thus, switch-driving circuit consisting of an analog buffer and an inverter as given in [13] is no longer needed. Moreover, a phase shifter component is written in HDL to arrange the phase shift between the input signal and reference signals. The phase shifter component which is implemented digitally on FPGA removes the need for analog realization of a phase shifter circuit as suggested in [16]. Transistor-transistor logic (TTL) level converter is employed to convert 3.3 V square waves into 5 V so that reference signals will be compatible with driving the switches. Since the active LPF should only pass the low-frequency components of its input signal and suppress unwanted higher frequency harmonics, a second-order Sallen-Key Butterworth LPF with a low cut-off frequency is designed and implemented. The output of the LPF is measured with the aid of the FPGA's integrated 12-bit 1 MSPS analog-to-digital converter (ADC) [24]. To sum up, FPGA performs three tasks: generation and application of analog signals, controlling of the phase shift, and measurement of the DC output. As a result, a complete and flexible mixed-signal lossy capacitance measurement circuit is proposed.
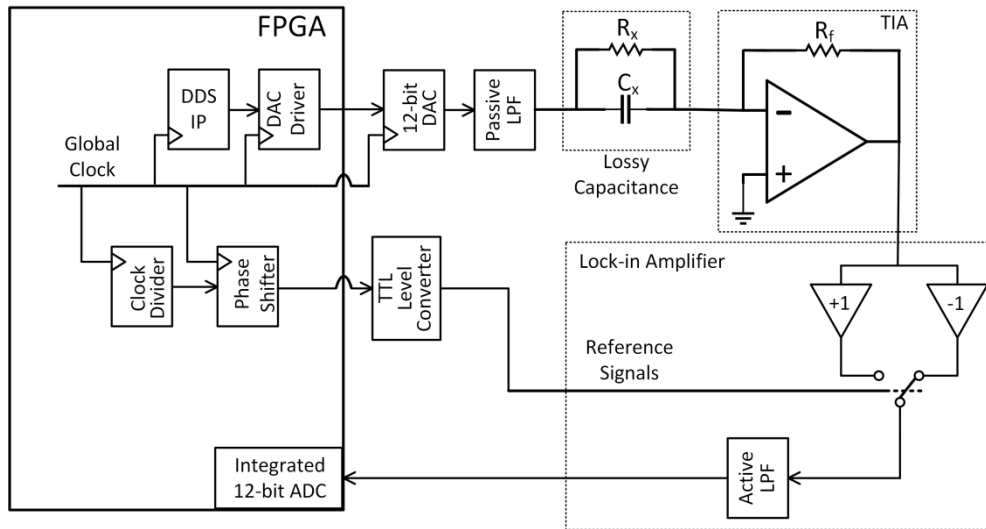

Fig. 2. Overall measurement circuit.

III. THEORETICAL ANALYSIS

The voltage at the output of TIA given in Fig. 1 is the signal that will be demodulated by the lock-in detection circuit. Its expression can be written as in (1) in the frequency domain

$$V_{out} = -V_{in}\left(\cfrac{1}{\cfrac{1}{A_v(f)} + \cfrac{Z_x}{A_v(f)R_f} + \cfrac{Z_x}{R_f}}\right), \qquad (1)$$

where V_{in} and V_{out} are the input and output voltages of TIA, respectively. Z_x is the impedance of the lossy capacitance

which is composed of desired capacitance and resistance connected in parallel. R_f is the feedback resistor of TIA and ω is the natural frequency of the input signal. $A_v(f)$ represents the open-loop gain of the op-amp which is inversely proportional to frequency. If TIA's usual operation frequency is taken into consideration, the open-loop gain value is much larger than the terms it is compared with in (1)'s denominator; thus, the output voltage expression can be simplified as in (2)

$$V_{out} = -V_{in}\frac{R_f}{Z_x} = -V_{in}\left(\frac{R_f}{R_x} + j\omega C_x R_f\right). \qquad (2)$$

Equation (2) implies that when a sinusoidal input voltage is applied to the input, TIA produces a sinusoidal output wave with different amplitude and phase, but with the same frequency. The output voltage of TIA has two terms with $90\,°$ phase shift. Therefore, the first component in (2) can be used to extract the value of unknown resistance while the second component can be used to find the capacitance value of the lossy capacitance.

The lock-in detector's role is to demodulate the output of TIA and extract lossy capacitance's unknown values. Its output signal will be proportional to the real or imaginary part of (2) depending on the phase of the reference signal [25]. Although a commercial analog multiplier is not explicitly used, the switches multiply the input signal with a square wave which has amplitude of 1 V and the same frequency with the input signal. If it is assumed that the lock-in detector's input is a sine wave as in (3)

$$x(t) = A\sin(\omega t + \theta), \tag{3}$$

where A, ω, and θ represent the input signal's amplitude, natural frequency, and phase shift with the reference signal, respectively. Two $90\,°$ phase shifted square waves can be generated as reference signals. The square waves can be approximated as the sum of odd frequency sinusoids as given in (4) and (5):

$$r_1(t) = \text{sqr}(\omega t) = \frac{4}{\pi}\left(\sin(\omega t) + \frac{1}{3}\sin(3\omega t) + \frac{1}{5}\sin(5\omega t) + ... \right) = \frac{4}{\pi}\sum_{k=0}^{\infty}\frac{1}{2k+1}\sin\left[(2k+1)\omega t\right], \tag{4}$$

$$r_2(t) = \text{sqr}\left(\omega t + \frac{\pi}{2}\right) = \frac{4}{\pi}\sum_{k=0}^{\infty}\frac{1}{2k+1}\cos\left[(2k+1)\omega t\right]. \tag{5}$$

The multiplication of the input signal with the first reference signal in (4) results in the in-phase output as given in (6) due to the $0\,°$ phase difference between the multiplicand signals

$$I = x(t)\cdot r_1(\omega t) = \frac{2}{\pi}A\cos(\theta) - \frac{2}{\pi}A\cos(2\omega t + \theta) +$$
$$+\frac{2}{\pi}A\sum_{k=1}^{\infty}\frac{1}{2k+1}\left[\cos(2k\omega t - \theta) - \cos(2(k+1)\omega t + \theta)\right]. \tag{6}$$

Similarly, when the input signal is multiplied with the shifted reference signal in (5), the product is the quadrature-phase output as given in (7)

$$Q = x(t)\times r_2\left(\omega t + \frac{\pi}{2}\right) = \frac{2}{\pi}A\sin(\theta) + \frac{2}{\pi}A\sin(2\omega t + \theta) +$$
$$+\frac{2}{\pi}A\sum_{k=1}^{\infty}\frac{1}{2k+1}\left[\sin(2(k+1)\omega t + \theta) - \sin(2k\omega t - \theta)\right]. \tag{7}$$

A low-pass filter with a cut-off frequency lower than ω stops the high frequency components and passes only the first terms given in (6) and (7). Therefore, the output of low-pass filter for in-phase and quadrature-phase components can be expressed as in (8) and (9):

$$I = \frac{2}{\pi}A\cos(\theta), \tag{8}$$

$$Q = \frac{2}{\pi}A\sin(\theta). \tag{9}$$

The output of low-pass filter is a constant DC voltage which depends on the input signal's amplitude, as well as the phase difference between the input and the reference signal. The in-phase and quadrature-phase components are not found simultaneously, but the phase shifter implemented on FPGA shifts the phase. Thus, those components can be determined separately. When the phase shift is $0\,°$, I component is found, and when the phase shift is $90\,°$, Q component can be found. Consequently, the unknown resistance and capacitance can be calculated using (2), (8),

and (9) by the following expressions:

$$R_x = -\frac{2AR_f}{\pi I}, \tag{10}$$

$$C_x = -\frac{Q}{4AfR_f}. \tag{11}$$

The lossy capacitance's parameters can be found by simply measuring I and Q components at the output of the LPF and entering their values into (10) and (11).

IV. COMPUTER-BASED ANALYSIS

Computer-based analysis is the last step before experimental evaluation of the measurement system. The simulations of the excitation signal and reference signals are observed using Vivado Design Suite. On the other hand, the measurement circuit's performance is simulated using a Simulation Program with Integrated Circuit Emphasis (SPICE) program called as "LTSPICE".

A. Signal Generation Simulations

The excitation signal is constructed digitally using DDS method and implemented on FPGA. The signal is a sine wave with a frequency of 2 kHz and amplitude of 3.3 V_{p-p}. The output frequency of a DDS system can be defined as in (12)

$$f_{out} = \frac{f_{clk}\Delta\theta}{2^{B_{\theta(n)}}}, \tag{12}$$

where f_{clk} is the FPGA's system clock which is 100 MHz for the used board. $B_{\theta(n)}$ is the number of bits in the phase accumulator and $\Delta\theta$ is the phase increment value. The phase increment value is calculated and entered into Xilinx's DDS Compiler IP to generate the required output frequency. FPGA's system clock is also exploited to generate reference signals. Reference signals are square waves to close and open switches in lock-in detection, so a frequency divider using counters is enough for the signal generation. The reference signals are routed out through Digilent's Peripheral Module (PMOD) interface. Figure 3 depicts the

behavioural simulations of the system clock, the excitation signal, and non-overlapping reference signals in-phase with the excitation input.
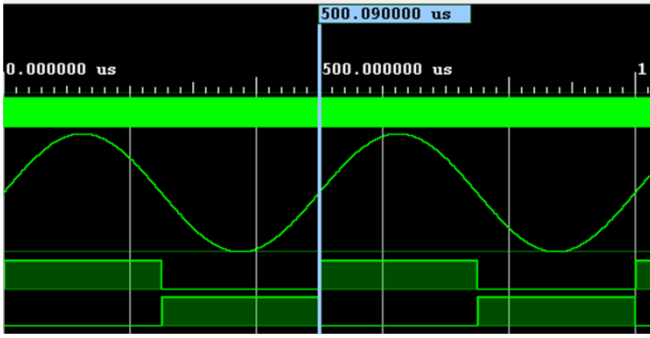

Fig. 3. Digitally generated excitation signal and reference signals.

Figure 3 indicates that all of three waveforms have a period of 500 µs period which corresponds to a frequency of 2 kHz. Sine wave samples are produced for a 12-bit DAC that converts digital samples into analog domain and drives the lossy capacitance circuit.

B. SPICE Simulations

SPICE simulation is a decent way of predicting the real-world performance of a circuit. It enables the designer to choose proper components before actually testing circuits. In this work, SPICE-based circuit simulations are carried out using LTSPICE. Initially, the measurement circuit is analysed in two parts. In the first part, the lossy capacitance is driven by the excitation signal and the performance of TIA is observed. In the second part, analog lock-in detector is constructed using switches, op-amps, and passive circuit elements. Finally, the overall measurement circuit's simulation is performed to observe its eventual behaviour.

The schematic of lossy capacitance and TIA is shown in Fig. 4. A 4.7 kΩ resistance and a 10 nF capacitor forms the lossy capacitance. The op-amp OA1 used in TIA design has the following properties: 1M open-loop voltage gain, 10 MHz gain-bandwidth product, 10 V/µs slew-rate, 25 mA output current limit, 45 ° phase-margin, and 500 MΩ input resistance. A 10 kΩ feedback resistance sets the gain of the TIA. Firstly, an AC analysis is carried out for the frequency range from 10 Hz to 100 MHz. Then, a 2 kHz 3.3 V_{p-p} sine wave is applied to find out the transient response.
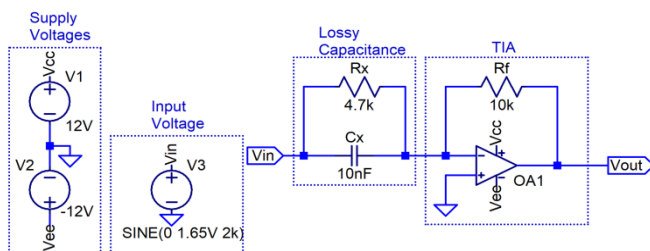

Fig. 4. Schematic of lossy capacitance and TIA.

The frequency response of the lossy capacitance and TIA is shown in Fig. 5. Although the operation frequency is 2 kHz, gain and phase responses are plotted against a wide frequency range. This provides an insight into how the circuit operates at higher frequencies. The circuit shows a behavior of an inverting amplifier. The output amplitude increases with frequency because the impedance of lossy

capacitance decreases. However, when the frequency is high enough, the gain-bandwidth product of the op-amp starts to reduce the gain. Two datatips displayed in Fig. 5 indicate that the gain is around 7.86 dB and phase is -149.5 ° at the operating frequency.
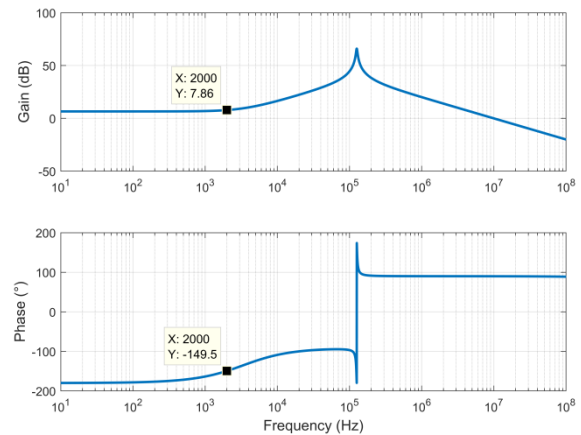

Fig. 5. Frequency response of lossy capacitance and TIA.

Figure 6 indicates the input and output signals in time domain when the transient analysis is run for ten periods. The datatips on Fig. 6 show that if the input's peak is 1.65 V, then the output's peak voltage is 4.064 V at 2 kHz. Thus, since the output voltage does not saturate at this frequency, it contains information of lossy capacitance.
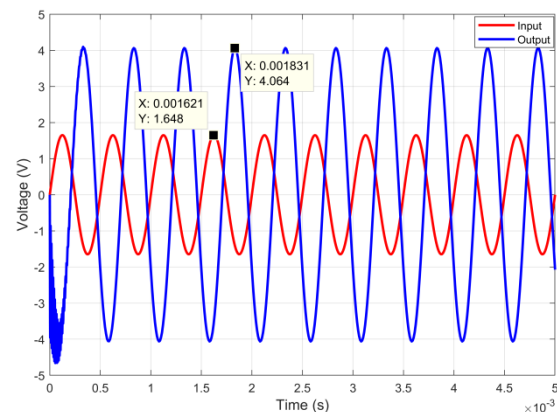

Fig. 6. Transient response of lossy capacitance and TIA.

The analog lock-in detector's schematic, which is drawn in LTSPICE, is shown in Fig. 7. The detection circuit is made up of multiplication part and LPF part. The multiplication part is designed using four switches which are controlled by two non-overlapping square-waves. When the switches S2 and S3 are on, the switches S1 and S4 are off and the resistors and op-amp produces a gain of +1. Similarly, if the switches S2 and S3 are off, the switches S1 and S4 turn on and the circuit produces a gain of -1. If the input signal and the reference signal are in-phase, then multiplication circuit generates a full-wave rectified output as shown in Fig. 8. Its output signal's frequency is 4 kHz with a peak voltage of 1 V.

The designed LPF performs to find the average value of the output of multiplication circuit which consists of a DC value plus high frequency components. This LPF is an active filter whose topology is Sallen-Key with a second

order Butterworth response. The filter's gain is 0 dB in the passband, while the corner frequency is 40 Hz. The gain is -80 dB at 4 kHz so that harmonics are reduced sufficiently by this LPF. The output of the LPF in time domain is shown in Fig. 9. The settling time is around 25 ms and the steady-state output is approximately 0.635 V, which is compatible with (8).
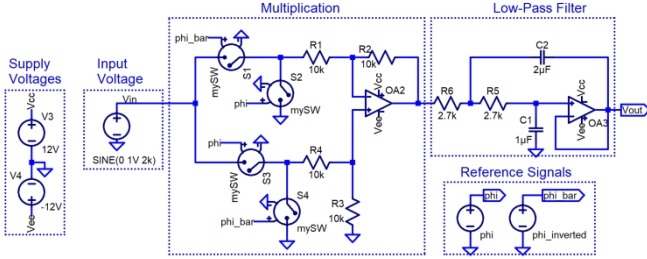

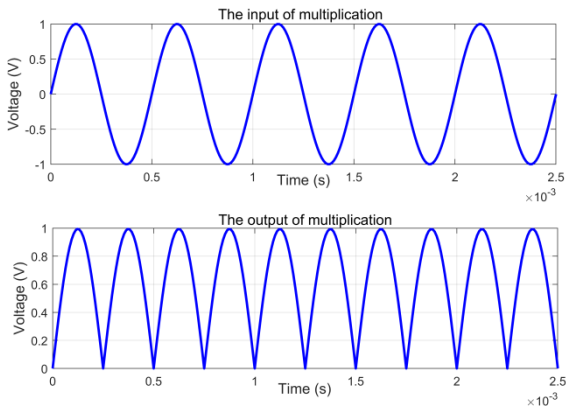Fig. 7. Schematic of lock-in detector.

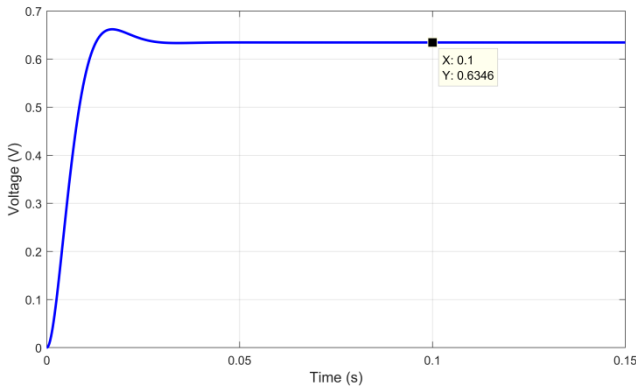Fig. 8. The input and output signals of multiplication unit.

Fig. 9. The output of LPF.

Eventually, the performance of the overall measurement circuit is simulated and tested by bringing the lossy

capacitance, TIA, and lock-in detector altogether in the same LTSPICE schematic. Time domain analyzes are carried out to be able find the values of three different lossy capacitances. In these simulations, the excitation signal is 3.3 V_{p-p} 2 kHz sine wave and the reference signal is 0 V–5 V square wave. The phase shift is given to the system by adding delays to the reference signals. Three different lossy capacitance values are simulated such that R_x = 4.7 kΩ and C_x = 10 nF, R_x = 10 kΩ, and C_x = 4.7 nF, and R_x = 22 kΩ and C_x = 2.2 nF, respectively. The in-phase (I) and quadrature-phase (Q) components are found for each simulation. Simulated values of R_x and C_x are calculated using (10) and (11). All those values are tabulated in Table I. Then, certain error analyses are carried out. Relative errors can be defined as in (13)

$$\text{relative error } (\%)= \frac{\left|\text{simulated value - real value}\right|}{\text{real value}} \times 100. \quad (13)$$

TABLE I. SIMULATION RESULTS FOR DIFFERENT LOSSY CAPACITANCES.

R_x (kΩ)	C_x (nF)	I (V)	Q (V)	Simulated R_x (kΩ)	Simulated C_x (nF)
4.7	10	-2.226	-1.325	4.719	10.038
10	4.7	-1.047	-0.627	10.033	4.742
22	2.2	-0.476	-0.289	22.068	2.189

The worst case error is simulated due to assess the effect of tolerances of the passive circuit elements used in the overall measurement circuit. Resistors and capacitors employed in TIA, multiplication unit and LPF are assumed to have 1 % and 5 % tolerances, respectively. The worst case error is determined by identifying the most deviation from the simulated values of I and Q, then calculating the new worst values of R_x and C_x and comparing them with the real values as given in (13). On the other hand, the phase error is defined as the error caused by a phase mismatch between the input signal and the reference signal. A 5 % phase mismatch is intentionally created between interested signals and relative errors are calculated again using (13). All types of errors and their values are listed in Table II.

The maximum relative error is 0.40 % for resistance simulation and 0.89 % for capacitance simulation when component tolerances are not taken into consideration and no phase mismatch exists. However, the maximum relative error increases to 2.55 % for R_x and 3.41 % for C_x when the component tolerances affect the measurement in the worst way. Table II also proves the significance of accurate phase shift because the maximum relative error may rise to 6.38 % for R_x and 14.77% for C_x even for a 5 % phase mismatch.

TABLE II. RELATIVE ERRORS, WORST CASE ERRORS, AND PHASE ERRORS FOR DIFFERENT LOSSY CAPACITANCES.

R_x (kΩ)	C_x (nF)	Relative Error for R_x (%)	Relative Error for C_x (%)	Worst Case Error for R_x (%)	Worst Case Error for C_x (%)	Phase Error for R_x (%)	Phase Error for C_x (%)
4.7	10	0.40	0.38	2.49	3.41	6.38	14.77
10	4.7	0.33	0.89	2.46	2.96	6.32	14.44
22	2.2	0.31	0.50	2.55	2.61	6.33	13.64

V. EXPERIMENTAL ANALYSIS

The experimental set-up is arranged according to the schematic given in Fig. 2. Xilinx ZedBoard FPGA is used for generating the required signals and for measuring the DC

output of the lock-in detector. The analog lock-in detector circuit is built on a breadboard. A commercial 3-pole passive LC filter with a 0.3 MHz cut-off frequency is connected before the lossy capacitance to smoothen the excitation signal. Also, the reference signals are converted

from 0 V–3.3 V to 0 V–5 V by a level converter. Three AD844 high-speed op-amps are used as a part of TIA, multiplication unit, and LPF. A quad bilateral switch CD4066B is used to multiply the input signal with reference signals coming from the level converter. Since ZedBoard's 12-bit ADC has an analog input range from -0.5 V to +0.5 V in bipolar mode, a resistive voltage divider is placed after the LPF so that the input range of the ADC is not exceeded. The circuit diagram for the DC output measurement is given in Fig. 10. The ZedBoard has an in-built anti-aliasing filter which is used to attenuate higher frequency components. Although the ADC stores its analog inputs as 12-bit digital values, the system monitor enables the user to monitor the averaged values of the measured voltages on PC.
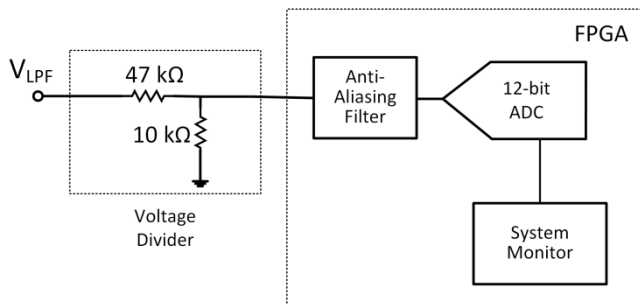

Fig. 10. DC output measurement circuit diagram.

In this work, this feature is used to monitor measured in-phase and quadrature-phase voltage components. The overall design photo of the experimental setup is given in Fig. 11.
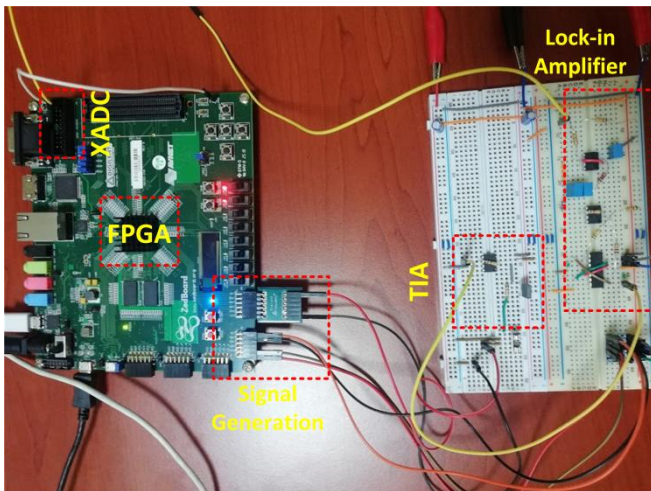

Fig. 11. Experimental setup.

In order to emulate lossy capacitance, three different combinations of discrete resistors and capacitors are selected. Nominal values of $R_x = 4.7$ kΩ and $C_x = 10$ nF, $R_x = 10$ kΩ and $C_x = 4.7$ nF, and $R_x = 22$ kΩ and $C_x = 2.2$ nF are tested in the measurement circuit. Real values of the capacitance and resistance are obtained from CHY 41R LCR meter that can measure resistance and capacitance with 0.5 % and 0.7 % accuracy, respectively. Table III demonstrates the real values obtained from LCR meter, the experimentally measured values, and relative errors for each lossy capacitance. The maximum relative error is 1.62 % for the resistance measurement and 6.38 % for the capacitance measurement. Those errors can be associated with the on-

resistance of the switches, non-ideal characteristics of the op-amps, and variations in the values of passive components. Although the relative errors are related to the measured values of resistance and capacitance, the obtained relative errors are comparable with that of similar studies in the literature [13], [16]. Compared with the simulation-based relative errors, experimental results indicate higher amounts of relative errors because of the aforementioned reasons. On the other hand, the measurement circuit performs better than phase error simulations in terms of relative errors. Thus, phase-related errors are significantly reduced in the experimental circuit with the help of accurate phase shifts provided by the FPGA. The errors caused by the tolerances of the circuit components can be decreased by employing lower tolerance passive elements in the design of TIA and lock-in detector.

TABLE III. EXPERIMENTAL RESULTS FOR DIFFERENT LOSSY CAPACITANCES

Real R_x (kΩ)	Real C_x (nF)	Measured R_x (kΩ)	Measured C_x (nF)	Relative Error for R_x (%)	Relative Error for C_x (%)
4.611	9.798	4.640	9.610	0.63	1.92
9.846	4.634	9.958	4.446	1.14	4.06
22.080	2.242	22.438	2.099	1.62	6.38

VI. CONCLUSIONS

The purpose of this study is to design, simulate, and experimentally test a lossy capacitance measuring circuit consisting of a digital signal processing platform and analog circuit elements. Firstly, theoretical background of the measuring circuit is laid out. Then, computer-based analysis is carried out to anticipate the real-world behaviour of the overall system, including signal generation simulations and SPICE-based circuit simulations. In simulation environment, three different error analyses are performed to determine the possible sources of errors. It is found out that the tolerances of the passive elements used to construct the measuring circuit can cause considerable amount of error. In the worst case scenario, a maximum error is found to be 2.55 % for resistance measurement and 3.41 % for capacitance measurement. Another major factor that causes measurement errors is identified as the inaccurate phase shift. In fact, it can cause 6.38 % and 14.77 % of maximum relative errors for resistance and capacitance measurements, respectively. In order to reduce the effect of phase mismatch, the excitation signal and reference signals are generated using the same internal clock so that the phase shift between these signals is controlled accurately in digital domain. In this way, analog phase shifter circuit and analog switch-driving circuit, suggested in the literature, are also no longer required. This measurement circuit can measure the final DC output of the system with precision, relieving the need for a separate measurement device. Furthermore, the measurement setup can be utilized for analog multiplier based lock-in detector by generating the reference sine wave using DDS method. A limitation of this measurement setup is that the analog lock-in detection part is built on a breadboard which makes it open to environmental interference. Also, undesired noises can be produced from the analog parts of the circuit, unlike the digital lock-in detectors.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

REFERENCES

[1] L. K. Baxter, *Capacitive Sensors: Design and Applications*. IEEE Press, Dec. 1997, pp. 221–270. DOI: 10.1109/9780470544228.

[2] M. Kim, W. Moon, E. Yoon, and K.-R. J. Lee, "A new capacitive displacement sensor with high accuracy and long-range", *Sensors and Actuators A: Physical*, vol. 130, pp. 135–141, 2006. DOI: 10.1016/j.sna.2005.12.012.

[3] M.-X. Zhou, Q.-A. Huang, M. Qin, and W. Zhou, "A novel capacitive pressure sensor based on sandwich structures", *Journal of Microelectromechanical Systems*, vol. 14, no. 6, pp. 1272–1282, 2005. DOI: 10.1109/JMEMS.2005.859100.

[4] J. A. Dobrzynska and M. A. M. Gijs, "Polymer-based flexible capacitive sensor for three-axial force measurements", *Journal of Micromechanics and Microengineering*, vol. 23, no. 1, p. 015009, 2012. DOI: 10.1088/0960-1317/23/1/015009.

[5] F. Reverter and O. J. S. Casas, "Direct interface circuit for capacitive humidity sensors", *Sensors and Actuators A: Physical*, vol. 143, no. 2, pp. 315–322, 2008. DOI: 10.1016/j.sna.2007.11.018.

[6] H. Eller and A. Denoth, "A capacitive soil moisture sensor", *Journal of Hydrology*, vol. 185, no. 1–4, pp. 137–146, 1996. DOI: 10.1016/0022-1694(95)03003-4.

[7] F. Reverter, X. Li, and G. C. M. Meijer, "Liquid-level measurement system based on a remote grounded capacitive sensor", *Sensors and Actuators A: Physical*, vol. 138, no. 1, pp. 1–8, 2007. DOI: 10.1016/j.sna.2007.04.027.

[8] E. Alnasser, "A novel fully analog signal conditioning circuit for loss-less capacitive sensor estimation", *IEEE Sensors Journal*, vol. 19, no. 18, pp. 8019–8026, 2019. DOI: 10.1109/JSEN.2019.2917029.

[9] A. U. Khan, T. Islam, B. George, and M. Rehman, "An efficient interface circuit for lossy capacitive sensors", *IEEE Trans. on Instrumentation and Measurement*, vol. 68, no. 3, pp. 829–836, 2019. DOI: 10.1109/TIM.2018.2853219.

[10] W. Q. Yang, A. L. Stott, and J. C. Gamio, "Analysis of the effect of stray capacitance on an ac-based capacitance tomography transducer", *IEEE Trans. on Instrumentation and Measurement*, vol. 52, no. 5, pp. 1674–1681, 2003. DOI: 10.1109/TIM.2003.817925.

[11] S. Lányi, "The noise of input stages with low parasitic capacitance", *Measurement Science and Technology*, vol. 12, no. 9, pp. 1456–1464, 2001. DOI: 10.1088/0957-0233/12/9/311.

[12] A. U. Khan, T. Islam, B. George, and M. Rehman, "An efficient interface circuit for lossy capacitive sensors", *IEEE Trans. on Instrumentation and Measurement*, vol. 68, no. 3, pp. 829–836, 2019. DOI: 10.1109/TIM.2018.2853219.

[13] D. Chen, W. Yang, and M. Pan, "Design of impedance measuring circuits based on phase-sensitive demodulation technique", *IEEE Trans. on Instrumentation and Measurement*, vol. 60, no. 4, pp. 1276–1282, 2010. DOI: 10.1109/TIM.2010.2084770.

[14] S. T. Ahsan and H. McCann, "Digital phase-sensitive detector (PSD) as accumulator-sampler and its implementation in FPGA", *Science International-Lahore*, vol. 26, no. 1, pp. 65–73, 2014.

[15] R. W. M. Smith, I. L. Freeston, B. H. Brown, and A. M. Sinton, "Design of a phase-sensitive detector to maximize signal-to-noise ratio in the presence of Gaussian wideband noise", *Measurement Science and Technology*, vol. 3, no. 11, pp. 1054–1062, 1992. DOI: 10.1088/0957-0233/3/11/006.

[16] W. Yang, "Teaching phase-sensitive demodulation for signal conditioning to undergraduate students", *American Journal of Physics*, vol. 78, no. 9, pp. 909–915, 2010. DOI: 10.1119/1.3428642.

[17] Z. Cui, H. Wang, Z. Chen, Y. Xu, and W. Yang, "A high-performance digital system for electrical capacitance tomography", *Measurement Science and Technology*, vol. 22, no. 5, p. 055503, 2011. DOI: 10.1088/0957-0233/22/5/055503.

[18] W. Huaxiang, C. Ziqiang, X. Yanbin, Z. Lifeng, and H. Yongbo, "Digital signal processing in electrical capacitance tomography", in *Proc. of 2008 IEEE Asia Pacific Conf. on Circuits and Systems*, Macau, 2008, pp. 465–468. DOI: 10.1109/APCCAS.2008.4746061.

[19] C. Kolle and P. O'Leary, "Low-cost, high-precision measurement system for capacitive sensors", *Measurement Science and Technology*, vol. 9, no. 3, pp. 510–517, 1998. DOI: 10.1088/0957-0233/9/3/028.

[20] D. Chen, W. Yang, and M. Pan, "The dynamic response of a Butterworth low-pass filter in an ac-based electrical capacitance tomography system", *Measurement Science and Technology*, vol. 21, no. 10, p. 105505, 2010. DOI: 10.1088/0957-0233/21/10/105505.

[21] Y. Fang and X. Chen, "Design and simulation of DDS based on Quartus II", in *Proc. of 2011 IEEE International Conference on Computer Science and Automation Engineering*, Shangai, 2011, vol. 2, pp. 357–360. DOI: 10.1109/CSAE.2011.5952487.

[22] M. Genovese and E. Napoli, "Direct digital frequency synthesizers implemented on high end FPGA devices", in *Proc. of the 2013 9th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Villach, 2013, pp. 137–140. DOI: 10.1109/PRIME.2013.6603105.

[23] Xilinx, "DDS Compiler v6.0 LogiCORE IP Product Guide". [Online]. Available: https://www.xilinx.com/support/documentation/ip_documentation/dds_compiler/v6_0/pg141-dds-compiler.pdf

[24] Xilinx, "XADC Wizard v3.3 LogiCORE IP Product Guide". [Online]. Available: https://www.xilinx.com/support/documentation/ip_documentation/xadc_wiz/v3_3/pg091-xadc-wiz.pdf

[25] O. Teren, J. Tomlain, and R. Sedlacek, "Direct comparison of analogue and digital FGPA-based approaches to synchronous detection", *Metrology and Measurement Systems*, vol. 25, no. 1, 2018. DOI: 10.24425/118162.