Single Conversion Stage Three Port High Gain Converter for PV Integration with DC Microgrid

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***Abstract*—A high gain three port converter with a unidirectional port for photovoltaic (PV) side and two bidirectional ports one each for the battery and the DC bus for PV integration to DC microgrid is presented. High gain is achieved by a coupled inductor with switched capacitor, whereas single stage conversion is used between the ports to achieve high efficiency. The proposed converter is modelled in PLECS/MATLAB and the simulated results for various operational modes are validated using a 500 W prototype. For main operating mode, i.e., single input single output (SISO), the efficiency is calculated to be as high as 96 %. Similarly, owing to the reduced number of components, the losses are reduced considerably for different operation modes.**

***Index Terms*—Boost; Simulink; Photovoltaic; Hybrid; Buck-boost; Multiport.**

I. INTRODUCTION

The photovoltaic (PV) power generation increases day by day with global installed capacity of 505 GW at the end of year 2018 [1]. The PV generation system is economical and long lasting solution to remote area electricity generation and distribution system. However, the low generation and intermittent nature of the PV system limit the implementation of this system. Therefore, multiple generation technologies need to be hybridized in order to have a steady availability of the power. For this, the multiport high gain power electronics converter is an obvious solution. Such converters can take input from multiple sources to drive the load.

There are many single or multistage converter topologies as addressed in [2]. The multiport power electronics are highly dense, cost effective, and efficient. In [3], A. K. Bhattacharjee *et al*. presented a comparison of the different topologies based on multiplier circuit, doubler and transformer.

A special type of multiport converters is a three port converter (TPC) having generating source and storage system. A comprehensive review of TPC topologies is presented in [4]. However, the common issue associated with these topologies is to achieve the high conversion gain suitable for the PV system that always prefers the voltage boosting techniques. M. Forouzesh *et al*. in [5] have reviewed the voltage boosting techniques. The techniques presented are the doubler and multiplier circuit, switched capacitor and coupled inductor. The coupled inductor based techniques are preferred for the high voltage and medium frequency applications. Based on these techniques, various high gain three port converters are presented in the literature [6]–[25].

Three port converters are classified as isolated [6]–[11] and non-isolated [12]–[18]. The isolated converter topologies are preferred where galvanic isolation is required, whereas the non-isolated converters are preferred due to the reduced size, cost, and simplicity. The reduced switch three port non-isolated converter topologies further enhance its usability. In [12], a single inductor based non-isolated TPC is presented. The basic buck and boost converter legs are used to process power between ports. Although converter topology is simple, but the gain is low. Also, the use of too many passive components and multistage power conversion reduce the converter efficiency. In [13], F. Kardan *et al*. proposed a TPC by using the conventional buck-boost converter. Authors developed prototype of 153 W at switching frequency of 30 kHz. The converter topology is simple and has flexible operation. However, the gain of the converter is very low along with too many passive components. In [14], R. Faraji *et al*. presented a coupled inductor based non-isolated TPC. Authors developed a 150 W prototype at 50 kHz for 400 V DC Bus. They used battery port applying the buck converter. Ch.-M. Lai *et al*. in [15] used a coupled inductor and capacitor stack based converter for fuel cell application. The converter has relatively high gain, but with too many passive components in the topology. An integrated three port converter for PV system is presented in [16]. Authors explain the complete energy management and control strategy of the proposed converter. The converter topology is simple, but has relatively low gain. In [17], B. Honarjoo *et al*. presented a single coupled inductor-based TPC for the PV applications. The converter has single element common for its operation. Although converter has high gain and reduced number of devices, it has the demerit of a low reliability.

The advantage of the coupled inductor-based topologies is that the required gain is achieved by an appropriate turns ratio leading to the decreased voltage stress. Due to

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increasing the turns ratio of the coupled inductor for achieving higher gain, it bears the disadvantages of higher leakage inductance, increased losses, and higher voltage spikes. Fortunately, these disadvantages can be overcome by proper design of the coupled inductor and using clamp circuit along with appropriate voltage boosting techniques.

In this paper, a three port bidirectional converter using single conversion stage is proposed. The proposed converter is modified form of the topologies presented in [18], [19] with reduced number of active and passive components while improving the operation of the converter and increasing the efficiency. A coupled inductor along with switched capacitor are used to achieve high voltage gain, which will, ultimately, enhance converter applications. The proposed converter is analyzed in continuous conduction mode (CCM). The battery is connected as it can be charged by the leakage inductance energy. The leakage inductance energy can also be used to achieve the zero voltage switching (ZVS). Moreover, the converter theoretical analysis in the single input single output (SISO) mode, double input single output (DISO) mode, and single input double output (SIDO) modes are explained. As obvious from the literature, higher the component count, higher is the loss in the converter. With reduced number of components used in the proposed converter due to single stage conversion, the loss of the converter is expected to be lesser.

After introduction, the remaining paper is organized as follows. The theoretical and operational analysis in different operating modes is elaborated in Section II followed by the detailed design and mathematical modeling of the proposed converter in steady state is discussed in Section III. The Section IV explains the on simulation and hardware results and comparative study. The conclusions and future work are discussed in Section V.

II. PROPOSED CONVERTER OPERATION

The proposed converter is shown in Fig. 1.

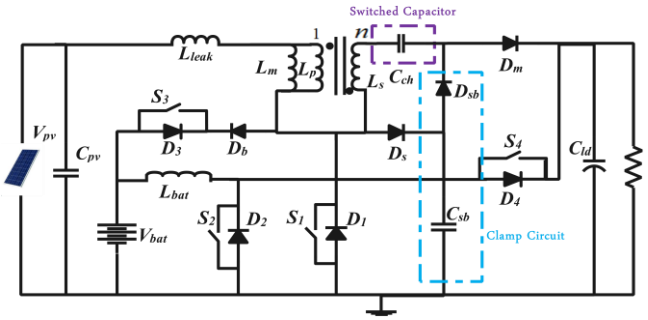


Fig. 1. Proposed converter.

It has three ports: one unidirectional port V_{pv} for PV, one port is V_{bat} for the battery source, and a bidirectional output port V_0. A coupled inductor with primary L_p and secondary L_s winding along with switched capacitor C_{ch} is used to achieve high voltage gain. The proposed converter has bidirectional power flow capability. It has four active switches S_1, S_2, S_3, and S_4, and four diodes D_b, D_s, D_{sb}, and D_m. There are three capacitors: switched capacitor C_{ch}, clamp capacitor C_{sb}, and the output capacitor C_{ld}. The proposed converter operation and analysis are explained for the single input single output (SISO) mode, double input single output (DISO) mode, and single input double output (SIDO) mode. The theoretical switching waveforms are shown in Fig. 2.

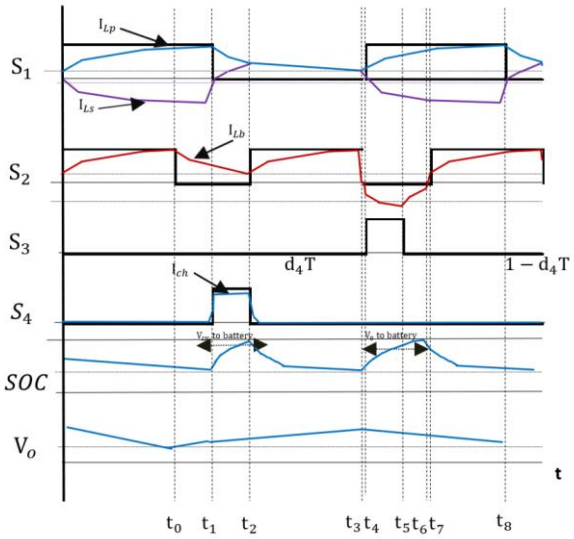


Fig. 2. Theoretical waveforms.

For the operation of the converter, it is assumed that all the components are ideal and capacitors are large enough to maintain the voltage constant.

A. SISO Mode

Due to a single input and output, only one conversion stage is used in this mode. The proposed converter has following operations.

1. *Power transfer from PV to main DC bus (Fig. 3(a))*

In this operation, converter supplies power from PV to the load. The equivalent circuit for this operation is shown in Fig. 3(a). The main operating switch is S_1. The operation is explained for the following states.

State-1 ($0 < t < D_1T$): In this state, switch S_1 is ON and the current I_{LP} increases. The current I_{LS} decreases, but in opposite direction. The capacitor C_{sb} charges the capacitor C_{ch} through diode D_{sb}. The converter has the following equations for this state:

$$\frac{dI_{LP}}{dt} = \frac{V_{pv}}{L_p}, \tag{1}$$

$$\frac{dI_{LS}}{dt} = \frac{V_{cb}}{n \times L_p}, \tag{2}$$

$$\frac{V_{cld}}{dt} = -\frac{V_{cld}}{C_{cl} \times R_{load}}. \tag{3}$$

State-2 ($D_1T < t < 1 - D_1T$): In this interval, coupled inductor energy is transferred to the load. The both currents I_{LP} and I_{LS} are same and decreasing. This interval has the following equations:

$$\frac{dI_{LP}}{dt}=\frac{V_{pv}-V_{cld}}{L_p}, \tag{4}$$

$$\frac{dI_{LS}}{dt}=\frac{V_{pv}-V_{cld}}{n\times L_p}. \tag{5}$$

$$\frac{V_{cld}}{dt}=\frac{I_{LP}}{C_{cl}}-\frac{V_{cld}}{C_{cl}\times R_{load}}. \tag{6}$$

2. *Power transfer from battery to main DC bus (Fig. 3(b))*

In this operation, the power is delivered to the main DC bus from the battery. As the PV power is not available, load is served by the battery system. The main operating switch is S_2. The operation is explained for the following time intervals.

State-1 ($0<t<D_2T$): In this interval, the switch S_1 is ON. The current I_{lb} through the inductor L_{bat} increases linearly. This interval has the following equations:

$$\frac{I_{lb}}{dt}=\frac{V_{bat}}{L_{bat}}, \tag{7}$$

$$\frac{dV_{cld}}{dt}=-\frac{V_{cld}}{C_{cld}\times R_{load}}. \tag{8}$$

State-2 ($D_2T<t<1-D_2T$): In this interval, the energy absorbed by the inductor L_{bat} is delivered to the load through the diode D_4. The following equations govern this interval:

$$\frac{I_{lb}}{dt}=\frac{V_{bat}-V_{cld}}{L_{bat}}, \tag{9}$$

$$\frac{dV_{cld}}{dt}=I_{lb}-\frac{V_{cld}}{C_{cld}\times R_{load}}. \tag{10}$$

3. *Battery charging from main DC bus (Fig. 3 (c))*

In this SISO mode, the input is main DC link capacitor and the output is battery. The main DC link capacitor is large enough to charge the battery. The main operating switch is S_4. The operation is explained for the following time intervals.

State-1 ($0<t<D_4T$): In this interval, the switch S_4 is ON and the current through inductor L_{bat} increases. The equations for this interval are

$$\frac{dI_{lb}}{dt}=-\frac{V_{cld}-V_{bat}}{L_{bat}}. \tag{11}$$

State-2 ($D_4T<t<1-D_4T$): In this interval, the switch S_4 is off. The inductor L_{bat} delivers the stored energy to the battery. The equations for these operations are:

$$\frac{dI_{lb}}{dt}=\frac{V_{bat}}{L_{bat}}, \tag{12}$$

$$\frac{dV_{bat}}{dt}=-\frac{V_{bat}}{C_{bat}\times R_{ch}}. \tag{13}$$

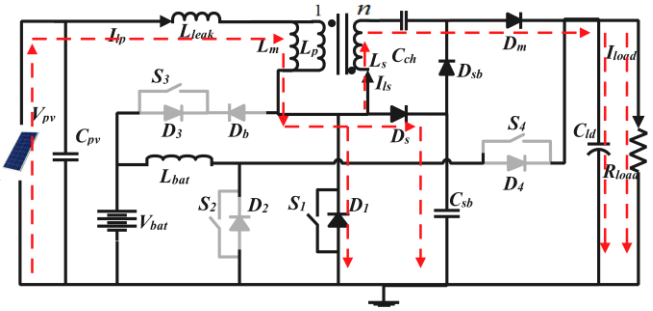
B. DISO Mode: (Fig. 3(d))

In this mode, PV power is not enough to facilitate the load. The battery is used to compensate for the reduced PV generation. For this mode, the voltage condition is $V_{bat} > V_{pv}$. So, D_2 is larger than the duty cycle D_1.

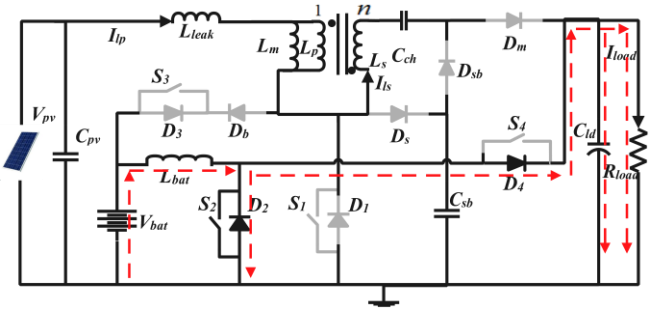
State-1 ($0<t<1-D_1T$ & $0<t<1-D_2T$): Both the switches S_1 and S_2 are ON and the currents I_{LP} and I_{LS} are increasing. The equations for this interval are:

$$\frac{I_{lb}}{dt}=\frac{V_{bat}}{L_{bat}}, \tag{14}$$

$$\frac{dV_{cld}}{dt}=-\frac{V_{cld}}{C_{cld}\times R_{load}}. \tag{15}$$



(a)



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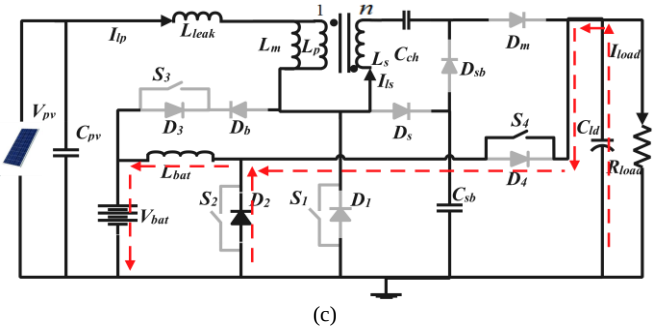
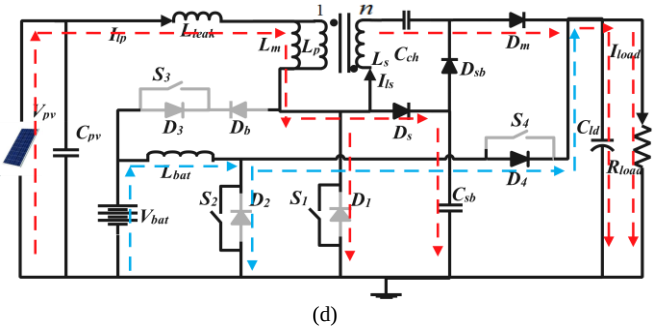
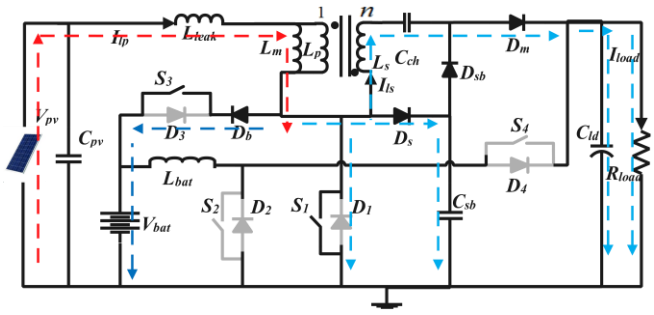


(c)



(d)



(e)

Fig. 3. Converter configuration: a) PV to main DC bus; b) Battery to main DC bus; c) Main DC bus to battery; d) Both battery and PV to main DC bus; f) (e)? PV to main both battery and main DC bus.

State-2 ($D_1 < t < 1-D_1T$ & $0 < t < 1-D_2T$): In this interval, the switch S_1 is off and the switch S_2 is still on. The equations are:

$$\frac{dI_{LP}}{dt} = \frac{V_{pv} - V_{cld}}{L_p}, \tag{16}$$

$$\frac{dI_{LS}}{dt} = \frac{V_{pv} - V_{cld}}{n \times L_p}, \tag{17}$$

$$\frac{V_{cld}}{dt} = \frac{I_{LP}}{V_{pv}} - \frac{V_{cld}}{C_{cl} \times R_{load}}. \tag{18}$$

State-3 ($D_1 < t < 1-D_1T$ & $D_2 < t < 1-D_2T$): In this interval, both the switches S_1 and S_2 are off. The energy stored in the coupled inductor and L_{bat} is transferred to the load. The equations for this modes are:

$$\frac{dI_{LP}}{dt} = \frac{V_{pv} - V_{cld}}{L_p}, \tag{19}$$

$$\frac{I_{lb}}{dt} = \frac{V_{bat} - V_{cld}}{L_{bat}}. \tag{20}$$

C. SIDO Mode (Fig. 2(e))

In this mode, PV generation is in excess and supplies power to both the DC bus and the battery system. The active switches for this modes are S_1 and S_4. The state-1 and state-2 of the SISO mode are also valid here for the switch S_1. The switch S_3 is used to control the charging current of the battery. For the switch S_1, the operation of the converter is explained for the following interval.

State-1 ($D_3T < t < 1-D_3T$ & $0 < t < D_1T$): During this interval, the switch S_1 is on and the switch S_3 is off. The L_P stores the energy and the current I_{LP} increases. This interval is similar to the state-1 of the SISO mode.

State-2 ($0 < t < D_3T$ & $t < 1-D_1T$): In this interval, the switch S_1 is off and S_3 is on. The energy absorbed by the primary inductor L_p is used to charge the battery. The following equation explains the operation of the converter in this interval

$$\frac{I_{lb}}{dt} = \frac{V_{bat} - V_{cld}}{L_{bat}}. \tag{21}$$

III. MATHEMATICAL MODELING AND DESIGN CONSIDERATION

To develop a mathematical model for every mode the averaging of the converter in each mode is performed by applying volt-second balance on inductor currents equations and the ampere-second method on all capacitors voltage equations. The steady state analysis results for each mode are elaborated in SISO, DISO, and SIDO modes.

A. SISO Mode

1. *Power transfer from PV to main DC bus*

By applying the volt-second balance on the primary inductor L_p, the voltage across the magnetizing inductor is calculated according to (22), whereas the voltages across the capacitors C_1 and C_2 are computed according to (23) and (24), respectively:

$$V_{Lp} = D_1 \times \frac{V_{pv}}{1-D_1}, \tag{22}$$

$$V_{C_1} = \frac{V_{pv}}{1-D_1}, \tag{23}$$

$$V_{C_2} = (n+2) \times \frac{V_{pv}}{1-D_1}. \tag{24}$$

The steady state voltage across the capacitor C_m is computed by using (25) and the output voltage V_0 across the load is computed by using (26):

$$V_{cld} = V_{pv} + V_{lp} + nV_{lp} + V_{C_2}, \tag{25}$$

$$V_{cld} = \frac{V_{pv} \times (2 + n + D_1(1+n))}{1-D_1}. \tag{26}$$

The converter gain increases significantly by increasing the duty cycle and the turn ratio "*n*" of the coupled inductor. The output voltage increases linearly with the input voltage. The proposed converter has the approximate gain of 8 in the SISO mode.

2. *Power transfer from battery to main DC bus*

Applying volt-second balance on the inductor L_{bat}, the voltage across the battery V_{lbat} and voltage V_{cld} are given as:

$$V_{lbat} = D_2 \times V_{bat} / 1-D_2, \tag{27}$$

$$V_{cld} = V_{bat} / 1-D_2. \tag{28}$$

3. *Battery charging from main DC bus*

The steady state voltage across the battery port is given as

$$V_{bat} = D_4 \times V_{cld}. \tag{29}$$

B. DISO Mode

For this mode, applying volt-second balance on the L_m

(magnetizing inductance), the voltage across the magnetizing inductance is computed by using (30)

$$V_{lm} = \frac{V_{pv} \times (D_1 - D_2) + V_{bat} \times D_2}{1 - D_1}. \quad (30)$$

The voltages V_{C_1} and V_{C_2} across the capacitors C_1 and C_2 are computed by (31) and (34), respectively:

$$V_{c1} = \frac{V_{pv} - D_2 \times V_{pv} + D_2 \times V_{bat}}{1 - D_1}, \quad (31)$$

$$V_{c2} = \frac{V_{pv} \times [1 + nD_1 - D_2(n+2)] + V_{ch}}{1 - D_1}, \quad (32)$$

where, $V_{ch} = V_{bat} \times \left[D_2 (n+1) + n(1 - D_1) \right]$.

The output voltage V_0 across the capacitor C_m is computed by using (33)

$$V_0 = V_{pvnew} \times \frac{V_{pv}(D_1 - D_2) + V_{bat} \times D_2}{1 - D_1}, \quad (33)$$

where, $V_{pvnew} = 2(V_{pv} + n.\, V_{bat} + (2n+2)$.

C. SIDO Mode

In this mode, the only input is from PV. By applying the volt-second balance on the magnetizing inductance L_m, the

$$V_{lp} = \frac{V_{pv} \times D_1}{1 - D_1}. \quad (34)$$

The voltage across the capacitors C_1, C_2, and C_m is calculated by using (31), (32), and (33), respectively.

The output voltage across the battery C_m is calculated by using (35)

$$V_{bat} = \frac{(V_{pv})}{(1 - D_1)}. \quad (35)$$

D. Design Consideration

The design specifications for the proposed converter are given in Table I. The main elements are the coupled inductor, power metal–oxide–semiconductor field-effect transistor (MOSFETS), capacitors, and diodes. The design of the components, all the relationships of SISO mode are considered. The detailed design of each component is discussed below.

1. *Coupled inductor design*

The coupled inductor is the only magnetic component. The required parameters for the inductor design are shown in Table I. The required values of the coupled inductor are $L_p = 5\ uH$ and $L_s = 20\ uH$ for DCM operation. For the CCM operation, inductor's values are $L_p = 25\ uH$ and secondary inductor $L_s = 100\ uH$. The Equivalent inductance is $L_{eq} = L_p + L_s + 2M$, where *M* is the Mutual inductance. In this work, we use the value of "n = *2*". The number of turns for the required inductance value of L_p is calculated by using equation (14). The required peak inductor current is $14\ A$ and the duty cycle $D_1 = 0.49$. For $500\ W$, core ETD-39 and wire AWG-14 are selected. The maximum flux density of the core can be computed by using (36)

$$B_{max} = \frac{U_{eff}.U_0.N_1^2.I_{max}}{L_e}. \quad (36)$$

The peak current I_{Dpk} through diode D_3 is calculated by using (37)

$$I_{Dpk} = \frac{V_0 - [(V_{IN}) \times (2+n) - V_{c2}]}{L_{eq} \times (1 - D_1 T)}. \quad (37)$$

The peak I_{Lpk} primary inductor current is calculated using (38). The peak to peak primary inductor current is $2\Delta I_{LP}$. The relationship between I_{Lpk} and I_{out} is expressed in (38)

$$I_{Lpk} = \frac{I_{out} \times (2 + n + D_1(1+n))}{(1 - D_1)}. \quad (38)$$

Where *N67* material is used and having properties. The parameters are $U_{eff} = 1590$, $A_e = 97.1\ mm^2$, $L_e = 78.8\ mm$, and B_{max} is Maximum flux density. The peak inductor current is defined as:

$$I_{Lpk} = V_{IN} / L_p \times D_1 T, \quad (39)$$

$$I_{out} = I_{Dpk}(1 - D_1)^2. \quad (40)$$

The primary inductance value, the loss in the primary inductor, and the magnetizing inductance are calculated by using (41), (42), and (43), respectively:

$$L_p = \frac{V_{IN}}{(2+n)^2 \times I_{out} \times D_1(1 - D_1)T}, \quad (41)$$

$$L_{Ploss} = R_{ESR} \times \left(\frac{(n+1)}{(1 - D_1)} \times I_{out}\right)^2, \quad (42)$$

$$L_m = \frac{n \times D_1 \times V_{in}}{f_s \times \Delta i_{lp}}. \quad (43)$$

The secondary inductor value is calculated by using the relationship $L_S = n^2.L_p$, where n = $N_1 / N_2 = \sqrt{(L_1 / L_2)}$ for N_1 to be the number of turns in the primary and N_2 to be the number of turns in the secondary. The coupling coefficient between the primary and secondary inductors is calculated by using (44)

$$k = \frac{M}{\sqrt{L_p \times L_s}}. \quad (44)$$

Loss in secondary inductor is calculated by (45)

$$L_{Sloss} = R_{ESR} \times (\frac{(n+1)}{(1-D_1)} \times I_{out})^2. \quad (45)$$

The leakage inductance value in the primary side can be calculated by (46)

$$L_{lk} = 1/(2.\pi f_r)^2 \times C_{outs1}, \quad (46)$$

where f_r is the resonance frequency and C_{outs1} is the output capacitance of the switch S_1.

TABLE I. PARAMETERS USED FOR SIMUALTION AND PROTOTYPE.

Parameter's Name	Symbols	Values
Input Source-1	V_{pv}	$48\,V$
Input Source-2	V_{bat}	$96\,V$
Output Voltage	V_0	$380\,V$
Primary Inductance	L_P	$25\,uH$
Secondary Inductance	L_S	$100\,uH$
Load Current	I_{load}	$1.319A$
Load Resistor	R_{load}	$288\,\Omega$
Frequency	f_s	$100\,kHz$
Output Power	P_0	$500\,W$

The finite element model of the coupled inductor is developed in Ansys Maxwell. The coupled inductor Ansys analysis report for CCM operation is shown in Table II, where complete details of the coupled inductor performance indicators are discussed in detail. The FEM of the coupled inductor for the magnetic flux density and magnetic flux lines are shown in Fig. 4.

2. *Capacitors' selection*

Three capacitors used in this topology are i) the clamping capacitor C_1, ii) the switched capacitor C_2, and iii) DC link capacitor C_m. The relationship between the clamp capacitor C_m and the input voltage V_{bat} is expressed in (47)

$$V_{C_1} = \frac{V_{bat}}{1-D_1}. \quad (47)$$

The blocking voltage across the switch S_1 is expressed in (48)

$$V_{DS1} = \frac{V_{bat}}{1-D_1}. \quad (48)$$

The minimum value of the capacitors C_1 and C_2 is computed by using equation (48) and (49), respectively:

$$C_{1min} >= \frac{V_{bat} \times D_1.T}{2 \times R_{dson1} \times \Delta V_{C_1}}, \quad (49)$$

$$C_{2min} >= \frac{V_{c1} \times D_1.T}{2 \times R_{dson1} \times \Delta V_{C_2}}. \quad (50)$$

Similarly, the voltage across the capacitor C_2 and the value of the output capacitor C_m are calculated by using (50) and (51), respectively:

$$V_{C_2} = \frac{V_{IN} \times (-1+2.D_1+2+n)(1+n(1-D_1))}{(1-D_1)}, \quad (51)$$

$$C_m >= \frac{V_{IN} \times D_1 \times T}{2 \times R_{load} \times \Delta V_{cm}}. \quad (52)$$

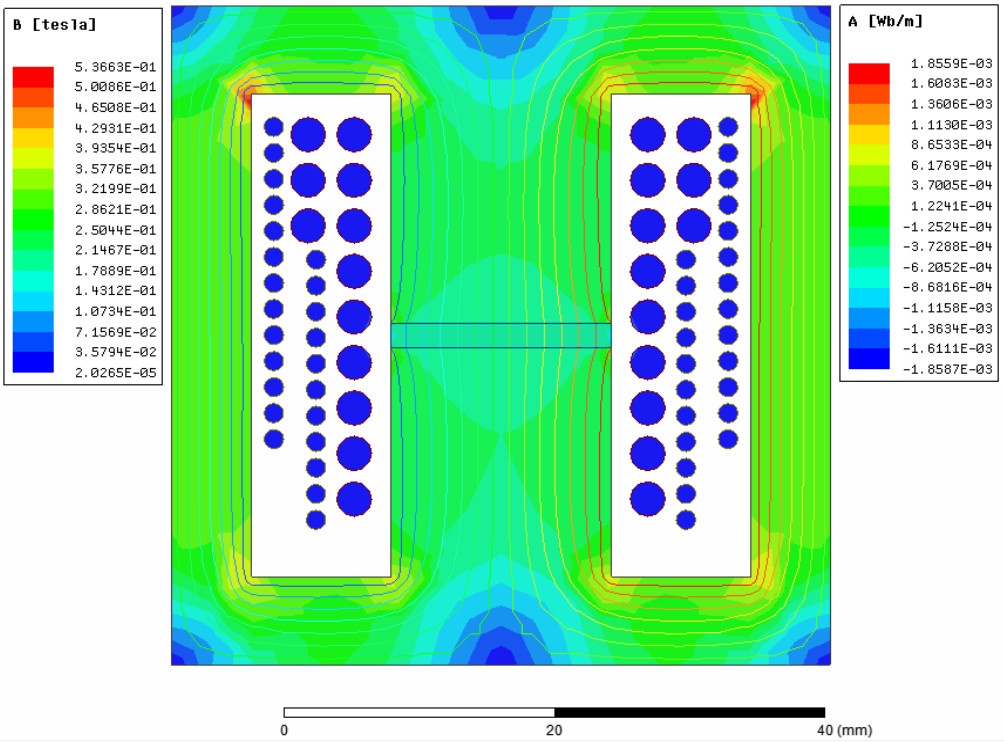


Fig. 4. Magnetic flux line and magnetic flux density (FEA).

TABLE II. ANSYS MAXWELL ANALYSIS REPORT OF COUPLED INDUCTOR.

	Primary Inductor (L_p)	**Secondary Inductor** (L_s)
Current Density	2.88 A/mm^2	1.22 A/mm^2
Inductance	25.00 uH	100.043 uH
Losses	815.77 mW	119.917 mW
R_{dc}	3.353 $m\Omega$	29.379 $m\Omega$
Losses		
Losses (Winding)	200.684 mW	
Losses (Core)	971.142 mW	
Total Losses	1.172 W	
Window Occupancy		
Window Filling (%)	31.09	55.72

3. *Switches and diodes*

The switches S_1, S_2, and S_4 have low blocking voltage capability, while switch S_3 has high voltage blocking capability. The maximum voltage stress across the main switch S_1 is calculated by (31). The fast recovery diode is chosen for D_c, whereas, for D_{ch}, ultrafast recovery diode is used. The D_{pv} and D_b are the ordinary rectifier diodes with required current and voltage blocking capability. The details of the components rating used for the simulation and prototype are given in the Table I.

IV. RESULTS AND DISCUSSION

In order to investigate the performance of proposed converter and theoretical analysis, a simulation model of 500 W converter is developed in PLECS/MATLAB. The proposed converter has high gain in SISO, DISO, and SIDO modes. The complete, simulated, and experimental results for SISO, DISO, and SIDO modes are presented. Main parts of the converter are common to all the ports. The parameters of various components used in simulation model are given in Table I. As the converter has only one coupled inductor, the turns ratio n can be increased by keeping the duty cycle constant in order to increase the gain of the converter. The simulation results and experimental results are explained in the following subsections.

A. Simulation Results

The PLECS simulation results in SISO mode are shown in in Fig. 5.

The waveforms of control signal V_{GS1} and the currents i_{lk}, i_{LS}, and I_{LM} of the proposed converter in SISO mode are plotted. The duty cycle of V_{GS1} is $D_1 = 0.49$. The ripples in the magnetizing current are approximately 40 %, which can be reduced by increasing the magnetizing inductance value of the coupled inductor. The peak current flowing through the primary inductor L_P is 31 A. The current i_{LS} increases with the slope of $V_{C_1}/n \times L_P$ during the on state of the switch S_1, while the current i_{dc2} increases linearly. When the switch S_1 is off, the current i_{dc} increases abruptly and reaches the value of the 31 A, and then decreases quickly. The ripples in the output voltage V_0 are approximately 20 mV.

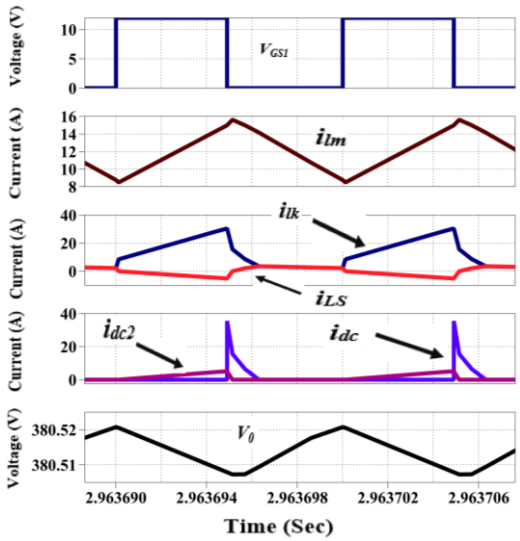


Fig. 5. SISO mode results.

The steady state simulation results for the converter in DISO mode are shown in Fig. 6.

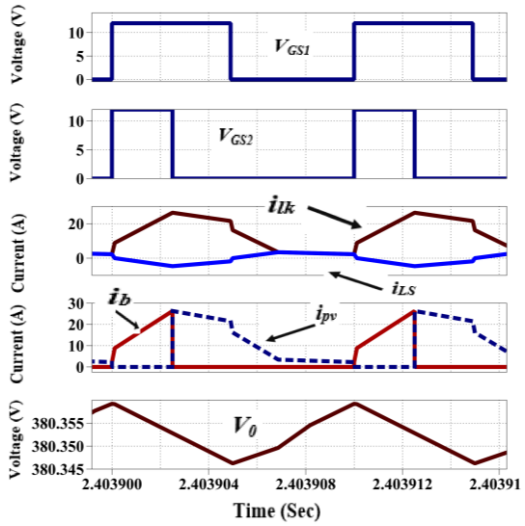


Fig. 6. DISO mode results.

The duty ratio of V_{GS1} and V_{GS2} are $D_1 = 0.49$, and $D_2 = 0.25$, respectively. When S_1 and S_2 are on, the current i_{lk} increases linearly. During on to off transition of V_{GS2}, the current i_b approaches to zero, while the current i_{pv} increases abruptly and follow the current i_{lk}. It is observed that the waveforms match the theoretical results of Fig. 2 and inductor current is continuous. In this mode, the current i_{lk} is maintained as current i_{pv} reaches the value of i_b as soon as the gate pulse V_{GS2} disappears. The output voltage V_0 across the capacitor C_m is regulated at 380 V. It can be seen that output voltage ripple is 15 mV, which is very little. The simulation results for the SIDO mode of operation are shown in Fig. 7. The results are in close comparison with the theoretical results. The control signal

V_{GS3} is used to control the charging current of the battery.

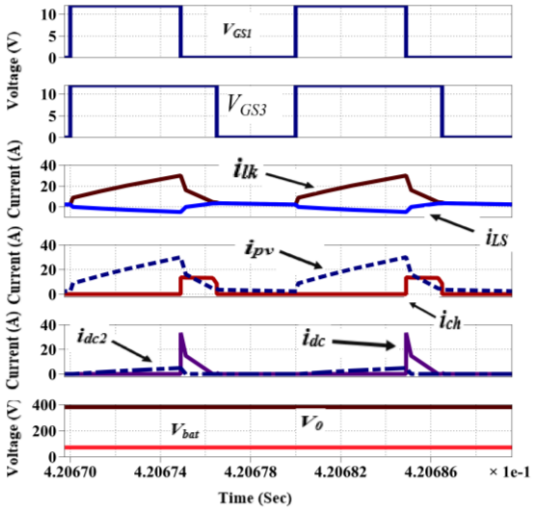
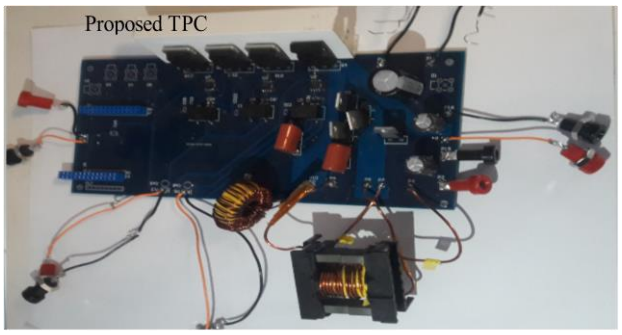


Fig. 7. SIDO Mode Results.

B. Experimental Results

To validate the theatrical and simulation results, a laboratory prototype is developed and tested. The converter prototype is designed for a power level of 500 W. A photograph of the prototype and laboratory are shown in Fig. 8. The laboratory is equipped with Power supplies, oscilloscope, driving modules, millimeters, and controllers. A four layer printed circuit board (PCB) is developed by using Altium designer with one power plan and one segmented ground plan. In the design of the PCB, the number of controlled interfaces is reduced. This reduces the common mode voltage between the interface ports, so that there is less coupling from the cables into or out of the system. In order to minimize the return current path impedance, the return current path is kept closer to the signal path. "Moats" in PCB ground plan are avoided. All power and ground rails are carefully checked to ensure that they do not offer common impedance routs within or outside the unit. The parameters and specifications of various components used in hardware prototype are given in Table I. For the generation of control signals, TI Launchpad-F28379D is used. The instruments used for measurements are: GDS-810C/Rigol oscilloscope, GDS-2A4S1 driving module, intelliSENS probes, the HOKIE current probes, and multimeter.



(a)

(b)

Fig. 8. Hardware prototype (a) and laboratory photograph (b).

The experimental results for the SISO, DISO, and SIDO modes are shown in Fig. 9, Fig. 10, and Fig. 11, respectively. All the results are in close comparison with the simulation and theoretical results.

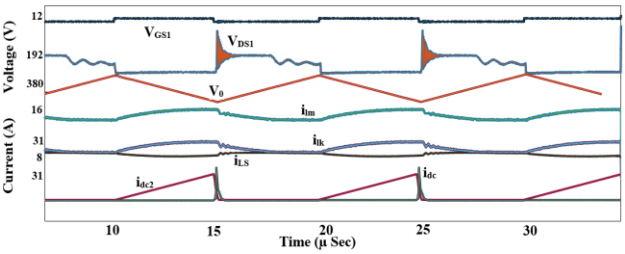


Fig. 9. Experimental Results in SISO Mode.

In Fig. 9, the control signal V_{GS1} and the block voltage V_{ds1} of the switch S_1 are shown. The ripples in the blocking voltage are due to the leakage inductance of the coupled inductor. The currents I_{dc2} and I_{dc} flowing through the diodes D_{sb} and D_s, respectively, has smooth transition. The diode D_s is Schottky diode and always conduct when the voltage across the switch exceeded the $2V_{IN}$. The experimental results for the DISO mode are shown in Fig. 10.

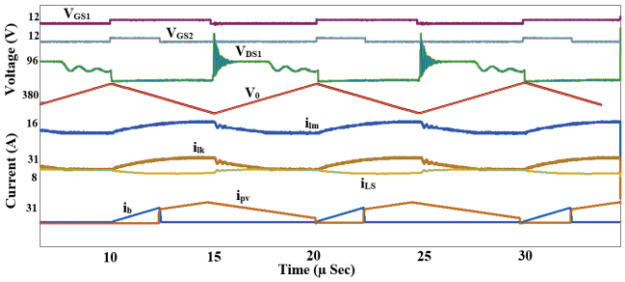


Fig. 10. Experimental Results in DISO Mode.

The control signals are V_{GS1} and V_{GS2}. In this, the both legs of the converter work indecently keeping the output voltage V_0 at the desired voltage. Figure 11 shows the SIDO mode results of the converter. The control signals V_{GS1} and V_{GS3} along with other currents and voltage waveforms are shown. The proposed converter has almost achieved zero voltage switching (ZVS) in SISO mode.

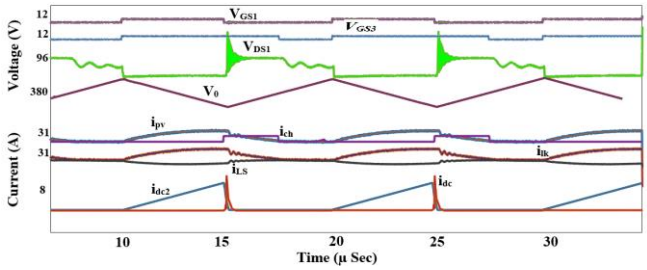


Fig. 11. Experimental results in SIDO mode.

The switch S_1 is main operating switch in this mode, switch S_1 is operated under the zero voltage condition without using the extra components. The leakage inductance of the coupled inductor is used to achieve (ZVS). Figure 12 shows V_{GS1} and V_{DS1} of the switch S_1. The Voltage V_{DS1} is zero before the turning on of gate signal V_{GS1}.

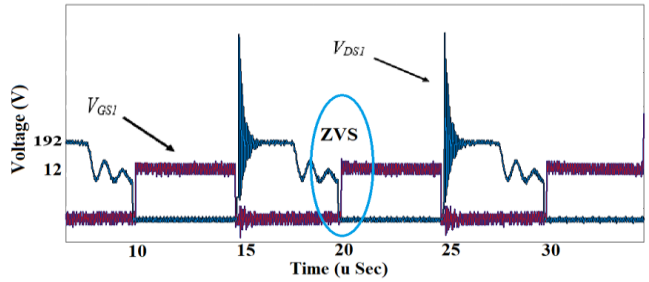


Fig. 12. ZVS condition in SISO mode.

C. Comparative Study

The comparison of the proposed converter in terms of the device count and gain is presented in Table III. The proposed converter is compared with the conventional boost converter, with [13] and [17]. In terms of the overall device count, the conventional boos converter has minimum device count but the gain is much less than the proposed converter. Hence, the proposed converter outperforms its counter parts in overall device count and conversion gain. Figure 13 shows the gain comparison of the proposed converter with the [13], [17], and conventional boost converter.

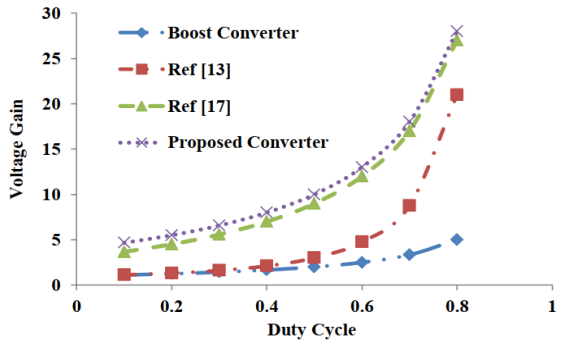


Fig. 13. Voltage gain comparison of the converter in SISO mode.

TABLE III. COMPARISON OF THE PROPOSED CONVERTER.

Converter	Boost	Ref. [13]	Ref. [17]	Proposed
Switches	1	4	4	4
Diodes	1	4	4	4
Capacitors	-	1	8	3
Inductors	1	2	1	2
SISO Voltage Gain	$\frac{1}{1-d}$	$\frac{1+d^2-d}{(1-d)^2}$	$\frac{((n+1)+nd)}{1-d}$	$\frac{(2+n+d_1(1+n))}{1-d_1}$

V. CONCLUSIONS

A three port bidirectional power converter using a coupled inductor and a switched capacitor is proposed. The converter has single conversion stage for each source. The minimum number of the common components makes the converter operation more flexible and simple. This leads to the advantage of less prone to the faults with increased reliability. The higher voltage gain is achieved by using active clamp and switch capacitor technique. The operation of the converter is explained in three different modes, i.e., SISO, DISO, and SIDO. Converter efficiency is calculated and loss analysis is performed using analytic, simulated, and experimental models. The proposed converter has 96 % efficiency in SISO mode. A prototype of 500 W is developed to by using 48 V and 96 V inputs and 380 V output voltage. The measured results of the converter are in closed comparison with simulation results.

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