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Analysis of Non-Uniform Current Distribution in Multi-Fingered and Low-Voltage-Triggered LVTSCR

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Abstract—**Laterally Diffused Metal Oxide Semiconductor Silicon-Controlled Rectifier (LDMOS-SCR) is usually used in Electrostatic Discharge (ESD) protection. LDMOS-SCR discharges current by parasitic SCR, but the MOS in it cannot work when parasitic SCR is stabilized. To further enhance the Electrostatic Discharge (ESD) discharging capability of LDMOS-SCR, a novel high failure current LDMOS-SCR with 12 V operation voltage is fabricated and verified in a 0.18-um high-voltage Bipolar-CMOS-DMOS (BCD) process. Compared with conventional LDMOS-SCR, the novel LDMOS-SCR (LDMOS-SCR-R) introduced a heavily doped p-type region, which is located between the heavily doped n-type and p-type regions of Cathode and is connected with the gate. The adding p-well resistance can drop the voltage on the gate, and the gate with p-well resistance also has resistance and capacitance coupling effect. According to the results of the transmission line pulse test (TLP), the voltage applied to the gate by increasing the p-well resistance plays a major role in the device working mechanism. Under the same device size, LDMOS-SCR-R has higher I_{t2} (8.6 A) than conventional LDMOS (2.21 A) or LDMOS-SCR (6.62 A) in TLP results. Compared with LDMOS-SCR, the failure current of LDMOS-SCR-R increases by 30 %, and the FOM of LDMOS-SCR-R increases by 34 %. The response of LDMOS-SCR-R is also faster than that of LDMOS-SCR under larger current conditions. In addition, the phenomenon in TLP results is consistent with simulation results. The proposed LDMOS-SCR-R can effectively increase failure current without affecting the device's design window, and the additional p-type region will not increase the layout area.**

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Index Terms—**Electrostatic discharge protection; LDMOS-SCR; Device simulation; Dual direction SCR (DDSCR); Failure current.**

I. INTRODUCTION

Electrostatic discharge (ESD) is very common in chip production, transportation, and testing [1]. Lateral Diffused MOS (LDMOS) is a popular structure in High-voltage input/output ESD protection, which is usually used in High-voltage applications, such as automotive electronics, power management in Integrated-circuits, and High-voltage circuit drivers [2]–[4]. The LDMOS devices are discharging ESD current by channel current in gate-biased condition, but the LDMOS has a random and unconstrained failure before reaching its intrinsic limitation, and the multiple fingers will cause a non-uniform turn-on issue [5]. SCR is an effective solution for ESD protection device [6]–[14]. A proving technique to gain the ESD current capability is combining SCR with LDMOS structure (LDMOS-SCR) [15]–[19]. Under ESD stress, the parasitic Bipolar Junction Transistor (BJT) inside the LDMOS turns on and the embedded SCR can work to snapback region stably, hence the LDMOS-SCR can get higher robustness than the LDMOS device stand-alone. However, the improvement of the ESD robustness of LDMOS-SCR is still a problem. One of the concepts is to provide trigger current to turn on parasitic BJT. The authors in [20] proposed a structure, which keeps LDMOS stable in the high-current holding region after snapback for improving ESD robustness [21], [22]. Chen *et al*. [23] proposed a LDMOS-SCR with SUPER-JUNCTION structure, which needs an additional layout mask. In addition, the authors in [24] discuss the change of failure current caused by the change of LDMOS-SCR structure size, and the

larger size, the larger the layout area. In this paper, a novel design is proposed, which can increase the failure current of the LDMOS-SCR device without affecting the design window or increasing the additional mask cost. The proposed LDMOS-SCR can meet the application of 12 V operation voltage, and it has a human body model (HBM) of up to 10 kV to achieve electrostatic discharge robustness.

II. ASYMMETRICAL LDMOS-SCR ESD PROTECTION DEVICE

The cross-sectional view of the conventional LDMOS, the conventional LDMOS-SCR, and the proposed LDMOS-SCR-R devices is shown in Fig. 1(a)–(c). The device sizes of stripe layout devices are 40 (length) × 50 (width) um^2. Compared with the conventional LDMOS-SCR, the LDMOS-SCR-R introduces a heavily p-type region between the heavily p-type and n-type regions of the Cathode, and the introduced heavily p-type is connected with the gate. In order to prevent the gate from being damaged by coupling voltage, the layout rule of the gate also follow the rules of High-voltage gate rule. Two heavily p-type regions in Cathode are equal to the resistance of the gate and ground connection. Due to better heat distribution and a better structure, the LDMOS-SCR-R has a better current discharging capacity. Comparing to adding an resistance and capacitance (RC)-trigger circuit, adding a p-type region hardly needs more layout area.

The equivalent circuit of the conventional laterally-diffused n-type metal-oxide semiconductor (LDNMOS) is given in Fig. 2(a). When the applied ESD voltage is greater than the breakdown voltage of the reverse PN junction, the avalanche breakdown current flowing through *Rpw* will turn on the parasitic NPN and a current discharge path1 will appear. However, the laterally parasitic NPN in LDNMOS may be difficult to turn on in an event of ESD, which has limited influence on current discharging ability of LDNMOS. A higher current discharge capacity requires a better structure. The equivalent circuit of the conventional LDMOS-SCR is given in Fig. 2(b). Path1 appears when the applied ESD voltage is greater than the breakdown voltage of the reverse PN junction. At present, the main current discharge path is path1, and the current flowing through Cathode N+ is greater than the current of Cathode P+. When the applied ESD voltage increases, the current flowing through the Cathode P+ can increase the *Rpw* voltage to 0.7 V, and then the parasitic NPN appears. The NPN will turn on the parasitic PNP, and then the SCR will begin to work and the path2 will appear. Because of the path2 suppresses path1, the main current discharging paths is path2. The working mechanism of path1 is parasitic NPN, and the working mechanism of path2 is parasitic SCR. So, the LDMOS-SCR has better current discharge capacity than LDNMOS.

In an application requiring a higher protection level, the improvement of the protection level of LDMOS-SCR without increasing the layout area still remains a problem. The equivalent circuit of the LDMOS-SCR-R is given in Fig. 2(c). The p-well resistance *Rp* and the Gate capacitance *Cp* can couple voltage on the gate. *Cp* depends on applied ESD voltage, and the gate coupling voltage depends on *Rp* and applied ESD voltage. Path3 appears when the applied ESD voltage is less than the breakdown voltage of the reverse PN junction. However, the resistor *Rp* is too small to couple enough voltage on the gate to turn on the parasitic NPN in NMOS. The trigger mechanism is the avalanche breakdown of NMOS, so the path1 appears. When the device is triggered, the path4 does always exist. The path1 also raises the voltage of *Rpw*. When the voltage drop reaches 0.7 V, the SCR begins to work, and then path2 appears, which also suppresses path1. However, when the discharge current becomes large enough, the coupling voltage generated by path3 and the path4 on the gate will turn on the NMOS. The main current discharge paths are path1 and path2. The different current discharge path in LDMOS-SCR-R makes a higher I_{t2} than LDMOS-SCR.

Also, the holding voltage of SCR depends on the current gains of NPN and PNP. PNP is a low current gain structure. With the change of NPN structure, the current gain will be easily reduced.

The common-base current gain α of NPN can be expressed by the following formula

$$\alpha=\gamma\times\beta^{*}, \tag{1}$$

where γ is the emitter injection efficiency, and β^{*} is the base transmission factor. The emitter injection efficiency γ is shown in (2)

$$\gamma=1-\frac{N_B D_E W_B}{N_E D_B W_E}. \tag{2}$$

In (2), N_E and N_B are the doping concentrations of the emitter region and the base region, D_E and D_B represent the emitter minority carrier diffusion coefficient and base minority carrier diffusion coefficient, W_E and W_B are the emitter effective width and the base effective width. The base transmission factor β^{*} is shown in (3)

$$\beta^{*}=1-\frac{1}{2}\left(W_B / L_B\right)^2. \tag{3}$$

Due to the insertion of P+ region, the base of NPN becomes wider, which makes W_B increase. However, the increase of W_B will decease γ and β^{*}. Therefore, the common-base current gain α of NPN will decrease. According to the (4), it can be seen that the SCR can stay stable when the sum of both α_{PNP} and α_{npn} is one

$$\alpha_{PNP}+\alpha_{npn}=1. \tag{4}$$

It appears that the smaller α_{npn}, the lower holding voltage is. The holding voltage of LDMOS-SCR-R depends on NMOS. At the same time, when the applied voltage is enough to turn on SCR, the coupling voltage on the gate will help SCR work. The holding voltage of LDMOS-SCR-R on the second trigger-point will be smaller than that of LDMOS-SCR.

At the same time, the equivalent circuits of LDMOS-SCR and LDMOS-SCR-R leakage current test are shown in Fig. 3. Leakage current is tested under 12 V, which is the working voltage of protected circuit.

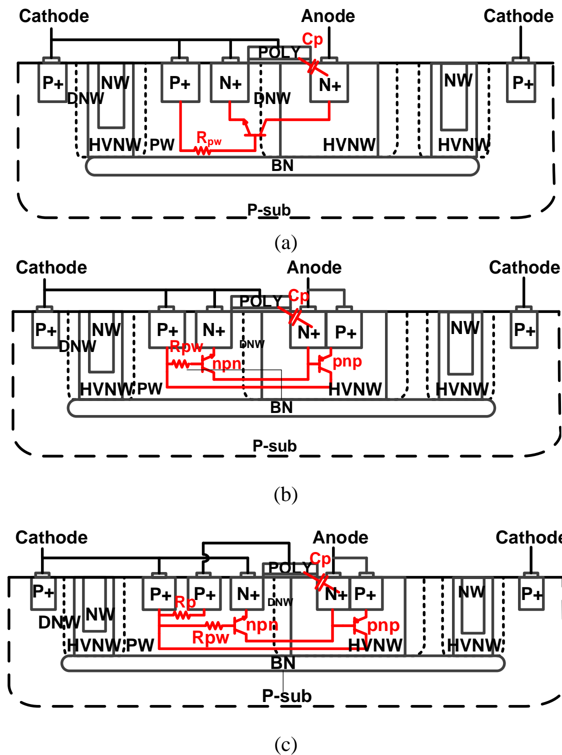

Fig. 1. Cross-section of (a) LDMOS, (b) LDMOS-SCR, and (c) LDMOS-SCR-R.

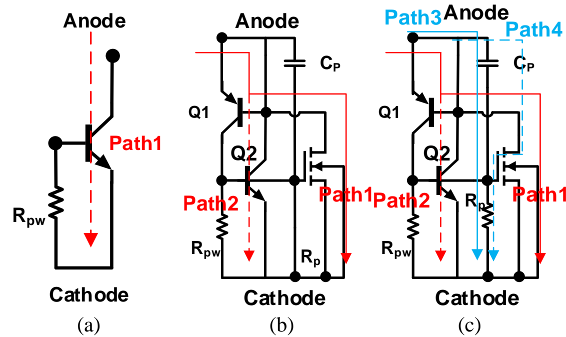

Fig. 2. ESD equivalent circuits of (a) LDMOS, (b) LDMOS-SCR, and (c) LDMOS-SCR-R.

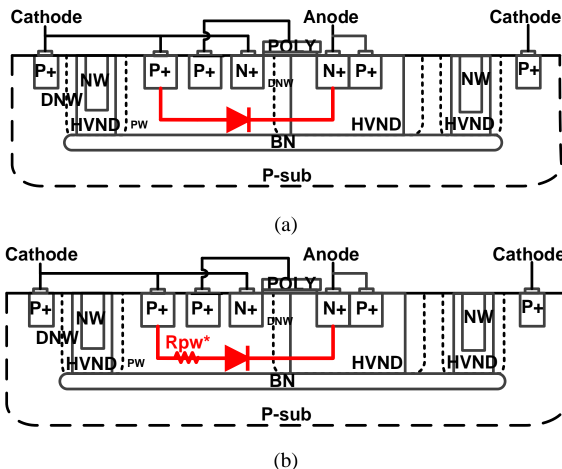

Fig. 3. Equivalent circuits of leakage current test of (a) LDMOS-SCR and (b) LDMOS-SCR-R.

The current path in LDMOS-SCR is a reverse diode, and the current path in LDMOS-SCR-R is a reverse diode and *Rpw**, LDMOS-SCR-R has a larger resistance than LDMOS-SCR. When the applied voltage is 12 V, larger resistance causes a smaller current. The LDMOS-SCR-R will have smaller leakage current than LDMOS-SCR.

III. MATH WORKING PRINCIPLE AND TCAD SIMULATION

The Atlas 2-direction device simulator by Silvaco Corporation is used to verify the operation process of the new structure. The trigger-point and holding-point (see Fig. 4) are simulated in DC simulation, and the simulation ends at 0.03 A, after snapback characteristic appears. Figure 4 shows the current density of LDMOS-SCR (Fig. 4(a)) and LDMOS-SCR-R (Fig. 4(b)) at trigger-point. Because of the same reversed PN junction, LDMOS-SCR and LDMOS-SCR-R have similar triggering characteristics. The reverse PN junction of LDMOS-SCR and LDMOS-SCR-R are both deep N-well and P-well. And we can see that a little current is spread on the inserted heavily p-type region in the red circle, it is inferred that the RC-couple effect has occurred, however, the coupling voltage on *Cp* cannot couple enough voltage on well resistance to control the NMOS into breakdown state. Therefore, avalanche breakdown voltage of LDMOS-SCR-R is similar to that of LDMOS-SCR. The current density of trigger-point can be expressed as it is shown in Table I.

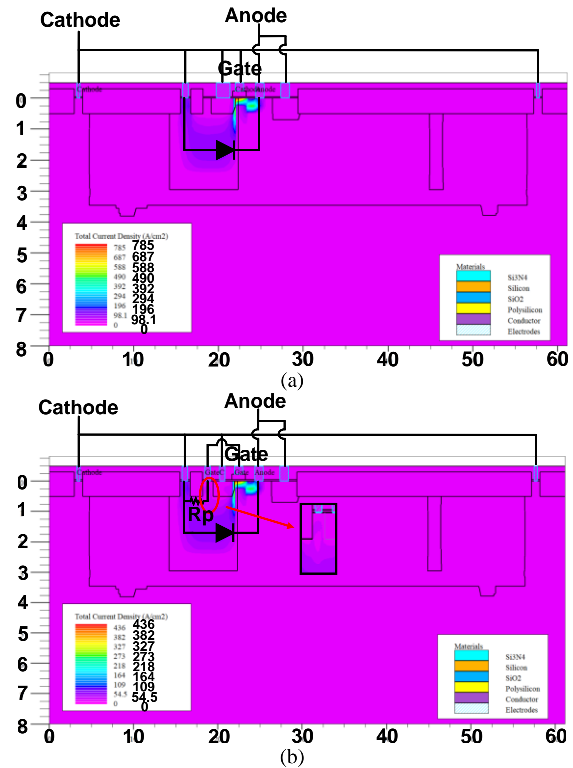

Fig. 4. Current density of trigger-point of (a) LDMOS-SCR and (b) LDMOS-SCR-R.

TABLE I. CURRENT DENSITY OF TRIGGER-POINT.

Device structure	Parasitic structure	Major current path
LDMOS-SCR	DIODE	DIODE
LDMOS-SCR-R	N+ (Anode) to P+ (Cathode)	N+ (Anode) to P+ (Cathode)

Figure 5 shows the current density of LDMOS-SCR (Fig. 5(a)) and LDMOS-SCR-R (Fig. 5(b)) at holding-point. The LDMOS-SCR has holding characteristics similar to that of

LDMOS-SCR-R. When avalanche breakdown occurs, the avalanche breakdown current will flow through *Rpw*. The voltage on *Rpw* can turn on the parasitic NPN, and the NPN can enter the current amplifying region. Although there are a few currents, which are flowing through P+ in Anode and N-buried, the parasitic NPN is the main current discharging path. The unformed SCR cannot work on holding voltage, which depends on parasitic NPN. Therefore, the LDMOS-SCR-R has same holding voltage as the LDMOS-SCR. The current density of trigger-point can be expressed as it is shown in Table II.

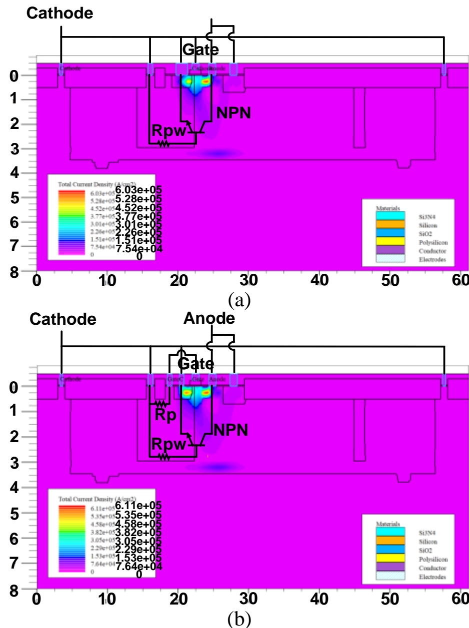

Fig. 5. Current density of holding-point of (a) LDMOS-SCR and (b) LDMOS-SCR-R.

TABLE II. CURRENT DENSITY OF HOLDING-POINT.

Device structure	Parasitic structure	Major current path
LDMOS-SCR	NMOS	NMOS
LDMOS-SCR-R	N+ (Anode) to N+ (Cathode)	N+ (Anode) to N+ (Cathode)

The Fig. 6, Fig. 7, and Fig. 8 are simulations in transient simulation, and the simulation ends at 0.1 A. The simulation shows the current density of the SCR path of LDMOS-SCR (Fig. 6(a)) and LDMOS-SCR-R (Fig. 6 (b)). It can be seen that when the applied ESD voltage increases to 2.06×10^5 A/cm^2, the current flowing through Cathode P+ can increase the *Rpw* voltage to 0.7 V, and then the parasitic NPN appears. The NPN will turn on the parasitic PNP, then the SCR begins to work. The current density phenomenon shows that current flows through the deep path. Now, the main current path is occurred from Anode's heavily p-type region to Cathode's heavily n-type region, because they have a higher current density and its main current discharging path is SCR. The only SCR work on discharge current. The current density of the SCR path can be expressed in Table III.

When applied ESD voltage increases to 7.02×10^5 A/cm^2 in Fig. 7, the channel of NMOS in Fig. 7(a) and Fig. 7(b) both appear current. However, the main current discharging path is still SCR, the unformed MOS path is defined as NPN* (marked with a dotted line). The channel current of NMOS in Fig. 7(a) and Fig. 7(b) show that the LDMOS-SCR-R has RC-effect, and the gate coupling voltage drives more current to flow through the MOS channel. Because of the current density of P+ connected to the gate is too small, it does not appear, but exists. The current density of the SCR path and unformed MOS path can be expressed as it is shown in Table IV.

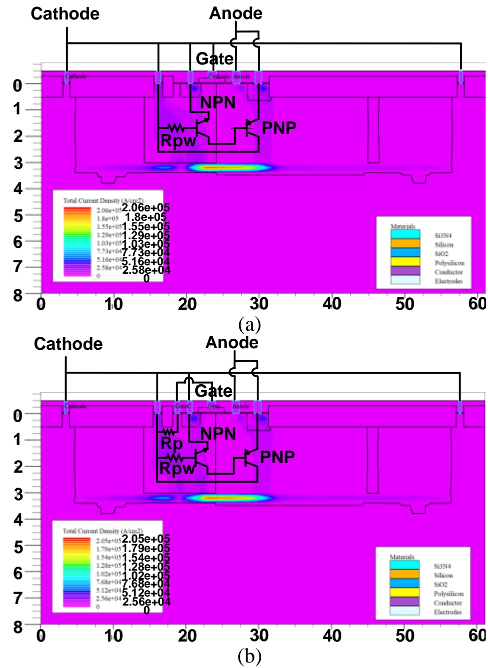

Fig. 6. Current density of SCR path of (a) LDMOS-SCR and (b) LDMOS-SCR-R.

TABLE III. CURRENT DENSITY OF SCR PATH.

Device structure	Parasitic structure	Major current Path
LDMOS-SCR	SCR	SCR
LDMOS-SCR-R	P+ (Anode) to N+ (Cathode)	P+ (Anode) to N+ (Cathode)

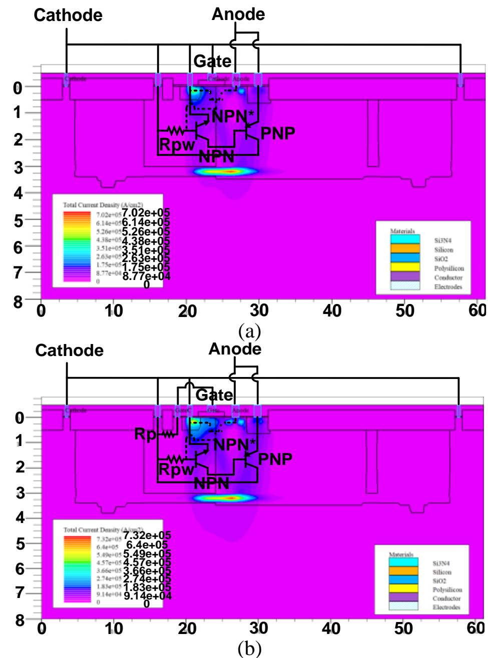

Fig. 7. Current density of SCR path and unformed MOS path of (a) LDMOS-SCR and (b) LDMOS-SCR-R.

TABLE IV. CURRENT DENSITY OF SCR PATH AND UNFORMED MOS PATH.

Device structure	Parasitic structure	Major current path
LDMOS-SCR	SCR	SCR
LDMOS-SCR-R	P+ (Anode) to N+ (Cathode)	P+ (Anode) to N+ (Cathode)

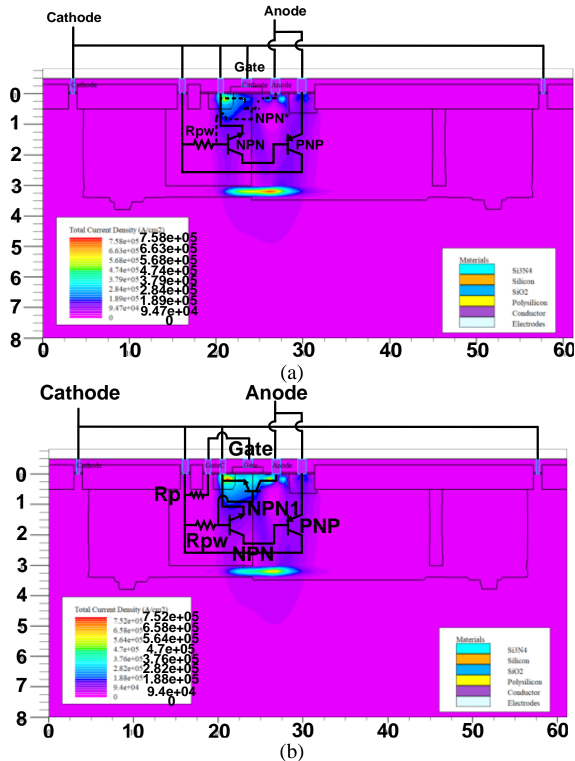

Fig. 8. Current density of SCR path and MOS path of (a) LDMOS-SCR and (b) LDMOS-SCR-R.

When applied ESD voltage is increased to 7.58×10^5 A/cm^2 in Fig. 7, the coupling voltage generated by *Rp* on the gate can turn on the NMOS. So, the main current discharge path is NPN1 and SCR (Fig. 8(b)). Both LDMOS-SCR and LDMOS-SCR-R discharge current by SCR when the current is enough to turn on the parasitic SCR. The difference between them is that, due to the adding p-well resistance, the current-generated voltage and the RC-couple effect can couple a higher voltage on *Rp* to control the gate of NMOS, and the electronics will be attracted to the channel of NMOS. There will be more current flowing through the NMOS channel along the surface of device. SCR has a deep current path on discharging current at the same time. NMOS discharges current on the surface of device, while SCR discharges current in a deep path. The current distribution in the device will be more uniform, and the heat distribution in the device will be more uniform. It indicates that the new structure has better current discharge capacity. The current density of the SCR path and MOS path can be expressed as it is shown in Table V.

TABLE V. CURRENT DENSITY OF SCR PATH AND MOS PATH.

Device structure	Parasitic structure	Major current path
LDMOS-SCR	SCR + NPN*	SCR + NPN
LDMOS-SCR-R	P+ (Anode) to N+ (Cathode)	P+ (Anode) to N+ (Cathode)

IV. EXPERIMENTAL RESULTS AND DISCUSSION

With Hanwa HED-T5000 TLP Test System, the transmission line pulse (TLP) *I-V* characteristics of LDMOS, LDMOS-SCR, and LDMOS-SCR-R are investigated. The rise time of 10 ns and width of 100 ns current pulse was supplied to the device. After a TLP pulse, the leakage current will be tested under 12 V working voltage. The Fig. 9 is the chip photo of LDMOS (Fig. 9(a)), LDMOS-SCR (Fig. 9(b)) and LDMOS-SCR-R (Fig. 9(c)). The Fig. 10 shows TLP curves of three different structures. The results show that the three different devices have the same trigger voltage, same holding voltage, and different failure current. The detailed data are listed in Table VI.

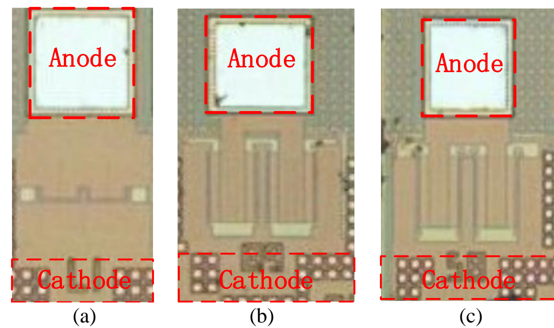

Fig. 9. The Chip photograph of (a) LDMOS, (b) LDMOS-SCR, and (c) LDMOS-SCR-R.

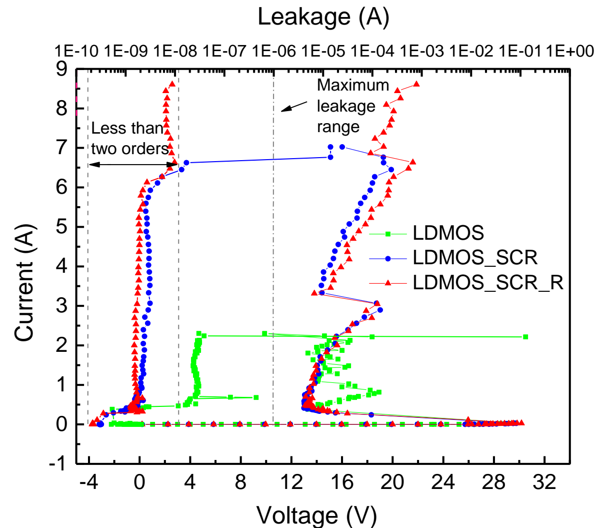

Fig. 10. TLP *I-V* curves of LDMOS, LDMOS-SCR, and LDMOS-SCR-R.

TABLE VI. COMPARISON OF ESD PERFORMANCE OF DIFFERENT STRUCTURE DEVICE.

Device name	V_{t1} (V)	I_{t1} (A)	V_h (V)	I_{t2} (A)	V_{t2} (V)	FOM (mA/μm)
LDMOS	29.72	0.036	13.3	2.21	7.42	4.95
LDMOS-SCR	29.6	0.033	13.02	6.62	19.27	14.56
LDMOS-SCR-R	30.18	0.029	13.7	8.6	21.88	19.52

The LDMOS is a standard comparison device, which is supplied by the factory. The proposed device size and the breakdown voltage are based on this. In this process, when the LDMOS is turned on, the current of LDMOS will become larger than its reverse cut-off state. Therefore, the leakage current suddenly increases when the three structures are

turned on.

The LDMOS, LDMOS-SCR, and LDMOS-SCR-R have the same breakdown voltage, which is triggered by the NMOS's reverse PN junction. While RC-effect in LDMOS-SCR-R has little effects on breakdown voltage, they have almost the same avalanche breakdown voltage. The zap voltages of the trigger voltage of the three structures are 15.1 V (LDMOS), 16.1 V (LDMOS-SCR), and 16.1 V (LDMOS-SCR-R).

The LDMOS-SCR and LDMOS-SCR-R have a second triggering phenomenon (see Fig. 10) when the current reaches about 3 A. The NMOS is easy to turn on, so the main current flows through the channel under NMOS, and the other current flows through the heavily p-type region of Cathode, but the voltage drop on parasitic NPN's *Rpw* is not enough to turn on the positive feedback of SCR. With the increase of current, the voltage drop on *Rpw* reaches 0.7 V and the parasitic SCR appears, so the negative resistance phenomenon makes the Ron of *I-V* curve of LDMOS-SCR-R smaller. That is why the *I-V* curve of LDMOS-SCR and LDMOS-SCR-R has a second trigger phenomenon. And when the current reaches about 6.5 A, the RC-effect on LDMOS-SCR-R enhances the current discharge capability of NMOS. The LDMOS-SCR-R still works when the LDMOS-SCR fails. The parallel resistance of NMOS turned on also has an effect on the Ron of the device.

Zap voltage and time curves of LDMOS-SCR and LDMOS-SCR-R are shown in Fig. 11. Red dot line is the second trigger-point of LDMOS-SCR, black dot line is the second trigger-point of LDMOS-SCR-R, the red line is the third trigger-point of LDMOS-SCR and the black line is the third trigger-point LDMOS-SCR-R. At the second trigger-point of LDMOS-SCR and LDMOS-SCR-R, the zap voltage and time curves are complete overlap. At the third trigger-point of LDMOS-SCR and LDMOS-SCR-R, the LDMOS-SCR-R has faster response than LDMOS-SCR, the current which flows through the adding p-well resistance will drop the voltage on the gate. The voltage coupled on the gate will affect the working mechanism of LDMOS-SCR-R.

The leakage current in Fig. 10 shows that the leakage current of LDMOS-SCR-R is less than that of LDMOS-SCR. Figure 11 shows that at the third trigger-point, LDMOS-SCR-R has faster response speed than LDMOS-SCR at a higher zap voltage. This is the difference between LDMOS-SCR-R and additional RC circuit.

The failure assessment criteria are as follows. The first one is that the maximum leakage current is less than 10^{-6} A. The second one is that the leakage current increases by no more than three orders of magnitude, and the third one is that the *I-V* curve of the device has not changed. The I_{t2} of the three structures are obeying three failure criterions.

The I_{t2} and V_{t2} in Table VI mean that the LDMOS-SCR-R have the best robustness among three structures. The current handling capacity is in line with the trend we expected. The value of LDMOS-SCR-R at 21.88 V is 8.6 A, which is 2 A larger than that of LDMOS-SCR 6.62 A at 19.27 V, and compared with LDMOS-SCR, the failure current of LDMOS-SCR-R has increased by 30 %.

It should be noted that the current capability of LDMOS-SCR-R is almost the sum of LDMOS and LDMOS-SCR. It is proved that the LDMOS-SCR-R makes the NMOS current turn on when SCR already appears. The Maximum leakage current of LDMOS-SCR-R reaches 8.6 A, which is larger than 10^{-6} A, and the leakage current increases by no more than two orders of magnitude.

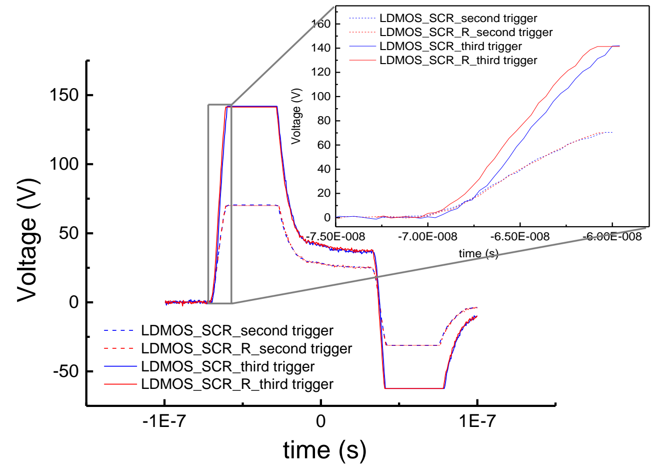

Fig. 11. Zap voltage and time curves of LDMOS-SCR and LDMOS-SCR-R.

To evaluate the ESD protection performance of various ESD devices, the following defined advantages (FOM) are used

$$FOM = \frac{I_{t2} \times V_h}{N \times W \times V_{t1}}. \tag{5}$$

I_{t2} is the failure current, V_h is the holding voltage, W is the width of the device, N is the finger number of the device, and V_{t1} is the trigger voltage. LDMOS-SCR-R has larger FOM than LDMOS-SCR. It also means that the proposed LDMOS-SCR-R has better performance and robustness than LDMOS-SCR, and the FOM of LDMOS-SCR-R is 34 % higher than that of LDMOS-SCR.

V. CONCLUSIONS

A new high robustness Laterally Diffused Metal Oxide Semiconductor Silicon-Controlled Rectifier (LDMOS-SCR) is proposed and realized in 0.18-µm HV BCD process. The propose structure can turn on the suppressed NPN when SCR stays stable. Measured TLP results illustrate that the proposed structure has the same trigger voltage (30.18 V) and holding voltage (13.7 V) than LDMOS-SCR. Under the same device size, the LDMOS-SCR-R has higher I_{t2} (8.6 A) than LDMOS-SCR (6.62 A) in TLP results. Compared with LDMOS-SCR, the failure current of LDMOS-SCR-R increases by 30 %, and the FOM of LDMOS-SCR-R increases by 34 %. The LDMOS-SCR-R also has faster response than LDMOS-SCR when ESD event occurs. The new proposed LDMOS-SCR-R is a simple and effective method, which can increase failure current of LDMOS-SCR and does not need additional mask or layout area to provide application at 12 V operation voltage.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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