Electronically Adjustable Emulator of the Fractional-Order Capacitor

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***Abstract*—This paper presents a design of the controllable emulator of the FOC (Fractional-Order Capacitor) and its application. The circuit is based on 5th-order RC topology (type Foster I), where the passive elements in the topology are replaced by electronically adjustable components. The proposed emulator is based on OTA (Operational Transconductance Amplifier) and VDCC (Voltage Differencing Current Conveyor). The electronically controllable resistors are implemented by OTAs. The electronically tunable capacitors are implemented using capacitance multipliers, which employ VDCCs. The proposed structure provides the electronic control of the order and electronic shifting of the frequency band of the approximation validity. The proposed FOC emulator is also used for fractional-order filter design. The proposed circuits are verified using PSpice simulations.**

***Index Terms*—Fractional-order element; Fractional-order capacitor; Foster I; RC ladder; Fractional-order filter.**

I. INTRODUCTION

The research in the area of fractional-order systems and circuits is an attractive topic for many scientific groups around the world [1], [2]. Compared to the integer-order systems, fractional-order systems can expand the possibilities in designing of different systems in various scientific areas, e.g., in measurement of biological samples [3]–[6], design of control systems [7]–[9], measurement techniques of various signals [10], [11], electronics [12], [13], and agriculture [14].

Recently, many research teams have focused on the design of the FOEs (Fractional-Order Elements) and its use. The FOE represents the non-integer order passive element when the slope of the attenuation of its impedance is $20\times\alpha$ dB/decade, where α is a real number in range $0 < \alpha < 1$ [15]. The phase shift of the FOE is $90\times\alpha$ degrees [15]. The most often designed FOE is FOC (Fractional-Order Capacitor) element with character between a capacitor and resistor [15]–[17]. The resulting impedance of FOC is then given by $Z_{FOC}(\boldsymbol{s}) = 1/(\boldsymbol{s}^{\alpha}\times C_{\alpha})$, where $\boldsymbol{s}$ is Laplacian operator and C_{α} is called as pseudo-capacitance in Farad/sec$^{1-\alpha}$ [17], [18]. Next type of the FOE is FOI (Fractional-Order Inductor), where its impedance is $Z(\boldsymbol{s}) = \boldsymbol{s}^{\alpha}\times L_{\alpha}$, where the L_{α} is called as pseudo-inductance in Henry/sec$^{1-\alpha}$ [19].

FOC is not commercially available element nowadays [16]. However, FOC can be approximated by suitable RC (Resistor-Capacitor) ladder structure with selected parameters. There are several types of the most commonly used RC ladder structures: Foster I, Foster II, Cauer I, and Cauer II [17]. The calculation of the values of resistors and capacitors of the RC structure is based on the selected approximation of the $\boldsymbol{s}^{\alpha}$. The CFE (Continued Fraction Expansion) and Oustaloup´s approximation are most commonly used approximations for the FOC design [8], [17]–[19]. The advantage of this method is easy usage of the proposed RC structures approximating the FOC in any circuit structure (oscillator, filter, etc.) instead of conventional capacitor [20]–[22]. One of the drawbacks of this design method is the limitation of frequency band of the approximation validity, which depends on the number of sections of the proposed RC structure. Another disadvantage is that for each value of α a new RC structure with recalculated values of the passive parts must be arranged.

A design of a novel controllable FOC emulator is introduced in this paper. The FOC emulator is designed based on 5th-order of the RC ladder structure (type Foster I) with Oustaloup's approximation, where the passive parts are replaced with the subcircuits with electronically controllable parameters. The proposed circuit offers electronic control of its order and shifting of the frequency band of the approximation validity without disturbing each other. In comparison with passive FOC, only one structure is used for realization of different values of the order of FOC emulator and approximation types (Oustaloup, CFE, etc.). All passive parts in the topology have a constant value. Another advantage is that the frequency band of the approximation validity can be easily shifted. Only in [19], scientists present similar solutions of the active FOC emulator. In comparison with [18], the circuit presented in this paper provides the FOC order and approximation validity frequency band controlling. The fractional-order low-pass and high-pass

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filters with controllable characteristics are designed using our proposed controllable FOC emulator.

II. PROPERTIES OF USED ACTIVE ELEMENTS

The proposed electronically adjustable FOC (Fractional-Order Capacitor) emulator consists of structure with two types of active elements. The first type of active element is OTA (Operational Transconductance Amplifier) with two voltage inputs and one current output [23]. The schematic symbol of this element is shown in Fig. 1(a). The function of the OTA element is described by the relation $I_{OUT} = g_m \times (V_{IN+} - V_{IN-})$, where the parameter g_m represents the transconductance. If necessary, the number of the current outputs of OTA can be easily extended. The second type of the active element used in FOC emulator is VDCC (Voltage Differencing Current Conveyor) [24]. The schematic symbol and internal block conception are depicted in Fig. 2. It can be seen that VDCC consists of one OTA and CCII+/– (Second Generation Current Conveyor). The relations between VDCC terminals are as follows: $I_Z = g_m \times (V_P - V_N)$, $I_P = I_N = 0$, $V_X = V_Z$, $I_{WP} = -I_{WN} = -I_X$ [24].

The proposed fractional-order filter is designed using one CCTA (Current Conveyor Transconductance Amplifier) [25] and auxiliary DO-CF (Dual-Output Current Follower). The schematic symbol and internal block concept of the CCTA are shown in Fig. 3. It can be seen that CCTA contains one CCII+/– and BOTA (Balanced-Output Transconductance Amplifier). The function of the CCTA is described by the following equations: $I_{OUT+} = -I_{OUT-} = g_m \times V_{Z+}$, $I_Y = 0$, $V_X = V_Y$, and $I_{Z+} = -I_{Z-} = I_X$. [25]. The DO-CF schematic symbol is shown in Fig. 1(b). The function of the DO-CF is described by following equation: $I_{OUT+} = -I_{OUT-} = I_{IN}$.

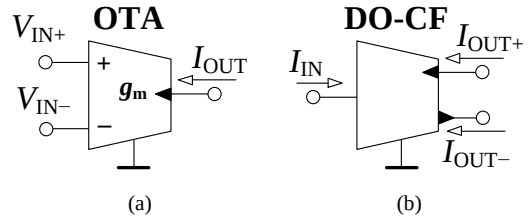


Fig. 1. Schematic symbols: (a) Operational Transconductance Amplifier (OTA); (b) Dual-Output Current Follower (DO-CF).

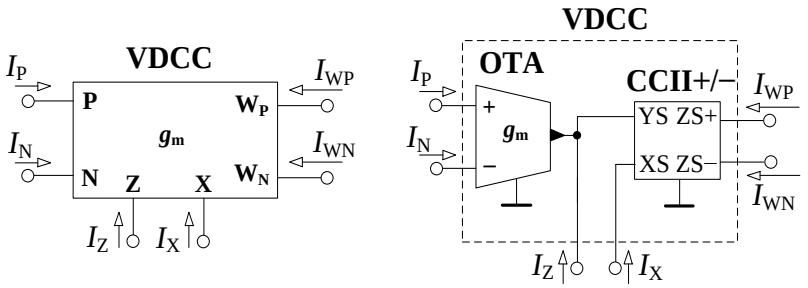


Fig. 2. Voltage Differencing Current Conveyor (VDCC): (a) Schematic symbol; (b) Internal block conception.

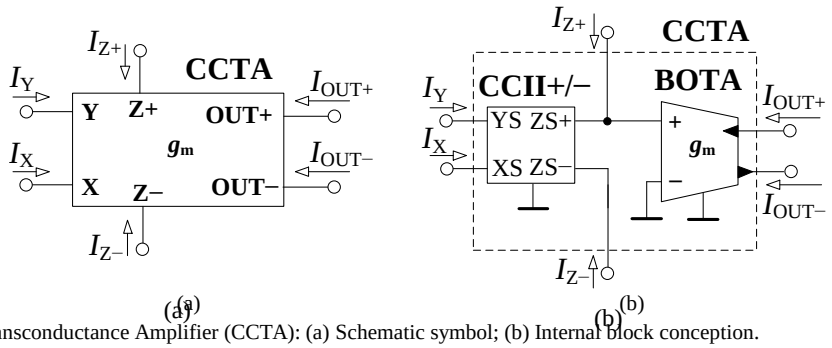


Fig. 3. Current Conveyor Transconductance Amplifier (CCTA): (a) Schematic symbol; (b) Internal block conception.

III. DESIGN OF THE ELECTRONICALLY CONTROLLABLE FOC

The FOC is approximated by 5th-order RC structure in our design. In this case, the Foster I type topology is used with floating resistors and capacitors as is shown in Fig. 4(a). The impedance of the Foster I structure is described by the following equation [18]

$$Z(s) = R_0 + \sum_{i=1}^{5} \frac{\frac{1}{C_i}}{s + \frac{1}{C_i R_i}}. \quad (1)$$

The values of the particular resistors and capacitors were calculated using Oustaloup's approximation (performed in the MATLAB) [8] for the selected values of α, central frequency $f_{CENTRAL}$ ($f_{CENTRAL}$ represents the center of the band, where the approximation is valid), and the frequency band of the approximation validity and equivalent capacitance C_{eq} of the FOC. The equivalent capacitance C_{eq} at the angular frequency ω_0, which is, in this case, equal to $2\times\pi\times f_{CENTRAL}$, is related to the so-called pseudo-capacitance C_α of FOC by the formula $C_\alpha = C_{eq} \times \omega_0^{1-\alpha}$ [18]. The obtained values of the capacitors and resistors from the proposed topology in Fig. 4(a) with five values of α are summarized in Table I.

Figure 4 (b) represents electronically controllable FOC emulator. In the RC structure (see Fig. 4 (a)), the passive parts are replaced by the subcircuits with electronically controllable active elements.

The resistors are replaced by BOTA elements connected as it is shown in Fig. 5 [6]. The value of the equivalent resistor is calculated as follows: $R_{new} = 1/g_{m\_R}$. It is obvious that the value of the resistor is electronically controllable by changing the value of the parameter g_{m_R}.

The capacitors in the RC structure are replaced by the capacitor multipliers that are designed by VDCC [26]. The design of the capacitor multiplier is depicted in Fig. 6. The value of the new capacitor is calculated by: $C_{new} = C \times R \times g_{m\_C}$, where C is original value of capacitance connected to the terminal X of the VDCC, R is auxiliary resistor, and g_{m_C} is transconductance. From the equation, it is observed that the value of the capacitance is electronically controllable by g_{m_C}.

Note that the values of the capacitors C and auxiliary resistors R for all capacitance multipliers in the topology are constant.

TABLE I. VALUES OF THE FOSTER I TYPE RC TOPOLOGY WITH FIVE DIFFERENT VALUES OF ALPHA.

α [-]	0.75	0.6	0.5	0.4	0.25
C_{eq} [nF]	20				
$C\alpha$ [μF/sec$^{1-\alpha}$]	0.32	1.7	5.01	15.1	79.4
R_0 [kΩ]	0.025	0.052	0.08	0.126	0.252
R_1 [kΩ]	0.03	0.059	0.082	0.106	0.129
R_2 [kΩ]	0.136	0.201	0.23	0.243	0.218
R_3 [kΩ]	0.560	0.622	0.59	0.516	0.35
R_4 [kΩ]	2.421	1.986	1.546	1.111	0.564
R_5 [kΩ]	22	9.692	5.431	2.921	1.004
C_1 [nF]	26.6	11.8	7.7	5.5	3.9
C_2 [nF]	36.9	21.8	17.4	15.03	14.6
C_3 [nF]	56.7	44.5	42.8	44.6	57.3
C_4 [nF]	82.75	87.8	102.9	130.7	224
C_5 [nF]	57.5	113.6	184.9	313.6	794.2

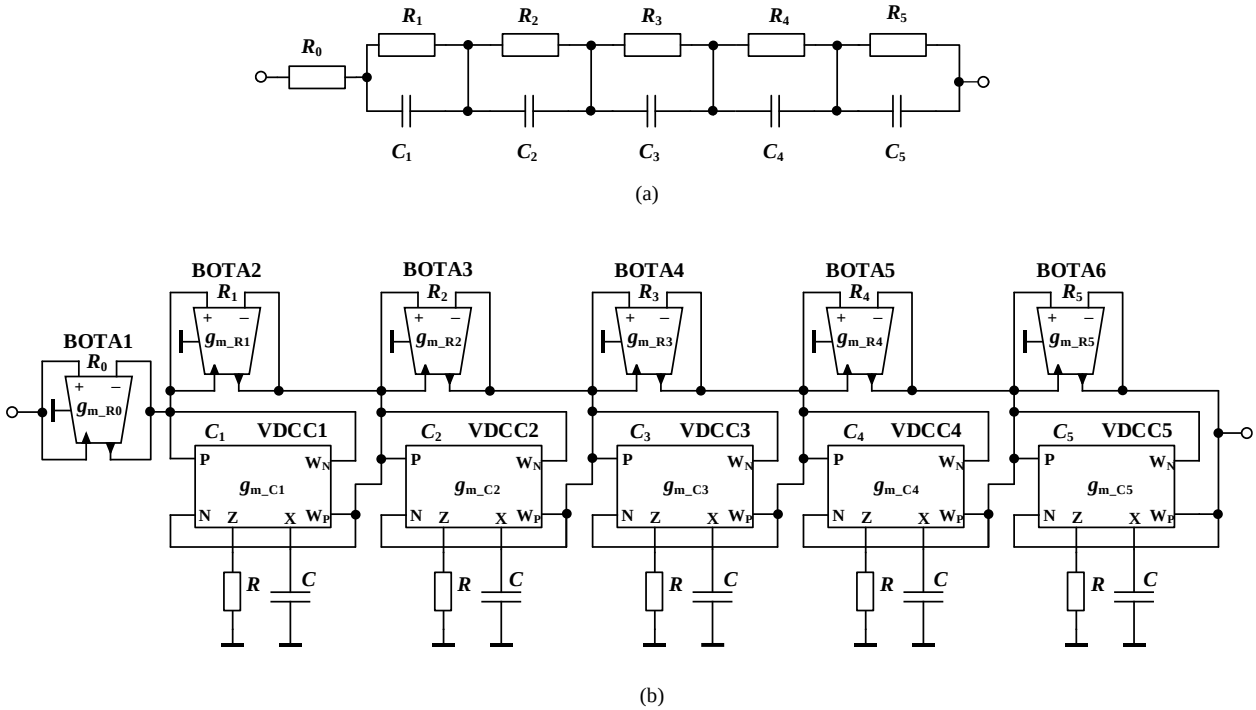


Fig. 4. The 5th-order structures approximating the FOC (Fractional-Order Capacitor): (a) Passive RC topology; (b) Electronically adjustable topology.

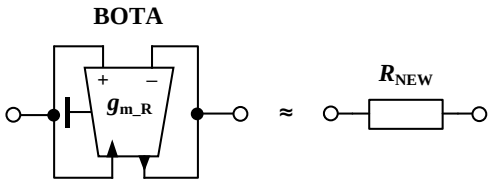


Fig. 5. The electronically controllable floating resistor designed with BOTA (Balanced Output Transconductance Amplifier).

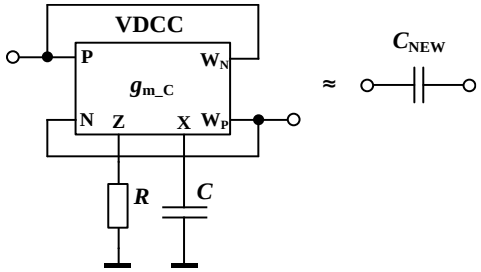


Fig. 6. The electronically adjustable floating capacitor designed by capacitance multiplier that uses the VDCC active element.

The proposed circuit enables control of the order of the FOC α and shift of the frequency band of the approximation validity. The value of α can be changed by adjusting all of the transconductances as in Fig. 4(b) to obtain the resistance and capacitance values according to Table I. The shifting of the frequency band of the approximation validity of the proposed FOC emulator is possible by changing the values of the controllable capacitors. When all the capacitances decreasing k-times, the frequency band shifts to k-times higher values and obviously the central frequency $f_{CENTRAL}$

also increases *k*-times.

IV. SIMULATION RESULTS

The features of the designed controllable FOC were verified in the OrCAD PSpice with behavioral models of the active elements.

The OTA (BOTA) elements are implemented by 3rd-level of the UCC (Universal Current Conveyor) simulation model with external resistor connected to its low impedance terminal X [27]. The value of the resistor represents the value of the transconductance $g_m = 1/R_X$. In case of the resistor emulator implemented by UCC, the new value of resistor is described by $R_{NEW} = 1/g_{m\_R} = R_X$.

The implementation of the VDCC is based on internal block conception previously presented in Fig. 2(b). The OTA is again implemented by UCC [27] active element. The 3rd-level of the simulation model is also used for the implementation of CCII+/–.

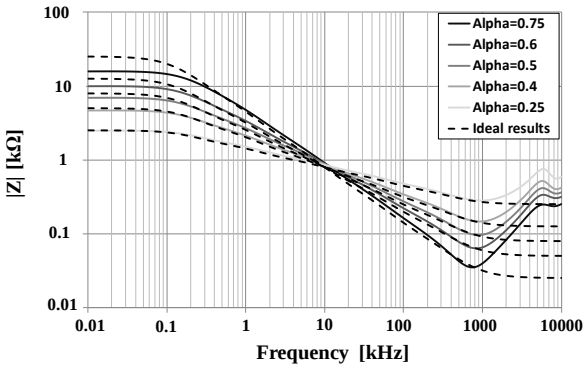
The proposed circuit is simulated with the following values of the parameters: central frequency of the approximation validity frequency band $f_{CENTRAL}$ = 10 kHz, validity of the approximation from 100 Hz to 1 MHz (4 decades theoretically), equivalent capacitance of the FOC C_{eq} = 20 nF, and five values of α from 0.25 to 0.75 (Table II). The values of passive parts of all capacitance multipliers in the 5th-order structure have constant and identical values for all selected α (R = 2 kΩ and C = 20 nF).

Table II summarizes all the values of the particular parts of the proposed controllable FOC for the five values of α. The values are calculated based on the values in Table I and the equations describing resistor emulator and capacitance multiplier as mentioned above. It can be seen that for changing the parameter α, all parameters, except R and C, must be changed.

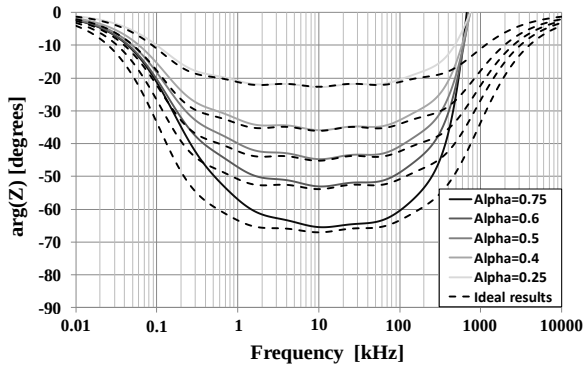
TABLE II. SUMMARIZATION OF THE DESIGNED TOPOLOGY PARAMETERS FOR FIVE VALUES OF ALPHA.

α [-]	0.75	0.6	0.5	0.4	0.25
C [nF]	20				
R [kΩ]	2				
$\|Z\|$ @ $f_{CENTRAL}$ [kΩ]	0.796				
C_{eq} [nF]	20				
C_α [μF/sec$^{1-\alpha}$]	0.32	1.7	5.01	15.1	79.4
$1/g_{m\_R0}$ [kΩ]	0.025	0.052	0.08	0.126	0.252
$1/g_{m\_R1}$ [kΩ]	0.03	0.059	0.082	0.106	0.129
$1/g_{m\_R2}$ [kΩ]	0.136	0.201	0.23	0.243	0.218
$1/g_{m\_R3}$ [kΩ]	0.560	0.622	0.59	0.516	0.35
$1/g_{m\_R4}$ [kΩ]	2.421	1.986	1.546	1.111	0.564
$1/g_{m\_R5}$ [kΩ]	22	9.692	5.431	2.921	1.004
$1/g_{m\_C1}$ [kΩ]	1.5	3.39	5.2	7.27	10.26
$1/g_{m\_C2}$ [kΩ]	1.08	1.83	2.3	2.66	2.75
$1/g_{m\_C3}$ [kΩ]	0.71	0.89	0.94	0.9	0.7
$1/g_{m\_C4}$ [kΩ]	0.48	0.46	0.39	0.31	0.18
$1/g_{m\_C5}$ [kΩ]	0.69	0.35	0.22	0.13	0.05

Figure 7(a) and Figure 7(b) show the obtained non-ideal simulation results (solid lines) of the designed circuit in comparison with ideal results (dashed lines). The values of α obtained from non-ideal simulations based on the magnitude slope values around the central frequency are: 0.72, 0.58, 0.49, 0.39, and 0.247. It is derived that non-ideal results are very close to the ideal ones. The value of the circuit impedance $|Z|$ is 796 Ω at the central frequency for all values of α. From both ideal and non-ideal phase responses, it is obvious that the approximation validity bandwidth decreases for increasing α. The most significant differences can be seen for the results of the FOC with α = 0.75. It is caused by unsuitable values of components with respect to parameters of the used UCC. The differences at high and low frequencies are given by bandwidth limitations and parasitic properties of the used models of the active elements. That also applies for the shifting of the frequency band of the approximation validity.



(a)



(b)

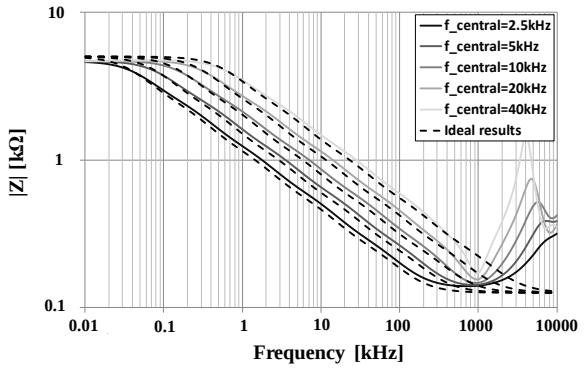
Fig. 7. Simulation results of the proposed controllable FOC for five selected values of α at central frequency 10 kHz: (a) Magnitude responses; (b) Phase responses.

TABLE III. VALUES OF THE DESIGNED CIRCUIT PARAMETERS FOR FREQUENCY CONTROL WITH ALPHA = 0.4.

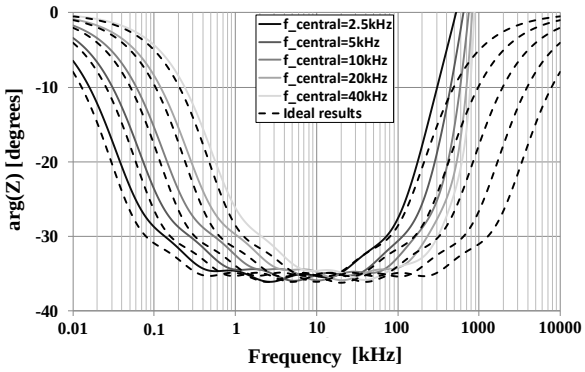
$f_{CENTRAL}$ [kHz]	2.5	5	10	20	40
C [nF]	20				
R [kΩ]	2				
$\|Z\|$ @ $f_{CENTRAL}$ [kΩ]	0.796				
C_{eq} [nF]	20				
C_α [μF/sec$^{1-\alpha}$]	15.1				
$1/g_{m\_C1}$ [kΩ]	1.82	3.63	7.27	14.54	29.09
$1/g_{m\_C2}$ [kΩ]	0.67	1.33	2.66	5.32	10.64
$1/g_{m\_C3}$ [kΩ]	0.23	0.45	0.9	1.8	3.6
$1/g_{m\_C4}$ [kΩ]	0.078	0.16	0.31	0.62	1.24
$1/g_{m\_C5}$ [kΩ]	0.033	0.065	0.13	0.26	0.52

The designed circuit also provides controllability of approximation validity frequency band. It is possible by changing the values of parameters g_{m_C1} to g_{m_C5} of the capacitance multipliers. For demonstration of the frequency

tuning, the circuit with $\alpha = 0.4$ was selected. The circuit was tested for five values of $f_{CENTRAL}$. The used values of the circuit parameters for frequency tuning are summarized in Table III. Figures 8(a) and 8(b) show the magnitude and phase responses of the circuit. Obtained values of $f_{CENTRAL}$ from non-ideal simulation results are: 3.1 kHz, 6.1 kHz, 12 kHz, 24.4 kHz, and 48 kHz.



(a)



(b)

Fig. 8. Tuning of the frequency band of approximation validity of FOC emulator with $\alpha = 0.4$: (a) Magnitude responses; (b) Phase responses.

V. APPLICATION OF THE DESIGNED CIRCUIT IN THE FILTER

As mentioned above, FOC can be used for fractional-order frequency filter design by replacing the conventional capacitor in the structure. The order of the fractional-order filter is described according to the formula $(n + \alpha)$, where n is positive non-zero integer number [20]–[22]. The slope of attenuation of the fractional-order filter is described by the following equation: $20\times(n + \alpha)$ dB/decade.

Figure 9 represents the proposed filtering topology. It consists of one CCTA and one auxiliary DO-CF as active elements, whose properties are described above. In the structure, capacitor C_α is replaced by controllable FOC structure presented above. The proposed filter provides the FLPF (Fractional-Order Low-Pass Filter) and FHPF (Fractional-Order High-Pass Filter) responses.

The general transfer function of FLPF is given by [28]

$$TF_{1+\alpha}(\boldsymbol{s}) = \frac{\frac{\omega_0^{1+\alpha}}{K_1}}{\boldsymbol{s}^{1+\alpha} + \boldsymbol{s}\frac{\omega_0^{\alpha} K_2}{K_1} + \frac{\omega_0^{1+\alpha} K_3}{K_1}}, \quad (2)$$

where $\omega_0 = 2\times\pi\times f_0$ [rad/s] is used for frequency shifting the cut-off frequency to the required value f_0. The values of $K_1 = 1$, $K_2 = 1.008\times\alpha^2 + 0.2867\times\alpha + 0.2366$, and $K_3 = 0.2171\times\alpha + 0.7914$ are adopted from [28]. They are found to obtain maximally flat (Butterworth-like) magnitude frequency characteristic of the filter.

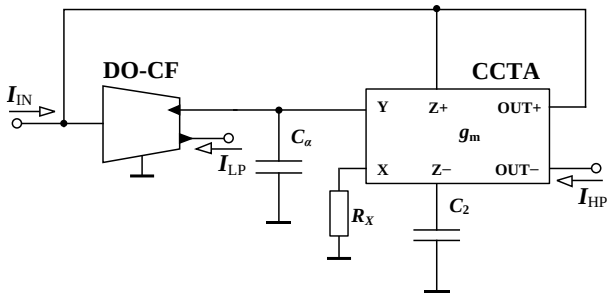


Fig. 9. Topology of the designed filter containing an electronically controllable FOC.

The denominator of the proposed fractional-order filter in terms of circuit elements is given by

$$D = \boldsymbol{s}^{1+\alpha} + \boldsymbol{s}\frac{1}{C_\alpha R_X} + \frac{g_m}{C_\alpha C_2 R_X}. \quad (3)$$

The values of the resistor R_X and transconductance g_m of the proposed filter are calculated by the following equations that stem from the comparison of (3) with denominator of (2):

$$R_X = \frac{K_1}{K_2 \omega_0^{\alpha} C_\alpha}, \quad (4)$$

$$g_m = \frac{K_3 \omega_0 C_2}{K_2}. \quad (5)$$

The PSpice simulations with behavioral models of the active elements were used for verification of the filter features. The DO-CF is implemented by 3rd-level of the CCII+/– simulation model. For CCTA implementation, CCII+/– and BOTA active elements connected as shown in Fig. 3 are used. The BOTA element is implemented as mentioned in Section IV. The simulations of the filter were performed with the following values of the parameters: pole frequency $f_0 = \omega_0/(2\times\pi) = 10$ kHz, equivalent capacitance of FOC at 10 kHz was $C_{eq} = 20$ nF, pseudo-capacitance $C_\alpha = C_{eq}\times\omega_0^{1-\alpha}$, and ordinary capacitor value $C_2 = 20$ nF. The fractional-order filter was tested for three values of the filter order (1.25, 1.5, and 1.75), which is controlled by changing the parameters of the FOC emulator presented in Fig. 4(b). The corresponding values of α are 0.25, 0.5, and 0.75. The used values of the filter parameters are listed in Table IV.

TABLE IV. THE FILTER PARAMETERS FOR ORDER CHANGING.

Theoretical values of the filter order	**1.25**	**1.5**	**1.75**
C_α **[μF/sec$^{1-\alpha}$]**	79.4	5.01	0.32
C_2 **[nF]**	20		
R_X **[kΩ]**	2.14	1.26	0.78
$R_{gm} = 1/g_m$ **[kΩ]**	0.349	0.56	0.85

The magnitude responses of the FLPF and FHPF for three selected values of α are depicted in Fig. 10(a) and Fig. 10(b). The values of the order of the FLPF obtained

from slopes of the non-ideal characteristics in Fig. 10(a) are as follows: 1.23 (slope of attenuation 24.6 dB/decade), 1.47 (slope of attenuation 29.36 dB/decade), and 1.72 (slope of attenuation 34.4 dB/decade). The values of the order of the FHPF (see Fig. 10(b)) from the non-ideal simulations are: 1.247 (slope of attenuation 24.94 dB/decade), 1.48 (slope of attenuation 29.61 dB/decade), and 1.67 (slope of attenuation 33.4 dB/decade). Obtained values are in good agreement with the respective theoretical values 1.25, 1.5, and 1.75. The differences are caused by complexity of the proposed circuit (FOC emulator). The bandwidth limitations of the non-ideal models of the active elements are seen at high frequencies.

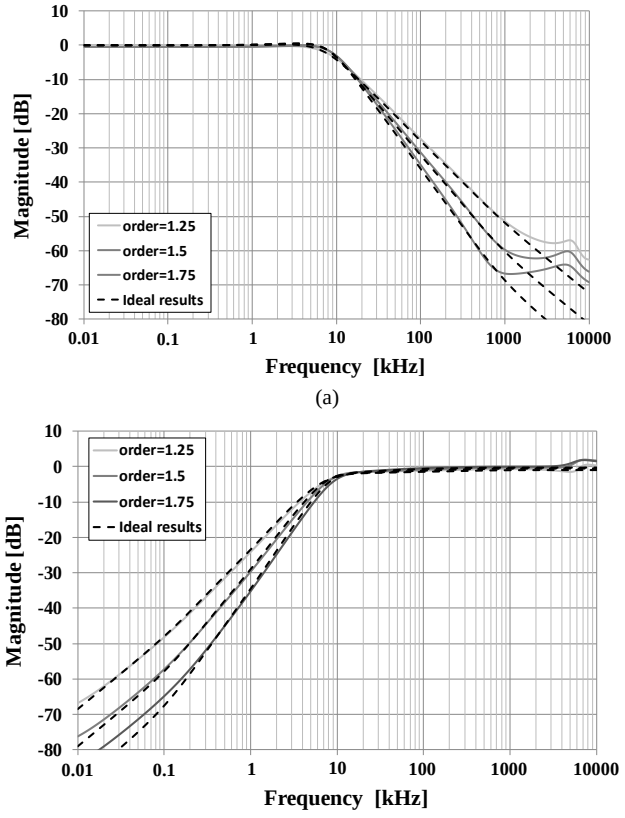


Fig. 10. Simulation results of the designed fractional-order filter with behavioralmodels. Magnitude responses of: (a) FLPF; (b) FHPF for three values of the fractionalorder at frequency f_0 = 10 kHz.

VI. CONCLUSIONS

The design of the controllable fractional-order capacitor (FOC) emulator and its application is presented in this paper. The circuit provides control of the order α and frequency band of the constant phase without disturbing each other. The FLPF and FHPF with controllable order are designed for verification of the FOC emulator function. The proposed filter also provides frequency tuning by changing the values of the R_X and g_m as seen from (4), (5). The frequency tuning of the filter is not included in this paper. Also, the presented study can be extended for other integer-order approximations of the fractional-order capacitive impedance as the Oustaloup's one. The order of the approximation can be varied and other RC topologies than Foster I can be utilized.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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