Minimizing Capacitance Value of Interleaved Power Factor Corrected Boost Converter for Battery Charger in Electric Vehicles

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***Abstract*—A dynamic voltage compensator (DVC) technique is presented for the minimizing of the capacitance value of the interleaved power factor corrected (PFC) boost converter for the battery charger in electric vehicles. This technique is based on eliminating the ripple on the capacitor by creating a voltage in the opposite direction as well as the amount of ripple on the capacitor. With the proposed method, the capacitance value is reduced by approximately five times. Reducing the size of the capacitor also provides the use of film-capacitors with a longer life. The other contribution of this study is designing a faster and more stable fully-digital control system, instead of the commonly used analogue controller of interleaved PFC boost converter. A 3.3 kW interleaved PFC boost converter is designed to verify the effect of the designed dynamic voltage compensator and digital controller.**

***Index Terms*—Dynamic voltage compensator; Electric vehicles; On-board battery chargers; Power factor correction.**

I. INTRODUCTION

The battery chargers play a key role in transferring power from the network to the vehicle at maximum efficiency and in compliance with the standard [1]. In addition to efficient charging, the battery chargers should also have features, such as small size, lower weight, and long service life.

Battery chargers can be designed as onboard and off-board. These topologies are divided into three sub-categories according to the power levels: Level 1 (< 3 kW), Level 2 (3 kW–22 kW), and Level 3 (50 kW >) [2]. Onboard chargers are located in the vehicle while off-board chargers are located in the station. Off-board chargers are known as fast chargers [3]. Compared to onboard and off-board battery chargers, the off-board chargers seem to be superior to the charging time. On the other hand, fast charging is not a healthy solution for Li-ion batteries. Also, since the off-board chargers are available only at stations, the usage of the onboard chargers is inevitable. The most common on-board chargers have two main parts. The first part is a power factor corrected AC-DC converter, which rectifies the input voltage from AC to DC and implements the power factor correction also. The second part is a DC-DC converter, which adjusts the voltage level according to the battery voltage [4]–[6]. The efficiency of the battery charger and its compliance with the standards are largely dependent on the AC-DC converter. Therefore, the selection of this topology is critical in designing the battery charger of the electric vehicles.

The boost PFC converter is a basic structure in all of AC-DC PFC converter topologies. This topology contains diode bridge stage and boost stage. In this topology, a very high ripple occurs at the output capacitor [7]. At the high power levels, the diode bridge heats up and power losses increase. Bridgeless PFC boost converter topology provides the reduction of the total number of the switches from six to four. Therefore, the power losses of the overall system decrease [8]. However, the electromagnetic interference (EMI) value increases due to the input inductor in this topology. In the semi bridgeless converter topology, the total return current flows through the two inductances. So, the total inductance value is twice greater than the traditional boost of the PFC converter [9]. In [10], the H-bridge converter is proposed. Since this topology needs three isolated current sensors, the complexity and cost of the circuit topology are high. The interleaved PFC boost converter consists of a parallel connection of two boost PFC converters. Due to its interleaved structure as illustrated in Fig. 1, this converter greatly reduces both EMI and switching losses compared to the other topologies [11].

High output ripple and controller complexity are the common problems of all PFC topologies. Ripple component of the output voltage affects the performance and size of the system. Reduction of output ripple provides the usage of a smaller size aluminium electrolytic capacitor (E-Caps) of the same type as well as the usage of a film capacitor with a longer life.

A variety of ripple cancellation methods have been proposed in previous studies. In [12], active power filter is

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presented for reduction of the output ripple.

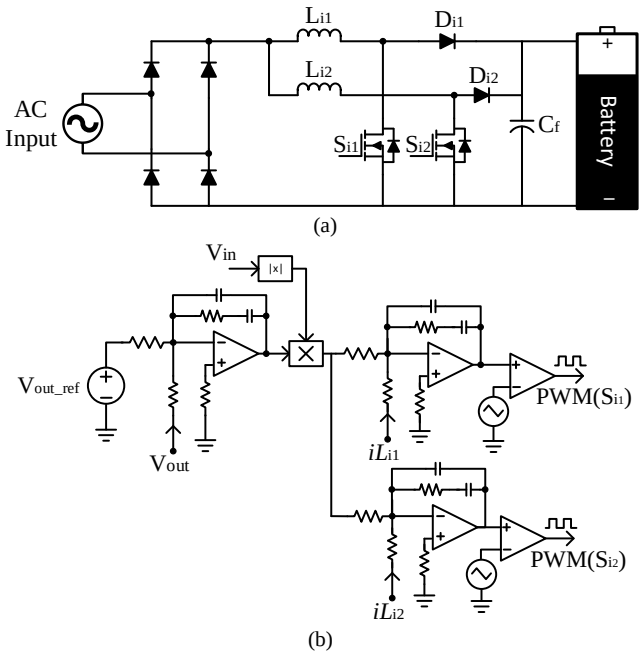

Fig. 1. (a) Circuit diagram of the conventional interleaved PFC boost converter; (b) Analogue controller of the interleaved PFC boost converter.

This concept is based on connecting an extra circuit to the output capacitor. This added circuit creates an impedance on the circuit. The common problem in all these studies is that the elements used in the extra circuit are under high voltage. The high voltage operation of these circuits has a negative effect on the dynamic performance of DC-link. In [13], the authors examine the switching conditions to minimize the current fluctuation of the output capacitor and reduce the fluctuation value by changing the switch states during the fluctuation. In [14], a series voltage compensator technique is presented for the capacitor supported system. In this study, a voltage source is connected between the capacitor and the DC output to reduce the ripple value on the capacitor. The voltage on the capacitor is reduced by this reverse voltage.

This paper presents a dynamic voltage compensator technique, which minimizes the size of the output capacitor used in the interleaved AC-DC converter. DVC circuit is inserted between the output DC-link capacitor and the battery. The DVC circuit operates at a low voltage and has no negative effect on the dynamic behaviour of the DC-link capacitor. Since the added circuit works dynamically, it has positive effects on the behaviour of the controller against sudden load changes. Also, apart from the methods in the literature, the conventional analogue controller of the interleaved PFC boost converter circuit is replaced with a fully-digital controller. Settling time of the converter is greatly reduced with the new controller.

II. SYSTEM ARCHITECTURE

A. Operating Principle of the Proposed Design

Figure 2 illustrates the interleaved PFC boost converter with the proposed dynamic voltage compensator and digital controller. The interleaved PFC boost converter aims to draw minimum of the reactive power from the grid by regulating the input current and voltage to have the same phase. It also applies PWM signals to the converter switches to keep the output voltage at the desired level.

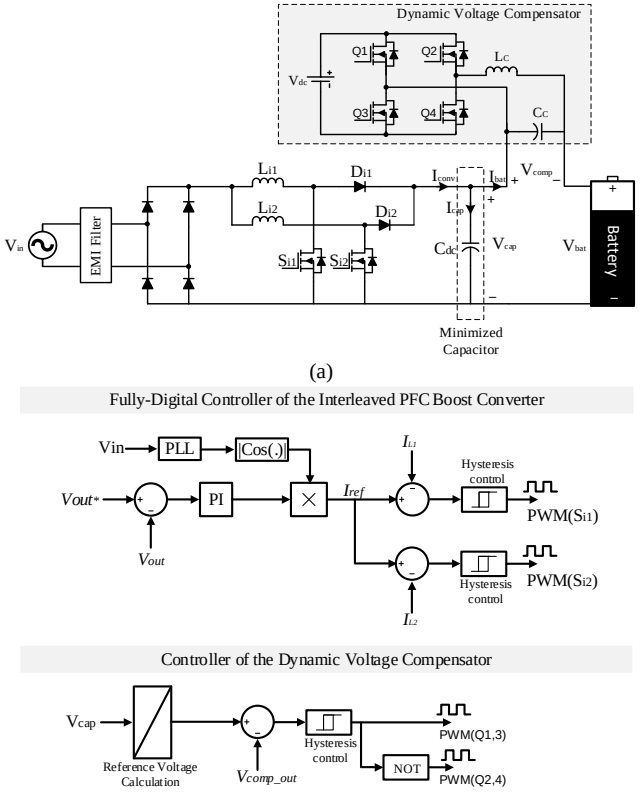

Fig. 2. (a) Circuit diagram of the proposed PFC boost converter with the proposed dynamic voltage compensator; (b) Fully-digital controller of the interleaved PFC boost converter and controller of the dynamic voltage compensator.

The operating regimes are the same for cases where the AC input voltage is positive and negative. The operating regimes of the proposed converter are determined by whether the duty ratio in the positive or negative cycle of the input cycle is greater or smaller than 0.5.

The duty ratio of the switches is calculated as follows

$$D = \left(V_{out} - V_{in}\right) / V_{out}. \tag{1}$$

Figure 3 and Figure 4 illustrate the operating interval circuits of the interleaved PFC boost converter and their waveforms for $D > 0.5$.

Regime 1 (t_1–t_2): In this regime, S_{i1} switch is in the cut-off situation and S_{i2} switch is in the conduction regime as illustrated in Fig. 2(a). Current flows through the two different paths. First one is that current flows through the L_{i2} and S_{i2}. Energy is stored in the L_{i2}. The current in the L_{i2} increases linearly

$$\Delta i_{Li2} = \left(1 / L_{i2}\right) V_{in} \left(1 - D\right) T_s. \tag{2}$$

Through the second path, power is transferred to the battery via L_{i1}, D_{i1} and C_f. The current in the L_{i1} decreases linearly

$$\Delta i_{Li1} = \left(1 / L_{i1}\right)\left(V_{out} - V_{in}\right)\left(1 - D\right) T_s. \tag{3}$$

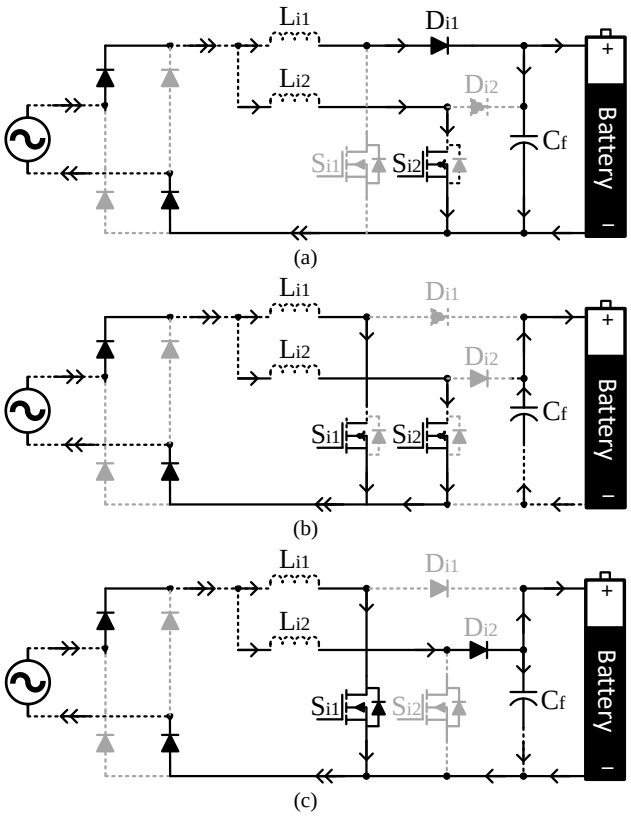

Fig. 3. Operating interval circuit of the proposed converter regimes: (a) Regime 1; (b) Regime 2; (c) Regime 3.

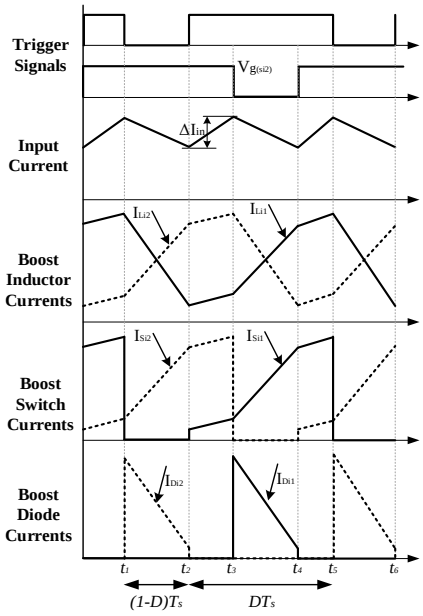

Fig. 4. Interleaved PFC boost converter Waveforms for $D > 0.5$.

Input ripple current of the converter is the sum of (2) and (3).

Regime 2 (t_2–t_3, t_4–t_5): In this regime, S_{i1} and S_{i2} switches are in the conduction regime as illustrated in Fig. 2(b). Current flows through the two different paths. First one is that current flows through the L_{i1} and S_{i1}. The second path is that current flows through the L_{i2} and S_{i2}. Energy is stored in the L_{i1} and L_{i2}. The current in the L_{i1} and L_{i2} increases linearly as given in equation (4):

$$\begin{cases} \Delta i_{Li1} = (1/L_{i1})V_{in}(D-1/2)T_s, \\ \Delta i_{Li2} = (1/L_{i2})V_{in}(D-1/2)T_s. \end{cases} \quad (4)$$

Regime 3 (t_3–t_4): In this regime, S_{i2} switch is in the cut-off situation and S_{i1} switch is in the conduction regime as illustrated in Fig. 2(c). Current flows through the two different paths. First one is that current flows through the L_{i1} and S_{i1}. Energy is stored in the L_{i1}. The current in the L_{i1} increases linearly

$$\Delta i_{Li1} = (1/L_{i1})V_{in}(1-D)T_s. \quad (5)$$

Through the second path, power is transferred to the battery via L_{i2}, D_{i2} and C_f. The current in the L_{i2} decreases linearly

$$\Delta i_{Li2} = (1/L_{i2})(V_{out}-V_{in})(1-D)T_s. \quad (6)$$

Figure 5 and Figure 6 illustrate the operating interval circuits of the interleaved PFC boost converter and their waveforms for $D < 0.5$.

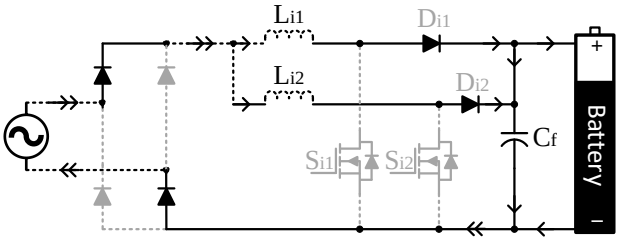

Fig. 5. Operating interval circuit of the proposed converter regimes (Regime 1).

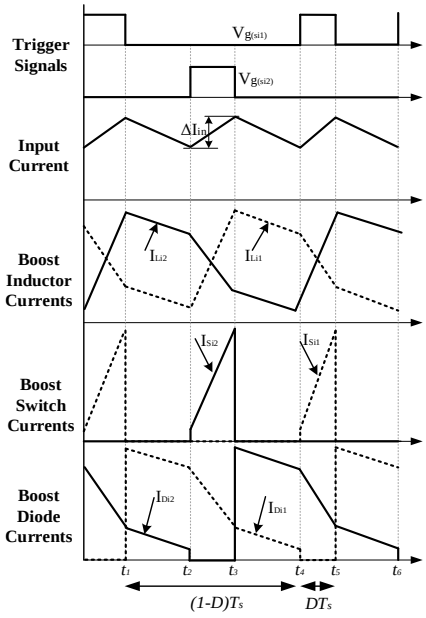

Fig. 6. Interleaved PFC boost converter Waveforms for $D < 0.5$.

Regime 1 (t_1–t_2, t_3–t_4): In this regime, S_{i1} and S_{i2} switches are in the cut-off regime as illustrated in Fig. 5. Current flows through the two different paths. The power is transferred to the battery via L_{i1}, D_{i1}, and C_f and L_{i2}, D_{i2}, and C_f. The current in the L_{i1} and L_{i2} decreases linearly as given in equation (7) below:

$$\begin{cases} \Delta i_{Li1} = (1/L_{i1})(V_{out}-V_{in})(1/2-D)T_s, \\ \Delta i_{Li2} = (1/L_{i2})(V_{out}-V_{in})(1/2-D)T_s. \end{cases} \quad (7)$$

Input ripple current of the converter is the sum of Δi_{Li1} and

Δi_{Li2}.

Regime 2 (t_2–t_3): Operating principle of this regime is similar to Regime 1 at $D > 0.5$. However, the duration of the current in this interval is different because of the duty cycle value. This difference affects the inductor ripple currents. These currents are determined as follows:

$$\Delta i_{Li2} = (1 / L_{i2}) V_{in} D T_s, \quad (8)$$

$$\Delta i_{Li1} = (1 / L_{i1})(V_{out} - V_{in}) D T_s. \quad (9)$$

Regime 3 (t_4–t_5): Operating principle of this regime is similar to Regime 3 at $D > 0.5$. However, the duration of the current in this interval is different because of the duty cycle value. This difference affects the inductor ripple currents. These currents are determined as follows:

$$\Delta i_{Li1} = (1 / L_{i1}) V_{in} D T_s, \quad (10)$$

$$\Delta i_{Li2} = (1 / L_{i2})(V_{out} - V_{in}) D T_s. \quad (11)$$

B. Proposed Dynamic Voltage Compensator (DVC)

DVC is a ripple cancellation circuit as shown in Fig. 2(a), which is added between the output of the converter and the battery. The main goal of this concept is minimizing the DC-link capacitance value of the interleaved PFC boost converter. The operating principle of the DVC is based on sensing of the ripple voltage on the DC-link capacitor. It generates the same voltage at the output of the DVC. With this method, the voltage fluctuation on the DC-link capacitor is eliminated.

For DVC circuit, full-bridge converter (FBC) and required input-output filters are designed to generate the inverse ripple voltage (V_{comp}), which is equal to ΔV_{cap}. FBC uses a DC voltage source at the input with voltage V_{dc}. Hysteresis controller is used to trigger the gate of the switches of the FBC. This control loop, firstly, senses the capacitor voltage and produce the reference voltage. Comparing this sensed voltage with V_{comp}, the error signal is calculated. The error signal is used as an input signal of the hysteresis control. Then, according to the switching frequency, the bandwidth of the hysteresis control is selected. Generated PWM signals trigger the switches of the FBC.

According to the DC analysis of the circuit illustrated in Fig. 2:

$$V_{bat} = V_{cap}, \quad (12)$$

$$I_{bat} = I_{conv}. \quad (13)$$

Voltage ripple of the DC-link capacitor depends on the integral of the difference between the output current of the converter and the battery current. This is expressed as:

$$v_{comp}(t) = \Delta v_{cap}(t) = (1 / C_{dc}) \int [i_{conv}(t) - i_{bat}(t)] dt, \quad (14)$$

$$\Delta v_{cap}(t) = |\Delta V_{cap}| \sin(2\omega t - \varphi). \quad (15)$$

α is the ripple factor expressed as follows

$$\alpha = |\Delta V_{cap}| / V_{cap}. \quad (16)$$

Substituting equation (15) and equation (16) into equation (14), the one has

$$C_{dc} = \lfloor 1 / (\alpha V_{cap} \sin(2\omega t - \varphi)) \rfloor \int [i_{conv}(t) - i_{bat}(t)] dt. \quad (17)$$

C. Proposed Digital Controller of Interleaved PFC Boost Converter

Control of the AC/DC converter aims to transfer power drawn from the grid to the battery with maximum efficiency and power factor correction, which is critical to the reactive power compensation. For this control, there are controllers designed as analogue as shown in Fig. 1(b) in the literature. However, the speed of this controller is quite slow. This paper presents a fully digital controller for to increase the dynamic performance of the system. With this controller, the output voltage and input current reach to the desired value in a shorter time and with fewer oscillations.

Controller of this circuit contains two control loops: the outer current loop and the inner voltage control loop.

– The inner voltage control loop is used to keep the output voltage at the desired value. This controller generates the reference current value required for the current control loop used for implementation of the unity power factor. For this regards, PI controller is designed for inner voltage control loop. The designed controller successfully maintains the output voltage at 400 V_{dc} for an input voltage range of 85 V_{rms} –265 V_{rms}.

– The outer current control loop is used to eliminate the reactive power drawn from the grid by providing unity power factor.

– The phase locked loop is used to detect the phase and frequency information of the grid voltage. The output of this loop is multiplied by error signal of the output voltage control loop to equalize the phases of the input current and input voltage.

III. TEST RESULTS

To validate the proposed technique and its controller, an AC/DC interleaved PFC boost converter is used. Simulation studies of the designed system are carried out in Matlab/Simulink environment. Matlab/Simulink model of the designed system is given in Fig. 7. The parameters of the designed system are given in Table I.

TABLE II. DEFINITION OF THE EU EFFICIENCY.

Output power (% of rated)	5 %	10 %	20 %	30 %	50 %	100 %
Weighting factor	3 %	6 %	13 %	10 %	48 %	20 %

The modelled converter is tested in different load conditions. These conditions are selected according to the EU efficiency standards as shown in Table II.

Figure 8 shows the comparison of the output voltages of the conventional and proposed interleaved PFC boost converters.

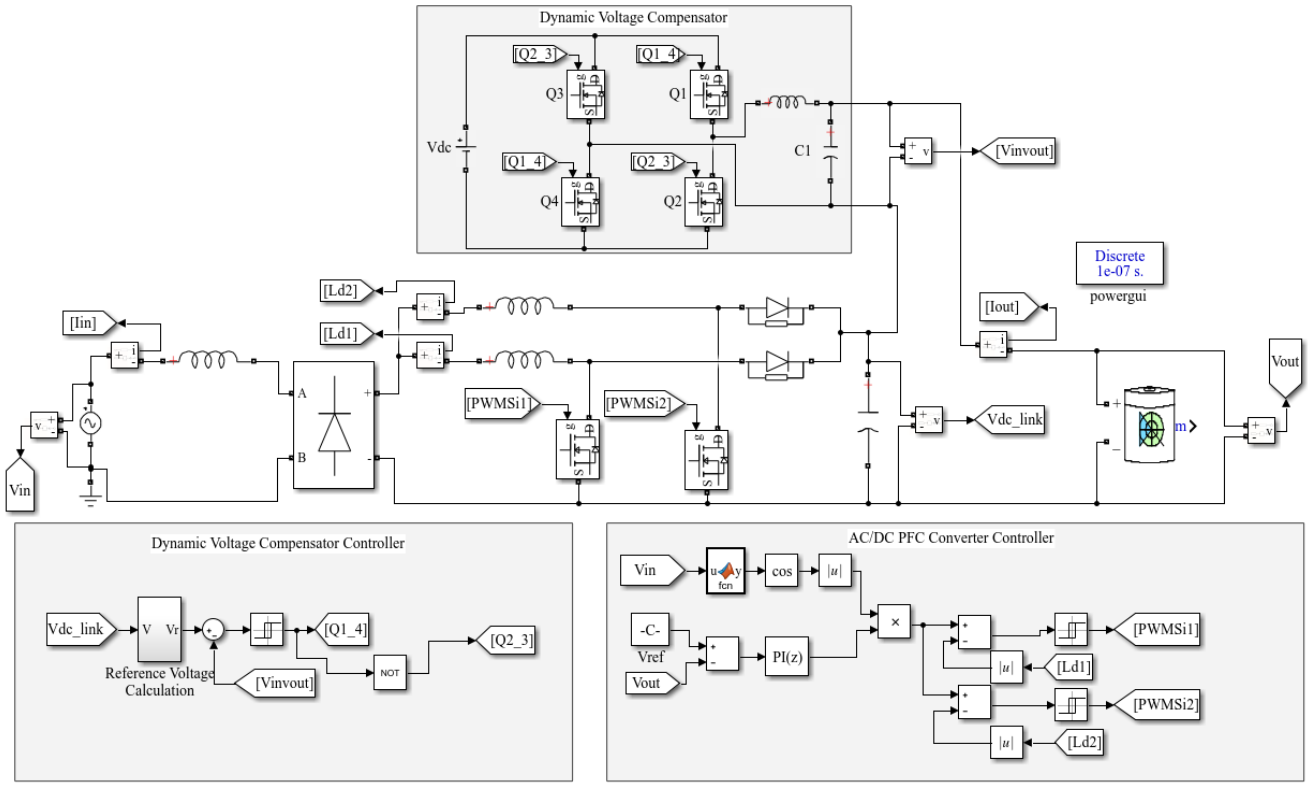

Fig. 7. Matlab/Simulink model of the designed system.

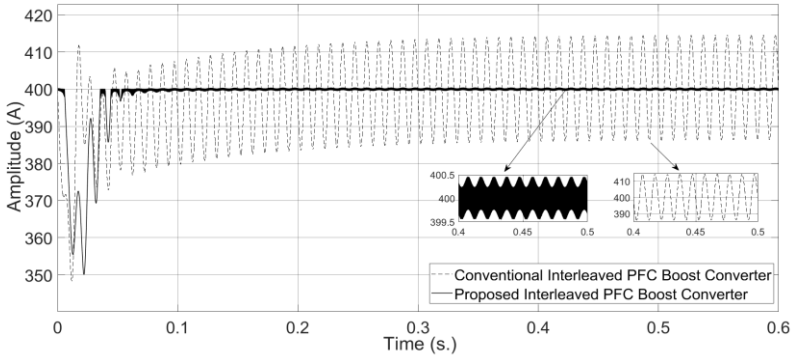

Fig. 8. Output voltage waveforms of the conventional and proposed converters (@Vin = 220 V_{rms}, P_{out} = 3300 W).

TABLE I. THE PARAMETERS OF THE DESIGNED SYSTEM.

Parameter	Value	Unit
Input voltage	85–265	V_{rms}
Input line frequency	50–60	Hz
Output voltage	400	V_{dc}
Output power	3.3	kW
Interleaved PFC boost converter inductances (L_{i1}, L_{i2})	0.6	mH
Interleaved PFC boost converter switching frequency	70	kHz
DC-link capacitor	1	mF
PI parameters of voltage control loop	K_p = 0.1 K_i = 12	N/A N/A
Hysteresis band value of the converters	0.4	A

From Fig. 8, it can be clearly seen that the output voltage ripple value is approximately 26 V in the conventional interleaved PFC boost converter circuit while the ripple value is 1 V in the proposed interleaved PFC boost converter with the same capacitor. With the reducing of ripple value, the capacitor size can be minimized by approximately five times. Also, with the proposed digital controller, the output voltage of the converter reaches the desired value with less oscillation in about 0.05 seconds. However, this time is about 0.4 seconds and the oscillations are higher in the conventional converter.

The input current harmonics of the conventional and proposed topology compared with EN 61000–3–2 standard at 220 V_{rms} input are given in Fig. 9. The proposed method greatly reduces the harmonics of the input current.

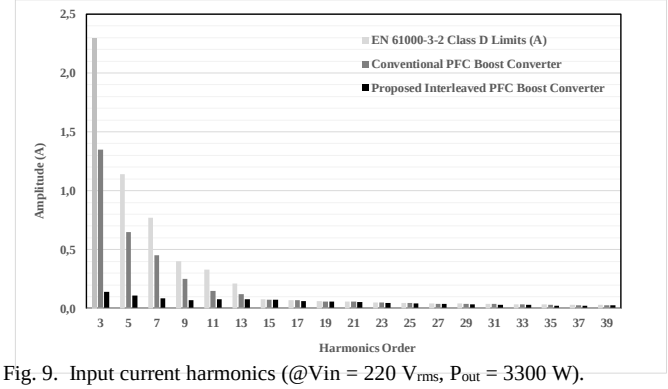

Fig. 9. Input current harmonics (@Vin = 220 V_{rms}, P_{out} = 3300 W).

Input voltage and input current of the proposed power factor corrected converter are given in Fig. 10.

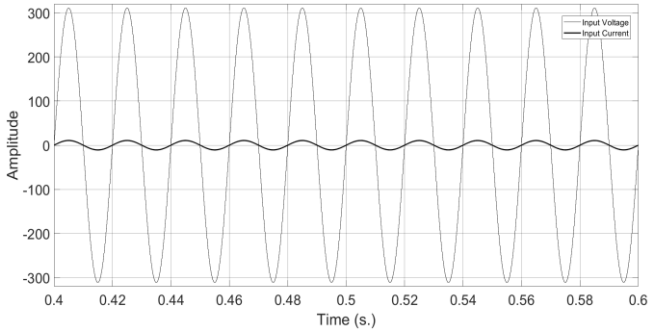

Fig. 10. Input voltage and input current (@P_{out} = 3300 W).

From Fig. 10, it can be deduced that the power factor correction ability of the proposed system is good.

TABLE III. PERFORMANCE OF PROPOSED SYSTEM.

States	Efficiency of the Conventional system (η)	Efficiency of the Proposed system (η)	ΔV Volt. Ripple (@Conventional system)	ΔV Volt. Ripple (@Proposed system)
@5 % Load	79.18 %	88.42 %	5.4 V	0.1 V
@10 % Load	88.42 %	93.22 %	7.6 V	0.2 V
@20 % Load	92.87 %	95.37 %	9.8 V	0.3 V
@30 % Load	93.90 %	96.02 %	11.5 V	0.5 V
@50 % Load	94.12 %	96.41 %	19.4 V	0.8 V
@100 % Load	94.11 %	96.75 %	26.2 V	1 V

Performance results of the proposed system vs. conventional system are given in Table III. Also, the output voltage, output current, and efficiency curve of the proposed system at EU efficiency standard conditions are given in Fig. 11–Fig. 13.

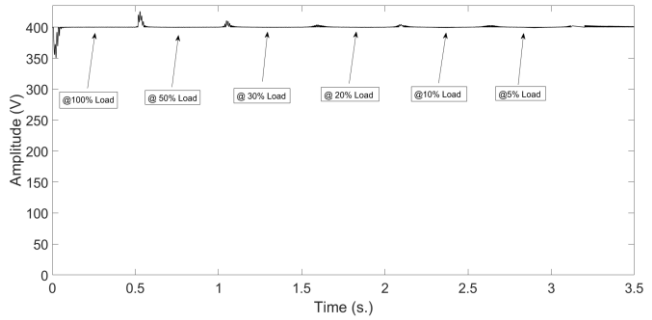

Fig. 11. Output voltage of the proposed system according to the load conditions in the European efficiency standard (@V_{in} = 220 V_{rms}).

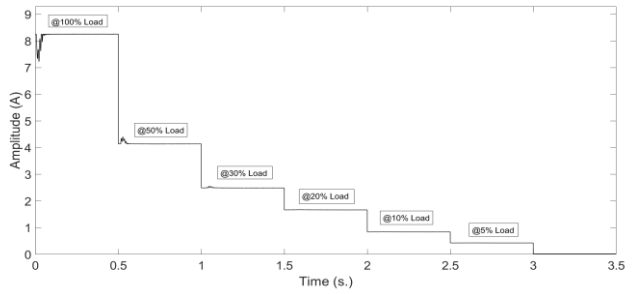

Fig. 12. Output current of the proposed system according to the load conditions in the European efficiency standard (@V_{in} = 220 V_{rms}).

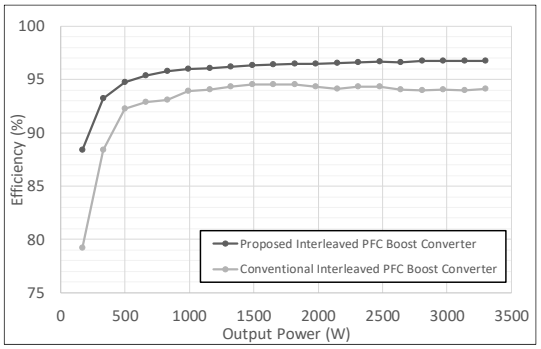

Fig. 13. Efficiency of the conventional vs. proposed system (@V_{in} = 220 V_{rms}).

From Fig. 11–Fig. 13, it is obvious that the proposed dynamic voltage compensator and the digital controller positively effect the performance of the system. According to the EU efficiency standard, the overall efficiency of the proposed system measured is about 95.87 %.

IV. CONCLUSIONS

A dynamic voltage compensator (DVC) technique and fully-digital controller are presented and analysed for the minimizing of the capacitance value and improvement of the dynamic behaviour of interleaved power factor corrected (PFC) boost converter for the battery charger in electric vehicles. The capacitance value is reduced by approximately five times. Also, due to the proposed fully digital controller, the response capability of the system is enhanced. The efficiency of the overall system measured is 95.87 % according to the EU efficiency standard.

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