An Active Inductor Based Low Noise Amplifier for RF Receive

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***Abstract*—Low Noise Amplifier (LNA) is a significant part in Radio Frequency (RF) receivers and plays a key role in the chip size and the implementation cost. An LNA for RF receivers utilizing the active inductor is presented. The proposed design is an alternative solution to overcome the usage of passive inductors to reduce the chip area. Besides, the active inductor reduces the parasitic capacitors affect at high frequencies. Designed in 0.18-µm CMOS process, the LNA achieves a voltage gain of 20dB, a minimum Noise Figure (NF) of 3.1 dB with low power consumption and good input and output impedance matching at 2.45 GHz. With 0.003 mm^2 chip area, the proposed design is suitable for portable wireless communication devices.**

***Index Terms*—Low noise amplifier, Radio frequency, RF receiver, CMOS.**

I. INTRODUCTION

Radio Frequency (RF) transmitters and receivers are used in many applications such as Global Positioning System (GPS), Wireless Fidelity (Wi-Fi), Bluetooth, RF Identification (RFID) systems etc. The performance of RF transmitters and receivers controls the efficiency of these portable systems. Low noise amplifier (LNA) is the most effective part in an RF receiver.

LNA design depends on the balancing of low power, high gain and low noise figure (NF). Various techniques have been applied to achieve the low power with high gain and low NF. Inductive LNA is suitable for ultra wideband application. It has two topologies: Common-Gate LNA (CGLNA) and Common-Source LNA (CSLNA) [1]–[3]. But the use of passive inductors in these designs result greater area and cost. In [4] CGLNA current-reuse technique is adopted to improve the transconductance at the expense of greater cost as it uses passive inductors.

Another technique of inductor-less LNA is used to reduce the chip size and overall cost. Noise cancelling technique is used to get lower NF. But this technique is not effective at high frequency as in [5], [6]. Noise cancelling techniques are used in [7], [8] but the disadvantage is the low voltage gain. In [9], inductor-less LNA is used to reduce the chip size. But the disadvantage of this design is the high power consumption. Inductor less LNA with CGLNA is also used in [10]. However, it consumes high power.

To avoid using passive inductors and implementation of active inductors for achieving high gain as well as reduced NF, a different approach of LNA is proposed in this paper.

II. CONVENTIONAL LNA

LNA is the backbone of radio receivers and it is the first stage in RF receivers. LNA should match with the antenna's characteristic such as input impedance. Fig. 1 shows few conventional LNA for input impedance matching. In Fig. 1(a), CGLNA with inductor and resistor is used at the input to get the desired frequency and input matching instantaneously. This is suitable in a narrowband as the design has a problem with NF in wideband LNA. Fig. 1(b) shows Resistive Feedback LNA with noise cancelling technique. However, this design has limitation at high frequency due to parasitic capacitor and high power consumption.

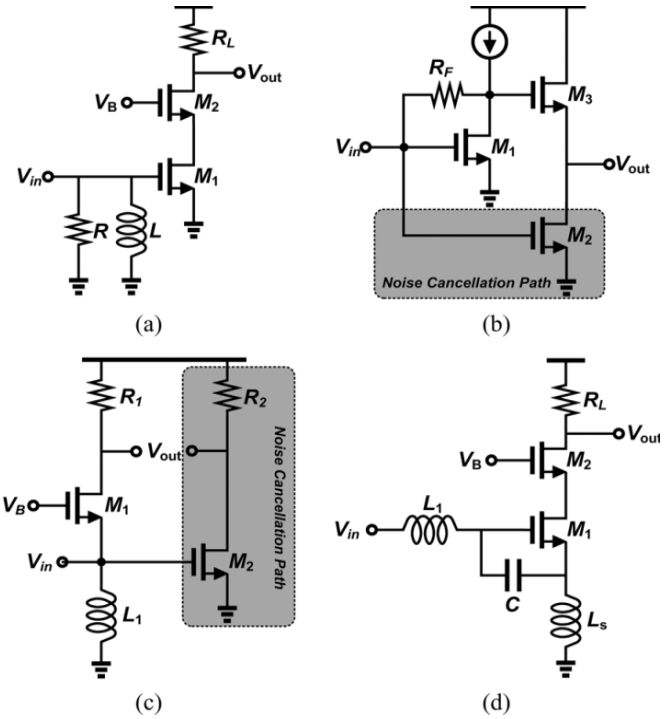

Fig. 1. Conventional LNA topologies: (a) parallel resistance input matching; (b) resistive feedback; (c) common gate; (d) inductive degeneration [9].

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The input impedance matching is easy to obtain in CGLNA shown in Fig. 2(c). However, the voltage gain is relatively low. The CSLNA with inductor at the source is used to compensate for the parasitic capacitor at resonance frequency as shown in Fig. 2(d). Active inductors have high flexibility for input impedance matching without any magnetic effects [9].

III. METHODOLOGY

In conventional CGLNA, inductor and resistor are used but in the proposed design register is eliminated. The design does not utilize the conventional resistive feedback technique as it suffers from parasitic capacitance and high power consumption at high frequency. The proposed LNA is composed of three stages as shown in Fig. 2. The details of the stages are explained in details below.

Fig. 2. Block diagram of the proposed LNA.

A. Common gate amplifier

Common gate amplifier is used as it is easy to obtain input impedance matching. The input impedance (Z_{in}) depends only on the transconductance (g_m) of CMOS transistor as shown in (1)

$$Z_{in} = \frac{1}{g_m}. \tag{1}$$

B. Active inductor

Active inductor is a combination of CMOS transistors which perform the same function as passive inductors. Fig. 3 shows the active inductor and its equivalent circuit.

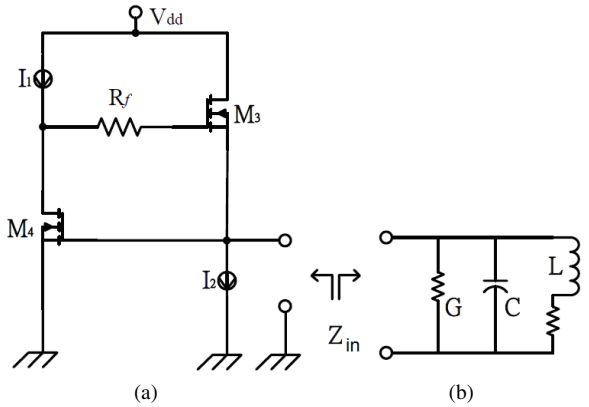

Fig. 3. Active inductor circuit and its equivalent circuit [10].

In Fig. 3(a), the quality factor (Q), inductance (L) and frequency (f) is calculated from (2), (3) and (4), where C is the capacitance, R is the resistance and g_m is the transconductance. The Q is high enough as it mainly depends on R_f:

$$L \approx \frac{C_{gs3}\left(1+R_{fgds4}\right)}{g_{m4}g_{m3}}, \tag{2}$$

$$Q \approx \sqrt{\frac{g_{m4}g_{m3}C_{gs3}X(1+R_{fgds4})}{g_{ds4}{}^2 C_{gs4}}}, \tag{3}$$

$$\omega \approx \sqrt{\frac{g_{m4}g_{m3}}{C_{gs4}C_{gs3}(1+R_{fgds4})}}. \tag{4}$$

To improve the active inductor in Fig. 3, double feedback with second order is used. Fig. 4 presents the active inductor after improvement.

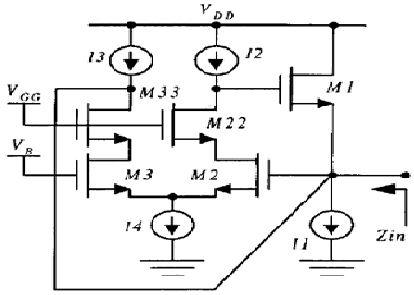

Fig. 4. Double feedback active inductor with second order effects [11].

C. Common drain (buffer)

Common drain is usually used as a final stage in every LNA because it has very small output impedance. So, it results good output impedance matching.

The proposed LNA is designed in CEDEC 0.18μm CMOS process. All stages are connected together and the complete LNA circuit is shown in Fig. 5. Minimum numbers of transistors with small widths are used to obtain low power consumption and reduce parasitic affect. The length of the transistors is 0.18μm for all transistors. The widths are shown in Table I.

TABLE I. THE TRANSISTORS WIDTH OF THE PROPOSED LNA.

Transistor	Width
M_0	8 μm
M_1,M_2,M_3	12 μm
M_4,M_5	1.8 μm
M_6,M_7	2 μm
M_8,M_9	4 μm
M_{10}	3.6 μm
M_{11}	2.7 μm

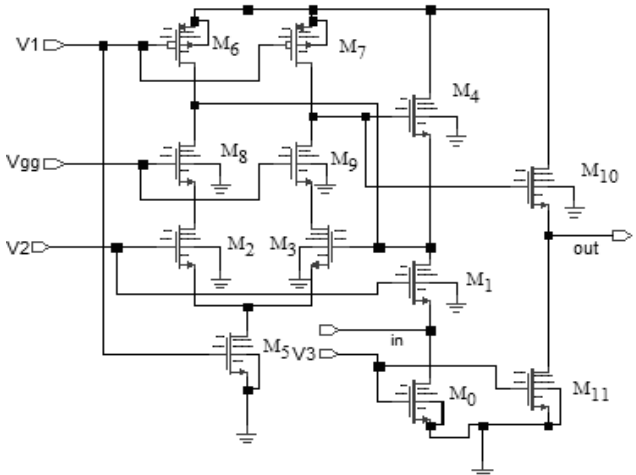

Fig. 5. Schematic of the proposed LNA with active inductor.

IV. DISCUSSION AND RESULTS

The proposed active inductor LNA is designed and simulated in CEDEC 0.18-µm CMOS process. Appropriate bandwidth is selected to get high voltage gain. The biasing voltage V1 =1.1V, V2=0.6V,V3=0.6V and Vgg=0.7V. Fig. 6 shows the simulation results of output voltage (dB) against frequency. The centre frequency is 2.45 GHz and the bandwidth extends up to 1GHz. The transient output voltage of the proposed LNA is shown Fig. 7.

Table II shows the comparison and specification of the proposed LNA with other reported work. The problem of the large area of Inductive LNAs is clearly evident in [1]–[4]. While the inductor-less LNA is one of the good ways to reduce the chip size and overall cost. However, they may cause loss in voltage gain as seen in [7], [8]. Moreover, inductor-less LNA is not effective at high frequency as in seen [5], [6] from the table.

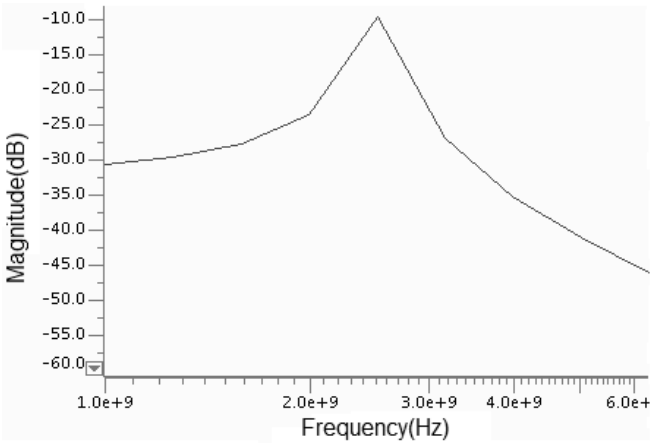

Fig. 6. Simulation result of output voltage (dB).

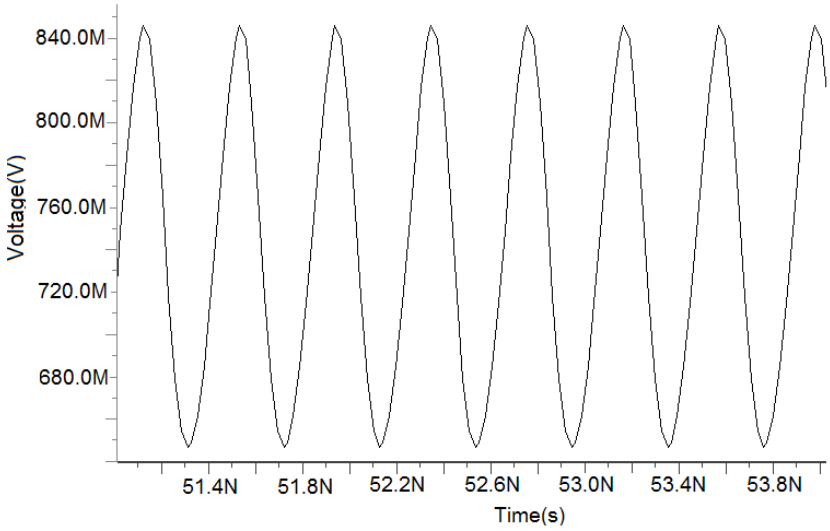

Fig. 7. The transient output voltage of the proposed LNA.

TABLE II. COMPARISON AND SPECIFICATION OF THE PROPOSED LNA AND OTHER REPORTED WORKS.

	Frequency (GHz)	**Technology (µm)**	**Gain (dB)**	**Supply (V)**	**NF (dB)**	**-IIP3 (dBm)**	**Power (mw)**	**Area (mm^2)**
This work	2-3	0.18	20	1.8	3.1	-	0.5	0.003*
[1]	3.1-10.6	0.18	7-12	1.5	5.2-7	-2.23	4.5	1.03
[2]	0.03-6.2	0.18	8.6	1.8	4.8	1.8	9	1.16
[3]	2.45	0.13	14.5	1.6	0.65	-	6.5	1
[4]	3.1- 4.8	0.13	13	1	3.5	-6.1	3.4	0.4
[5]	0.15-0.6	0.18	12.9	1.8	3.9	1.03	-	-
[6]	0.05-0.9	0.18	16.4	1.8	3.4	0	14	0.04
[7]	0-2	0.18	12.4	1.8	4.9	0	18	0.034
[8]	0-10	0.065	10.5	1	3.3	-3.5	13	0.02
[9]	0.32-1	0.18	18	1.8	2.7	0	15.3	0.1
[10]	1-3.05	0.18	16.9	1.8	2.85	-0.7	12.6	0.073

As shown in Table II, by employing the proposed active inductor based LNA achieves a voltage gain of 20dB at 2.45 GHz frequency, which is comparably higher than other works. Compared to other mentioned research works, NF of 3.1dB and power consumption of 0.3mW in such a high frequency are also major achievements. Therefore, output signal-to-noise ratio has improved data rate speed with little expense of power. The chip area is only 0.003mm^2 and it is due to adopting small size of transistors as well as avoidance of passive components. The proposed active inductor LNA layout is designed in CEDEC 0.18-µm CMOS process. The layout is shown in Fig. 8.

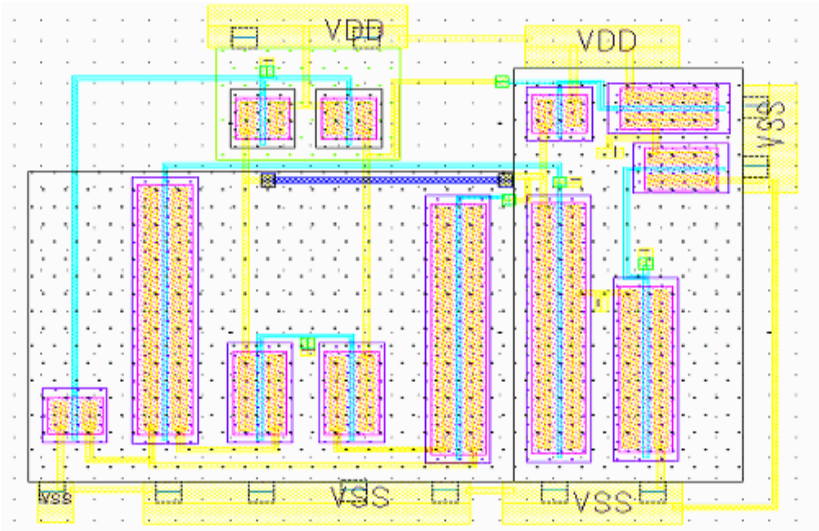

Fig. 8. Layout of the proposed LNA.

V. CONCLUSIONS

LNA for 2.45GHz of RF receiver is developed by using an active inductor. Designed in 0.18-µm CMOS process, the design achieves a voltage gain of 20dB, a minimum NF of 3.1 dB with low power consumption and good input and output impedance matching. The chip area is only 0.003 mm^2 which would also reduce the implementation cost. The proposed LNA is suitable to be implemented in portable wireless communication devices.

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