Comparative Study of SiC Transistors for Active Current Limitation in S3R

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***Abstract*—In this paper a comparative analysis between different kinds of Silicon Carbide (SiC) transistors applied to the Sequential Switching Shunt Regulator (S3R) with active current limitation capability is presented. The S3R is a well-known Direct Energy Transfer photovoltaic power conditioner used in space vehicles.**

The main novelty discussed in this paper is the use of SiC transistors, JFET cascodes and SiC MOSFETs, instead of Silicon MOSFETs. High-voltage, high-power and high-temperature characteristics of these devices make them ideal for this application.

***Index Terms*—S3R; sequential switching shunt regulator; SiC; Cascode; current limiter; WBG.**

I. INTRODUCTION

In the literature, many different options to implement the power conditioning unit (PCU) of a satellite could be found [1]. In all of them, the main purpose is to extract the energy from the solar arrays and deliver it to the main bus for distribution and consumption.

There are two main groups of satellite's PCU. On one hand there are Direct Energy Transfer (DET) systems, which are characterized by its simplicity, robustness and lower mass. On the other hand, Maximum Power Point Tracking (MPPT) systems have the advantage of maximise the energy drawn by photovoltaic sources, but require DC-DC converters and it has a subsequent impact on the power density ratio. In both cases, each group is subdivided into unregulated systems and regulated systems, being the latter, a more complex architecture.

The Sequential Switching Shunt Regulator (S3R) is a photovoltaic DET power conditioner developed in the 70s [2], [3] and widely employed in telecom and scientific missions, especially in Europe. Figure 1 shows the diagram of a typical regulated system using S3R, Battery Charge Regulator (BCR) and Battery Discharge Regulator (BDR).

The main advantages of the S3R include high modularity, robustness (in a catastrophic power cell fault, neither dynamics nor bus voltage ripple would be affected), reduced switching losses (only one power cell switches while the rest of the cells stay connected or unconnected) and design flexibility (applicable for a wide power range).

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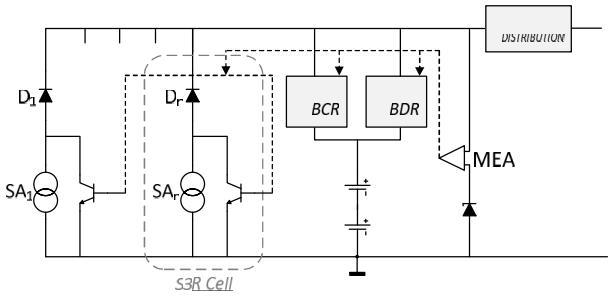


Fig. 1. Simplified topology of a direct transfer conditioning system with S3R control system. Battery charging and discharging units, BCR and BDR, respectively, are shown.

In the past, the parasitic capacitance of the solar array was neglected for the design of this type of photovoltaic power regulators; nonetheless, nowadays this has become a critical issue [4]. Two facts are the main causes for the increase of solar section parasitic capacitance, increase of individual cell capacitance due to multi-junction technologies and larger sections with many strings in parallel. Currently, parasitic capacitances values reach few microfarads [5].

This fact has a wide importance in the S3R system where the regulation is achieved short-circuiting some solar array sections through a shunt branch. This is implemented with power transistors and, when panel is short-circuited, they should discharge also this capacity, achieving quite high currents. This current discharge must be limited through the transistor so it is not damaged.

This work is focused on the active limitation of the solar array parasitic capacitance discharge current. To limit this current, the shunt transistor will work in its lineal region during the discharge, restricting the current.

II. S3R DESCRIPTION AND OPERATION

In Fig. 2, the S3R regulation system with four switching cells is shown. It should be noted that a real system could have a different number of cells, depending on the dimensions and energy requirements of the satellite. All the parasitic cells have been depicted in Fig. 3.

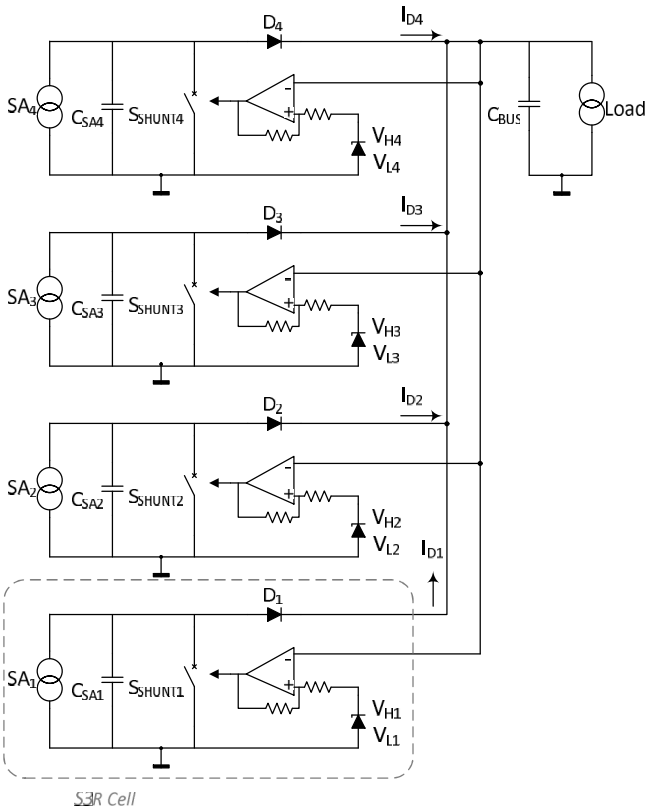


Fig. 2. S3R regulator simplified topology with four switching cells.

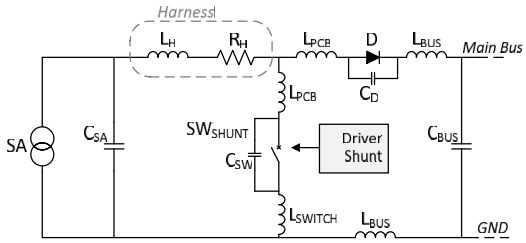


Fig. 3. Representation of the principal parasitic elements in an S3R switching cell.

First of all, the operation of a single cell will be explained, and straightaway, the sequential operation of the system will be detailed all together. As it can be observed in Fig. 2, each single cell has two states dependent on the switch S_{SHUNT} state. Both states are shown in Fig. 4 in simplified form.

From Fig. 4, supposing that the solar array current is greater than the load current, it can be deduced that as long as the cell is in position a), the bus voltage will increase due to the bus capacitor charge. While as long as the cell remains in state b), the bus voltage will decrease due to the capacitor discharge through the load.

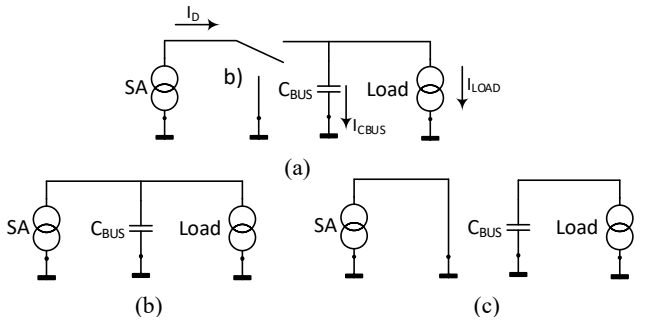


Fig. 4. Basic topological states of an individual S3R cell: (a) and (b) the SA injects power to the bus capacitor (C_{BUS}); (c) the C_{BUS} capacitor is discharged through the load.

The regulation concept is based on the establishment of two thresholds (V_H and V_L) for each single cell, where the state change is carried out, being able to maintain the bus voltage limited between these two values. Figure 5 represents the waveform or the bus voltage.

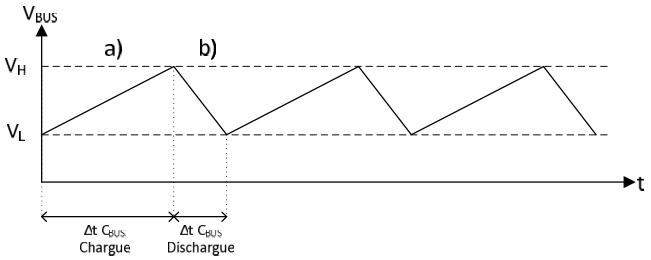


Fig. 5. Regulated voltage of the bus by means of the regulation system S3R monocellular.

The main bus current equations of this regulation system are described hereunder. Regarding state, a), the bus capacitor would be charging by means of a current defined as (1), whereas during state b), the capacitor would be discharged through a value current (2):

$$i_{C_{BUS}} = I_D - I_{LOAD} = C_{BUS}\frac{V_H - V_L}{\Delta t_{Cbus_{Charge}}}, \quad (1)$$

$$i_{C_{BUS}} = -I_{LOAD} = C_{BUS}\frac{V_H - V_L}{\Delta t_{Cbus_{Discharge}}}. \quad (2)$$

A system with a single S3R cell would not be feasible due to different reasons. The size of this solar array should be very high in systems where considerable powers are required. On other hand, it would not be a reliable system, because all the energy supply would depend exclusively on this only array and this only S3R cell. For these reasons a sequential regulation system is implemented, a system in which diverse cells in parallel are set.

To define its functioning, we will consider a S3R with four cells like in Fig. 2.

First, the levels of the voltage thresholds are defined for each cell in such a way that they remain in a sequential system as it is shown in Fig. 6.

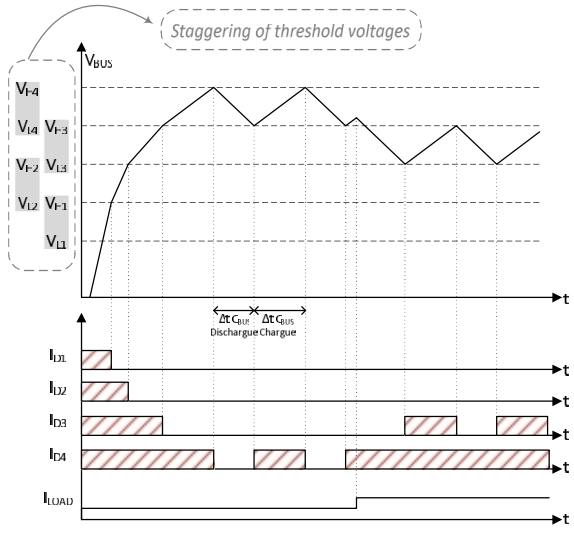


Fig. 6. Staggering of the threshold voltages in the S3R and the bus voltage evolution with a positive charge step.

The final aim of the system is to remain in such a state that only one of the solar array is switching. As a general rule, a steady situation while there are no load changes, in which case is probable that the system changes to a higher or a lower step depending on if the demand of current is higher or lower in the new state.

In a starting system situation, since the bus voltage would be below all thresholds, all cells would inject current in the bus, as Fig. 6 shows, thus leaving a load current (3) and a slope in the capacitor voltage (4):

$$i_{C_{BUS}} = \sum I_D - I_{LOAD}, \tag{3}$$

$$\frac{\Delta V_{BUS}}{\Delta t} = \frac{t_{C_{BUS}}}{C_{BUS}}. \tag{4}$$

As the bus is charging, it will exceed the threshold voltages of each section and hence, that section will short-circuit its solar array, reducing the supply of current to the bus and therefore the main capacitor charge slope. This will happen until a steady state in the system is established. In this steady state some solar arrays are permanent connected to the bus and a single solar array switching, permitting the regulation between its values V_H y V_L, and some solar arrays are short-circuited. In Fig. 6 this operation is shown with a positive load jump.

III. CURRENT LIMITATION IN THE SHUNT TRANSISTOR

As it was explained in the previous section, the regulation of the main bus is achieved limiting the power delivered by the solar array short-circuiting some sections permanently and switching between the main bus and short circuit one section. To short-circuit the solar arrays implies the discharge of their parasitic capacitance. Nowadays, the increase of the parasitic capacitance supposes a risk for the power transistors reliability, for this reason different methods have been studied to limit the current [6].

In addition to the methods described in [6], to ensure the device safe operation, the European Space Agency (ESA) defines in ECSS-Q-ST-30-11C some specifications that the devices used for space applications must accomplish as safe preventive measures. In the case under examination there are three considerations:

1. The current through the transistor must be derated to 75 % of the maximum established for the device;
2. The maxim junction temperature must be limited to 110 ºC;
3. The power dissipated must be derated to 65 % of the maximum established power.

It must be considered that the limit for the semiconductor junction temperature is for Si semiconductors, this is due because the SiC semiconductors are relatively recent and they are not considered in the ECSS guides. However, it is a proven fact that the temperature supported by the Si semiconductors is considerably supported by SiC devices, in addition, from the ESA different objectives are analysed for the application of the SiC due in large measure to the advantages it brings [7].

Different methods are used to limit the shunt transistor current, one of the most used is the active limitation current technique because it is the most independent of the system. The other options must be designed and adjusted according to the parasitics of the elements. For the satellite PCU designs, the modularity and flexibility are very important points in order to consider different options.

The main waveform of the S3R switching cell are shown in Fig. 7. In discontinuous it is shown S3R cell waveforms without active current limitation and in continuous S3R cell waveforms with active current limitation.

As can be seen in Fig. 7, in a S3R cell without active current limitation, a high current peak will circulate through the transistor due to solar array parasitic capacitance discharge. In the active current limitation design, the discharge current of the parasitic capacitance is limited to a predefined value (I_{LIM}), this is accomplished controlling the gate voltage of the shunt transistor so it works in its linear region.

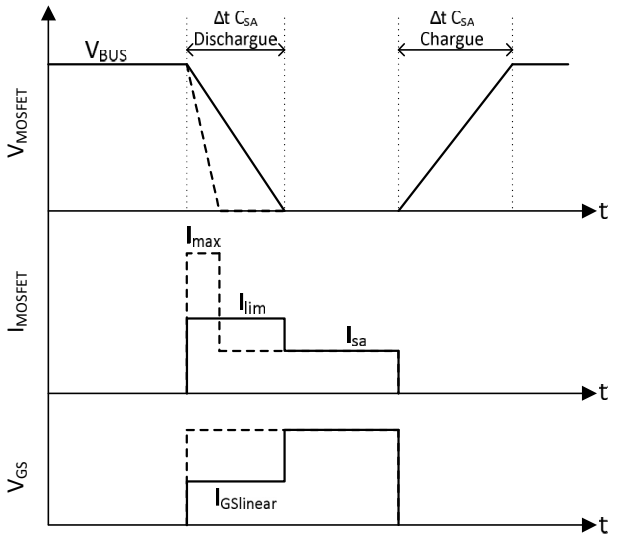


Fig. 7. S3R cell switching waveforms. In discontinuous line, the system without current limitation. In continuous line, the system with active current limitation.

From these waveforms, we obtain the shunt transistor dissipated power equations. In this case the parasitics elements shown in Fig. 3 are neglected. The solar array parasitic capacitance stored energy can be expressed as (5), therefore, if the transistor must dissipate this energy, we have an expression like (6):

$$E_{C_{SA}} = \frac{1}{2} C_{SA} V_{BUS}^2, \tag{5}$$

$$P_{M_{SHUNT}} = \frac{1}{2} C_{SA} V_{BUS}^2 f_{S_{BUSC_{SA}}}, \tag{6}$$

where $f_{S_{BUSC_{SA}}}$ is the cell switching frequency analysed in detail in [3] and according to authors it is given by (7)

$$f_{S_{BUSC_{SA}}} = \frac{< I_D > (I_{SA} - < I_D >)}{\Delta V_{BUS} I_{SA} C_{BUS} + < I_D > C_{SA} V_{BUS} - 2ESR < I_D > C_{BUS} (I_{SA} - < I_D >)}, \tag{7}$$

where I_{BUS} is defined as the solar array average current which is switching.

In the other hand, in a cell which implements active

current limitation, we are be able to obtain the dissipated power like (8)

$$P_{M_{SHUNT}} = \frac{1}{2}\frac{I_{LIM}}{I_{LIM} - I_{SA}} C_{SA} V_{BUS}^2 f_{S_{BUSC_{SA}}}. \quad (8)$$

In Fig. 8, it is shown the concept of active current limiting used in this study. Its operation is simple, at the moment that the bus exceeded the level V_H, the transistor M_{SHUNT} will be short-circuited, the current flows through it and therefore the voltage in the base of the Q transistor is increased because the current goes through the resistor R_{SHUNT}. As the voltage in the Q base increases, the Gate voltage of the Shunt transistor (V_G) is reduced, so the shunt transistor (M_{SHUNT}) operates in lineal zone limiting de current through it.

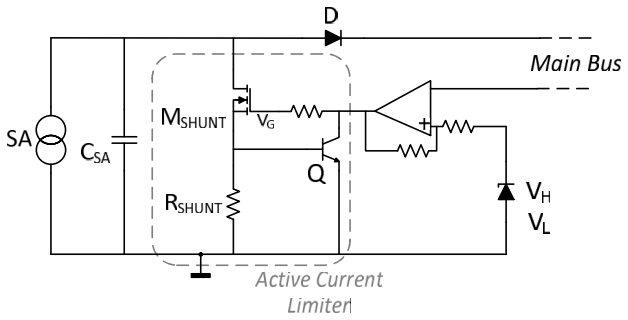


Fig. 8. Simplified topology concept active current limiter through the shunt branch of S3R cell.

Considering a saturation voltage of transistor Q V_{SAT_Q}, current limitation is defined by expression (9)

$$I_{LIM} = \frac{V_{SAT_Q}}{R_{SHUNT}}. \quad (9)$$

It should be noted that at the moment the shunt transistor short-circuits the panel, the dynamic of the current limiter must be fast enough so that there are not quick peaks that exceed the established maximum limits.

IV. Design Validation

A comparative study of different types of power transistors and semiconductor technologies will be carried out. The following table details the transistors used and their main characteristics.

TABLE I. USED TRANSISTORS.

Transistor	Technology	V_{DS} max [V]	I_D max [A]	R_{DSon} [mΩ]
IRF250n	Mosfet-N Si	200	30	85
C2M0080120D	Mosfet-N SiC	1200	36	80
UJC1206K	Cascode SiC	1200	35	60

The most commonly used transistor for this application is the IRF250n. It should be noted that the two alternatives have a voltage blocking capacity six times higher, and an ability to lead a similar current. On the other hand, the two new proposals are implemented with silicon carbide instead of classical silicon. The aim is to validate these alternatives for this application, as they have characteristics that make them very interesting, such as their greater capacity of block voltage and the capacity of the SiC semiconductor to operate at higher temperatures than conventional Si. First, the simulation results obtained will be presented and then the results of the real tests performed will be analysed.

The test consists on short-circuiting the photovoltaic panel, that will be considered a constant current source in simulation, and a solar panel simulator in the real test, with a parallel capacity simulating the parasitic capacity of the panel. As load, a resistive load in simulation and a resistance in the real case is used. The operation is performed at a constant frequency, simulating a steady state of the S3R.

Figure 9 shows an image of the implemented validation prototype.

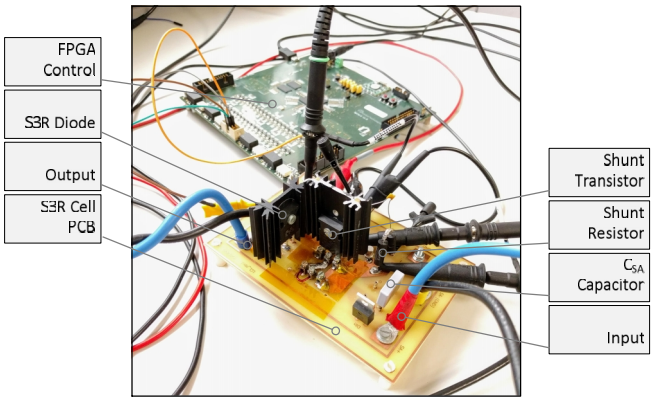


Fig. 9. Prototype implemented to test the different transistors. In the background the FPGA card for the generation of the PWM for the switching of the S3R cell.

The values used for the design validation are the following and will be common both for the simulations and for the real tests carried out:

– Input source current = 2 A;
– Limiting current = 8 A;
– Input capacitor = [0.68 - 1.5] µF;
– Bus capacitor = 480 µF;
– Switching Frequency = 1 kHz;
– Duty cycle = 50 %;
– Load resistor = 70 Ohm;
– Shunt resistor = 0.1 Ohm;
– Gate resistor = 110 Ohm.

A. Simulation Results

The software used for the simulation has been LTspice because of the large number of existing models on the market and its great potential for analysis. The manufacturers of the transistors, have LTspice models available, so they will be used and validated experimentally in the different simulations.

Figure 10 shows the scheme that has been simulated. The transistor model has been changed for each specific case. The same happens with the capacitor C6, which represents the parasitic capacity of the panel, it has been modified between the values 680 nF and 1 µF to analyse the behaviour.

There are two components used that have not been detailed: R25 and C9.

R25 (R_{GATE}) limits the current to charge and discharge the

parasitic capacitance of the shunt transistor gate; therefore, it fixes the dynamics of the limiter. A small value thereof is interesting, since otherwise the response of the R25-Q5 loop becomes very slow so that the active current limitation would be unusable. However, a further decrease in resistance returns to the unstable system, as detailed in [8]. To compensate this problem, due to the resonance between the CMILLER of the transistor and the serial parasitic inductor thereof, the C9 capacitor is added, which reduces system instability. This fact is analysed in depth in [8] and [9].

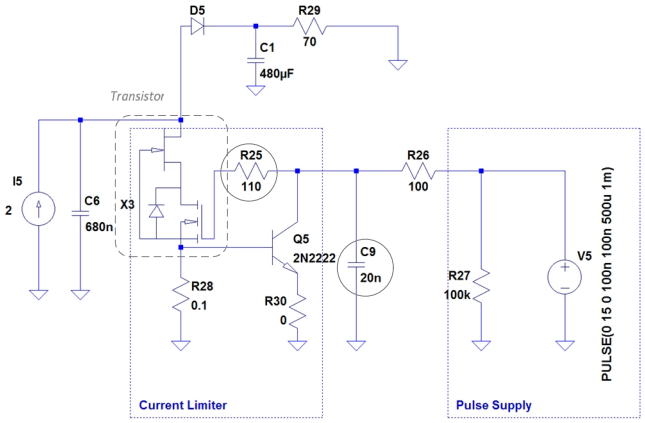


Fig. 10. Example of simulated S3R cell scheme in LTspice. In this particular case using the USCi transistor UJC1206K. C6 represents the parasitic capacity of the panel.

The simulation results are shown in Fig. 11.

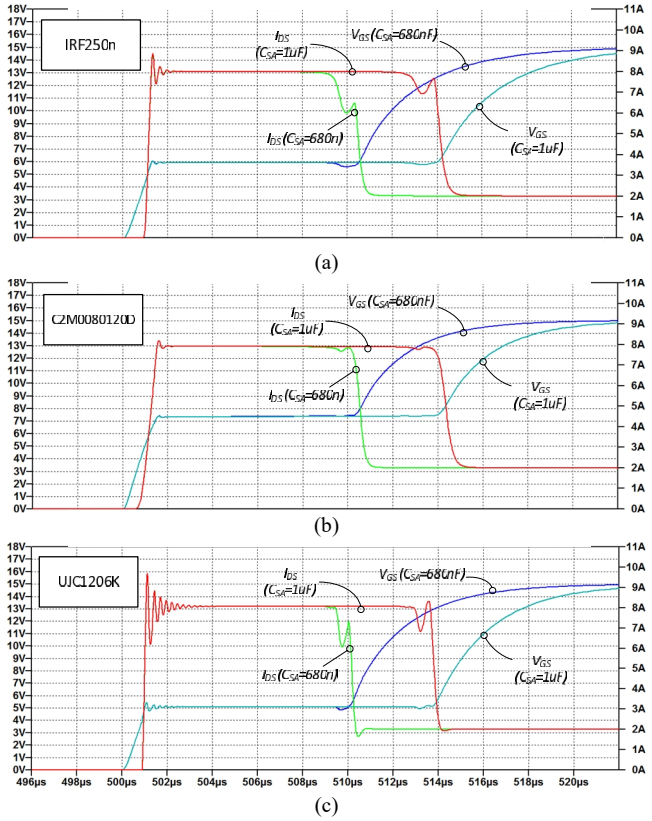


Fig. 11. Switch simulation result for the three types of transistors: (a) – IRF250n; (b) – C2M0080120D; (c) – UJC1206. For each type, two different capacities have been simulated: 680 nF and 1 µF. The legend is in the draw.

The three types of transistors have been simulated, modifying in each case the parasitic capacity of the panel to observe the effect on the current limitation. It is observed that regardless of the type of transistor used, the current limiting value is the same, approximately 8 A.

It is worth noting that the voltage V_{GS} of each type of transistor is different for its operation in linear zone, the UJC126K being the one with the lowest voltage. The reason is that it is a cascode and the government transistor is optimized, while the other two are conventional N-mosfet.

On the other hand, to emphasize the current overshoot that occurs in the limitation. It can be observed that in the case of the UJC1206 we have a greater overshoot than in all other cases, this is due to a greater inductance of the cascode source. Notably, despite having blocking voltages characteristics six times higher in the case of C2M0080120D and UJC1206K against IRF250n, very similar behaviours are observed. A slower dynamic response would be expected from a higher blocking voltage, however, in simulation they are very similar.

Of course, when the parasitic capacitance of the panel increases, the length of time the transistor remains in the linear zone to discharge it also increases, and therefore increases the temperature reached and the power dissipated.

B. Real Test Results

The tests performed on the real circuit are the same as those in simulation. The test consists on switching a S3R cell at a frequency of 1 kHz with different parasitic capacitances and analyse the operation of the current limiter. For testing, we have used the following equipment and components.

– Solar panel simulator E4351B – Agilent;
– Resistive load = 70 Ohm;
– Bus Capacitor = 480 µF – EPCOS (MKP);
– S3R diode = STTH6002C – ST;
– Switching frequency = 1 kHz;
– Shunt Resistor = 0.1 Ohm;
– Gate Resistor = 110 Ohm.

The bus capacitor is an especially critical so capacitors with low ESR and ESL are required. The capacitor used consists of 48 high performance 10 uF and 250 V EPCOS B32669 capacitors optimally positioned to minimize parasitic effects.

A complete period of the short-circuit phase of the solar panel using USCi UJC1206K is shown in Fig. 12.

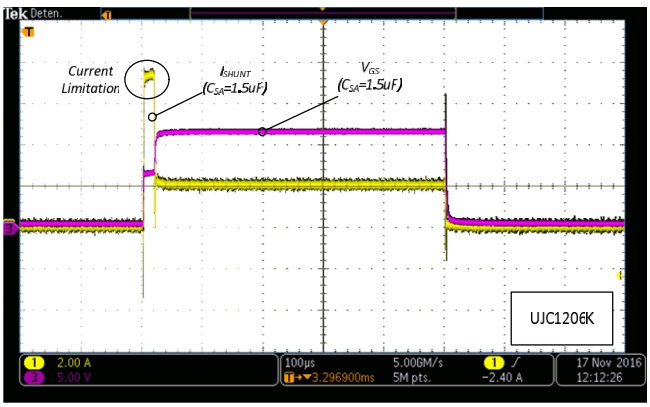
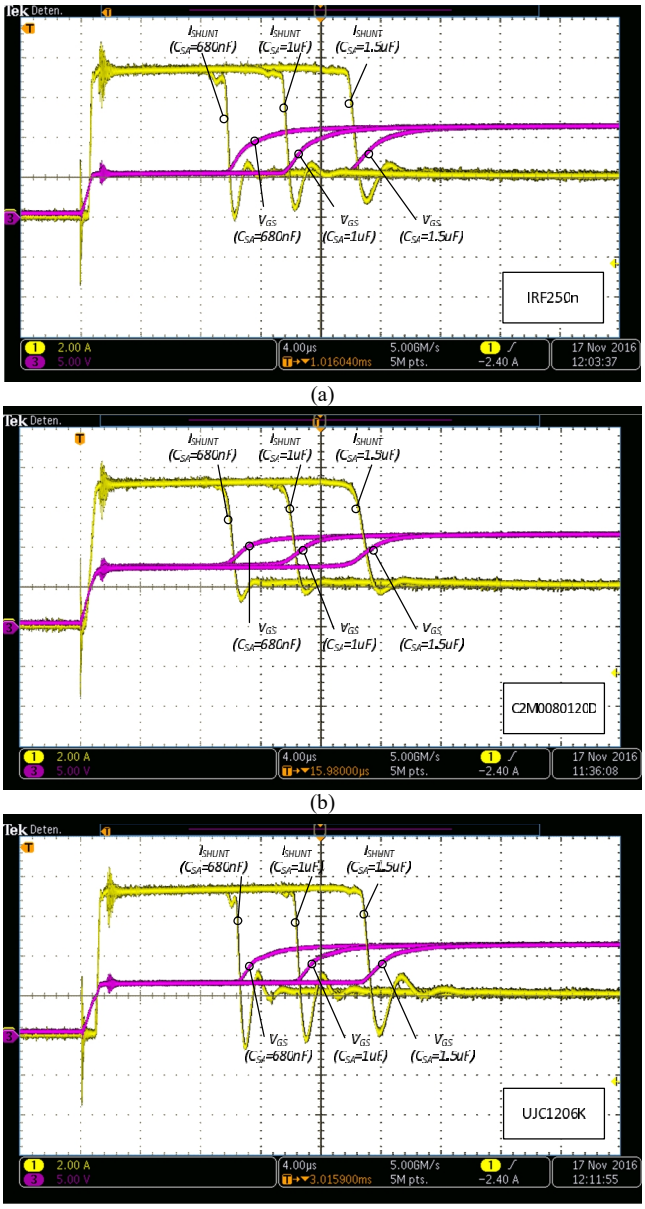


Fig. 12. Test result using USCi UJC1206K. The value of the parasitic capacity analysed is 1.5 µF. In yellow the current through the branch shunt and in violet the voltage V_{DS}.

It can be seen that the circuit of the active current limiter holds the transistor in the linear region for the time necessary so that the parasitic capacitance is discharged; limiting the current through it to the value defined in (9), in this case a value very close to 8 A.

Next, the current limiting phase for each proposed transistor type will be analysed by performing a sweep of the parasitic capacity of the panel. The results obtained are shown in Fig. 13.



(a)

(b)

(c)

Fig. 13. Result of the real test with the three types of transistors: : (a) – IRF250n; (b) – C2M0080120D; (c) – UJC1206. For each type, three different capacitances have been tested and are represented superimposed: 680 nF, 1 µF and 1.51 µF. For each draw the V_{DS} voltage for each tested parasitic capacity is shown in violet and the current through the shunt is yellow.

The three types of transistors proposed have been tested with three parasitic capacities of the panel (680 nF, 1 µF and 1.5 µF). In Fig. 13, it can be seen that the time that the transistor remains in the linear region limiting the current increases proportionally with the parasitic capacitance of the panel. This test confirms the similarity in the behaviour of the three tested types of transistors. There is no slower dynamic response on SiC transistors despite being able to block 1200 V. The three transistors react very quickly with a gate resistance of 110 Ohm and a 20 nF capacitor between the collector-emitter of the transistor Q5.

As shown in simulation the IRF250n transistor operating in a linear region has a voltage V_{GS} of 6 V, while C2M0080120D has a 7.5 V voltage and the UJC1206K have a 6 V. This makes the C2M0080120D to take longer to reach the limit current value, however, it is not appreciated that the transistor stays longer than the rest in linear zone. This is because the UJC1206K and IRF205n have a gate threshold voltage higher than C2M0080120D.

C. *Thermal Results*

To analyse the impact of the increase of parasitic capacitance in the shunt transistors, a thermal analysis has been done in order to measure the temperatures reached by the transistors due to its operation in linear zone. The expression that allows to calculate the power dissipated by the transistors is detailed in (8).

To know the temperatures reached in the transistors, their temperatures have been measured in steady state of operation using a thermographic camera. The three types of transistors analysed have TO247 encapsulation, so for analysis they have been installed on identical heatsinks, being isolated from them by means of a mica film.

The conditions of the test when measuring the temperature of the transistors, as well as the equipment used were:

– Solar panel simulator E4351B – Agilent;
– Thermographic camera Ti450 – Fluke;
– Average ambient temperature 24 ºC;
– Resistive load = 70 Ohm;
– Bus capacitor = 480 µF – EPCOS (MKP);
– S3R diode = STTH6002C – ST;
– Switching frequency = 1 kHz;
– Shunt resistor = 0.1 Ohm;
– Gate resistor = 110 Ohm.

Figure 14 shows the measurements taken for the different types of transistors and for each parasitic capacity of the solar panel.

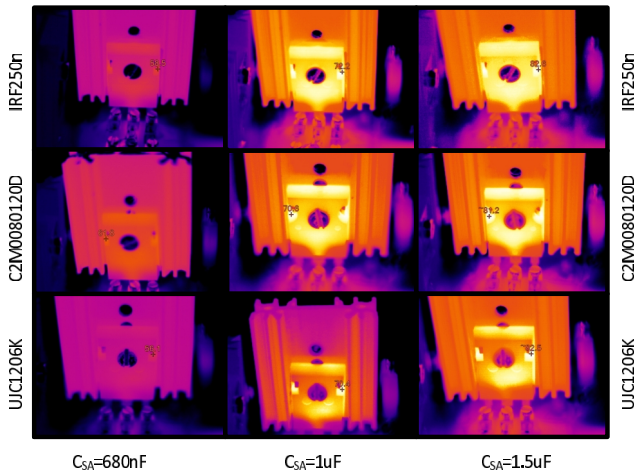


Fig. 14. Thermal analysis of the different transistors analysed for each parasitic capacity considered. The first row corresponds to the transistor IRF250n, the second to the C2M0080120D and the third to the UJC1206K. The first column corresponds to a CSA of 680 nF, the second one with 1 µF and the third with 1.51 µF.

TABLE II. TEMPERATURES REACHED.

Transistor	**Max. temperature (ºC)**		
IRF250n	58.5	72.2	82.6
C2M0080120D	61.8	70.6	81.2
UJC1206K	56.1	70.4	82.5
	C_{SA} = 680nF	**C_{SA} = 1uF**	**C_{SA} = 1.5uF**

As can be observed, the temperature of the transistors increases proportionally with the parasitic capacity, reaching maximum temperatures of 82.6 °C in the IRF250n case. Given that the maximum temperature set by the ECSS at the junction is 110 °C, the available transistors capable of withstanding higher temperatures is a matter of great importance. If the future satellites demand a higher energy, quite probable thing, the solar panels will be bigger with their corresponding increase of parasitic capacity. This is a problem because the transistor dissipation limit depends on maximum junction temperature. This could involve increasing the number of solar panel sections and therefore the number of cells S3R. This new set would have a higher mass and cost. On the other hand, it must be taken into account that in vacuum the heat dissipation is carried out exclusively by radiation, this decreases the dissipation capacity with the consequent increase in temperature.

V. CONCLUSIONS

In view of the results, it can be concluded that the tested SiC transistors are valid candidates for use in the S3R, both the UJC1206K cascode configuration and the C2M0080120D in the N-channel MOSFET.

It has been verified how the dynamics of the SiC transistors is very similar to that of the IRF250n, even in the case of the C2M0080120D seems slightly more stable.

Taking into account the temperatures reached by the transistors due to the dissipation of the energy stored in the parasitic capacities of the solar panels, it is logical to use semiconductors capable of operating at higher temperatures, as in the case of SiC.

Finally, we could analyse the reliability of the components used and their degradation with time [10], ts dependence on short-circuit versus temperature [11], and to single events [12]. In the case of UJC1206K, reliability cascodes 1200 V is justified to a greater extent due to the robustness of the JFET that blocks most of voltage. While in the case of C2M0080120D, insulation degradation gate should be analysed, since at such high voltages it could suffer premature deterioration.

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