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Design of an 8-bit 1GS/s F&I ADC in 0,13µm SiGe BiCMOS Technology

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Introduction

Ultra high-speed, medium-resolution analog-to-digital converters (ADCs) are required in wireless communication applications such as receivers, in optical digital system such as DVD, Blu-ray disk drivers, and in measurement instrumentation such as digital oscilloscopes and waveform recorders. The flash ADCs are widely used for high-speed conversion because of their parallel architectures. However, for *N*-bit flash ADC architecture needs 2^N-1 comparators, which consumes more power and occupies large die area. Folding-Interpolating (F&I) technique is another alternative to reduce the number of comparators with nearly the same conversion speed as flash [1, 2]. For these reasons, we chose the F&I architecture for our ADC.

Bipolar and BiCMOS technology F&I ADCs with resolutions of 8-bits and sampling speeds over 1 GHz have been reported [2-6]. In this work, the architecture of the 0,13 µm SiGe BiCMOS technology 8-bit 1 GS/s F&I ADC and simulation results of dynamic and static characteristics are presented.

F&I ADC Architecture

The presented ultra-high speed, 8-bit F&I ADC architecture shown in the Fig. 1. The F&I ADC consist of reference ladder, high 4-bits flash ADC and low 4-bits F&I ADC.

In low 4-bits F&I ADC architecture, the input signal U_{in} is applied to the input of 6 folding blocks in parallel where it is compared to the reference voltages generated by the resistor ladder. Analog processing is used by each folding block to transform the input signal into a phase-shifted sinusoid-like signal. These sinusoidal signals are applied to the two differential interpolating circuits to create an array of 60 equally phase-shifted sinusoids. After interpolation, array of 60 waves are combined in right order and summarized in the analog multiplier block. The outputs of the multiplier block are applied to a set of 15 comparators to translate the analog information into digital data. Finally a digital encoding logic is used to produce the four least significant bits (LSBs). The four most significant bits (MSBs) are obtained by a high 4-bits ADC with a simple flash structure.

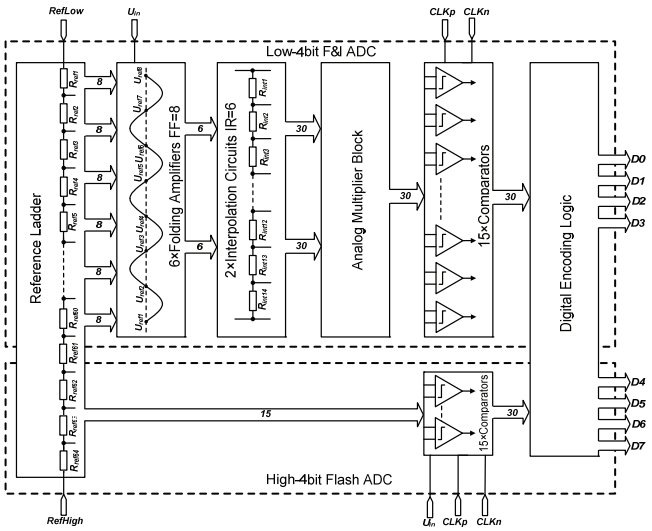

Fig. 1. Block diagram of 8-bit F&I ADC architecture

Details of ultra-high speed, 8-bit F&I ADC circuit design and simulation results are presented in the following sections.

Reference ladder

The set of reference voltages is usually generated through a resistive ladder. As already mentioned, the flash architecture requires 2^N-1 comparators for *N* bits of resolution, the same number of resistors is needed and for reference ladder. These resistors must be precise, carefully matched and properly biased to ensure that the reference voltages are linear.

In F&I ADC the step size of the reference ladder is larger than in a flash converter, because missing signals for comparators generate the interpolation block. In our case, the reference ladder consisting only of 64 resistors, to form the quantization levels for the input signal. The number of resistors depends on MSB, folding factor (FF) and interpolation rate (IR). The circuit diagram of the reference ladder is shown in Figure 2. The top level of the resistive ladder is connected to U_{refHigh} and the minimum level is connected to U_{refLow}. So, the full-scale range (1,8 Volts) of the F&I ADC is divided into 63 reference voltages.

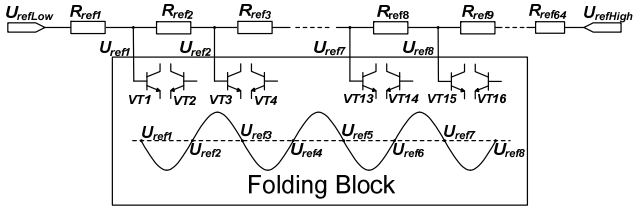

Fig. 2. Reference ladder circuit

The same reference ladder generates reference voltages both for LSB and MSB. The voltage difference between all MSB inputs must be equal, and voltage difference between all folding circuits must be equal also. The F&I ADC accuracy directly depends on reference ladder accuracy, so it should be very precise and linear as possible.

Folding block

The F&I ADC has the advantage of small number of comparators, low power consumption and die area, while the operating speed is same as that of flash ADC type. The number of comparators required is reduced by the folding factor. A high folding factor results in a low number of comparators, but on the contrary, it lowers the maximum input signal frequency of the ADC [1, 2]. The folding amplifier with folding factor of eight (FF=8) is shown in the Fig. 3.

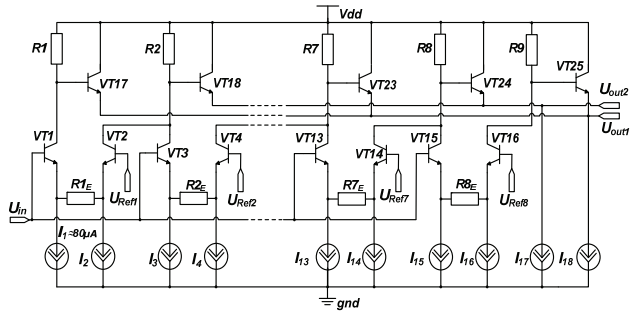

Fig. 3. Folding amplifier circuit

This circuit consists of eight differential pairs (the first pair consist of *VT1* and *VT2* transistors, the second - *VT3–VT4* and etc.). These differential pairs are used with cross coupling of odd and even numbered differential pair (collector of *VT2* is cross coupled with the collector of *VT3*). In this folding amplifier emitter-degeneration resistors $R1_E$–$R8_E$ are used to improve the linearity. The folding characteristic is obtained by analog wired-OR connection realized by *VT17* to *VT25*. This type of connection has the advantage of reducing the capacitances and the common mode current at the output node [3, 4].

Interpolation block

The differential outputs of the folding amplifiers are applied to the interpolation block to create an array of missing phase-shifted folding characteristics for comparators. In this F&I ADC design, interpolation block consist of two fully differential interpolating circuits, each of which is implemented using resistor voltage divider, because of its simplicity and power-efficiency. The interpolation rate (IR) of each circuit is equal to 6. So, each of the 6 folding amplifier outputs are used to drive a two resistive interpolation circuits, producing a total of 60 phase-shifted folding characteristics to drive comparators.

Analog multiplier block

The array of 60 signals, obtained from interpolation block, must be combined in pairs and in right order and summarized. For this purpose the multiplier block is used. The multiplier block is implemented using the Gilbert cell. The Gilbert cell operates as an exclusive OR (XOR) gate and as an analog multiplier with small input swings. Combined and summarized signals now are applied to a set of 15 high-speed comparators.

Comparators block

The high-speed comparator in the F&I ADCs is an essential functional block to compare the output signals of the interpolation circuit and quantize digital output codes. The comparator circuits used in this implementation is shown in Fig. 4. Basically this circuit consists of two parts: a preamplifier and a clocked latch.

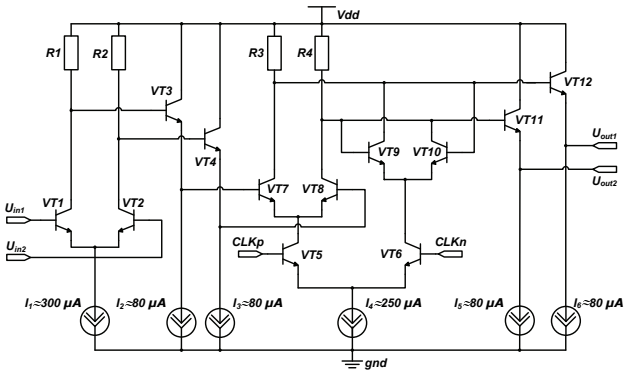

Fig. 4. Comparator circuits

The preamplifier consists of a low gain classical differential amplifier (*VT1* and *VT2*) with resistances as load (*R1* and *R2*) and emitter-followers (*VT3* and *VT4*). The preamplifier with resistive loads shows better linearity, offset and gain response than circuits with active or diode loads. Emitter-follower stages are used to level shift the signals between the clocked latch and the preamplifier.

The clocked latch consists of a differential pair (track pair, *VT7* and *VT8* transistors) that produces a differential voltage across resistors *R3* and *R4*, and second differential pair (latch pair, *VT9* and *VT10*), connected in a positive-feedback configuration and latches the differential signal. Two clock signals track (labelled as *CKLp* in Fig. 4) and latch (labelled as *CKLn* in Fig. 4) control the track pair and the latch pair through *VT5* and *VT6*, respectively. When track is high, the differential track pair tracks the preamplifier output and when latch is high, the latch pair establishes a positive feedback loop and amplifies the difference voltage between track pair output.

The clocked latch output consists of the emitter followers *VT11* and *VT12* that provide low output impedance for driving the following stage and improve the capacitance loading effect at output nodes.

Digital encoding logic

The last part of the F&I ADC is digital encoding logic. The cyclic thermometer code, generated by the comparators from both coarse and fine ADC parts is converted into binary code. Here must be taken care to match the delay through the coarse ADC and the delay through the rest of the circuitry (i.e., fine ADC). Therefore, the encoder is designed mainly form exclusive OR (XOR) elements and time delay blocks, unifying delay times.

Simulation results

The 8-bit F&I ADC circuits designed in the 0,13 µm SiGe BiCMOS technology with 2,5 V power supply has been simulated with Cadence Design Kit tools. Simulation indicates that power consumption is less than 70 mW. The fast Fourier transform (FFT) for an input frequency (f_{in}) of 1 MHz at 1 GS/s is shown in Fig. 5.

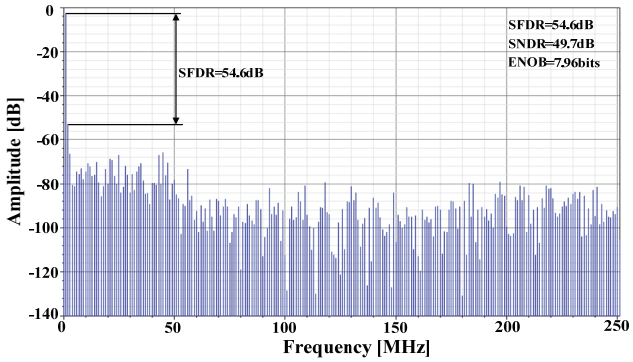

Fig. 5. Frequency spectrum for an input frequency of 1 MHz (sinusoid) at 1 GS/s

Fig. 6 shows the simulated curves of signal to noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) versus input signal frequency at 1 GS/s. It can be seen that the SNDR/SFDR achieves 49,7/54,6 dB at 1 MHz input and 37,15/39,45 dB at 500 MHz input, respectively.

Fig. 7 shows the plot of effective number of bits (ENOB) at different input frequencies when the ADC is clocked at 1 GS/s. The ENOB is around 8 bit at low frequency. At an input frequency of 500 MHz (up to Nyquist frequency), the ENOB drops to around 6-bit.

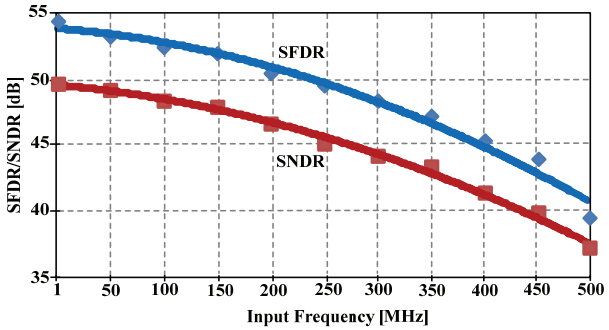

Fig. 6. SNDR and SFDR versus input frequency at 1 GS/s

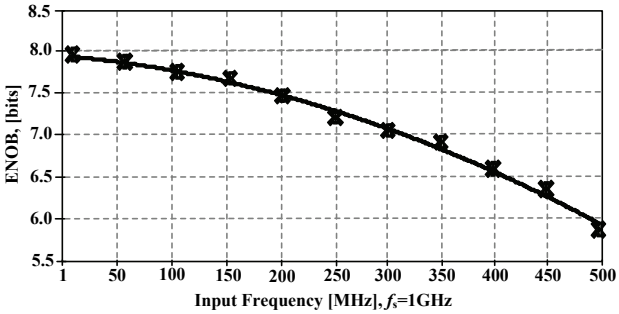

Fig. 7. ENOB versus input frequency at 1 GS/s

The integral nonlinearity (INL) and differential nonlinearity (DNL) of the ADC are illustrated in Fig. 8. From the graph, the maximum value of INL and DNL are ±0,59 LSB and ±0,38 LSB, respectively.

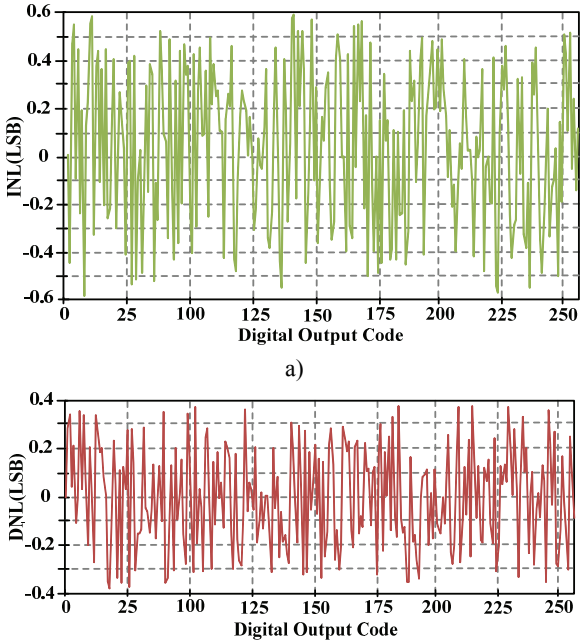

Fig. 8. Simulated static characteristics of ADC: a) INL; b) DNL

A summary of the simulated ADC performance is presented in Table 1.

Tabel 1. Performance summary

Technology	0,13 µm 2,5V SiGe BiCMOS
Architecture	Folding and Interpolation
Resolution	8-bit
Folding Factor (FF)	8
Interpolation Rate (IR)	6
Sampling Rate	1 GS/s
Power Supply	2,5 V
Power Consumption	<70 mW
SNDR@f_{in}=(1...500)MHz	(49.7…37.15) dB
SFDR@f_{in}=(1...500)MHz	(54.6…39.45) dB
ENOB@f_{in}=(1...500)MHz	(7.96…5.88) bit
INL	<±0,6 LSB
DNL	<±0,4 LSB

Conclusions

In this paper, an 8-bit 1 GS/s F&I ADC is designed in a 0,13 µm SiGe BiCMOS technology. It is composed of a high 4-bits flash ADC and low 4-bits F&I ADC. In the low 4-bits F&I ADC, folding amplifiers and interpolating circuits are used. The functionality of the designed F&I ADC is evaluated by simulation in Cadence using foundry provided models. The simulation results show that at 1 GS/s power consumption the ADC is less than 70 mW. The SNDR and SFDR of F&I ADC are greater than 37 dB up to 500 MHz at 1 GS/s, and the INL and the DNL are less than ±0,6 LSB and ±0,4 LSB, respectively.

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In this paper, design and simulation results of an 8-bit 1 GS/s clock speed folding and interpolating analog-digital converter (F&I ADC) are presented. The converter for four lower bits used folding with interpolation whose coefficients respectively equal to 8 and 6, and four upper bits made using parallel comparators structure. ADC design and simulations carried out with Cadence software packages. Dynamic characteristics of the converter are presented, which shows that signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) at 1 MHz input signal and 1 GS/s clock frequency is respectively equal to 49,7/54,6 dB. It is also identified effective number of bits (ENOB), which is approximately equal to 8-bit, when the input signal frequency is 1 MHz and at 500 MHz, ENOB drops to around 6-bit. After static characteristics simulation were got that the differential nonlinearity (DNL) did not exceed ±0,4 LSB and integral nonlinearity (INL) is less than ±0,6 LSB. Ill. 8, bibl. 6, tabl. 1 (in English; abstracts in English and Lithuanian).

V. Barzdėnas, D. Poviliauskas, G. Gražulevičius, K. Kiela. 0,13 µm SiGe BiKMOP technologijos 8 skilčių 1 GS/s sąsūkos ir interpoliacijos ASK projektavimas // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2012. – Nr. 6(122). – P. 55–58.

Darbe pateiktas suprojektuotas 0,13 µm SiGe BiKMOP technologijos, 8 skilčių bei 1 GS/s taktinio dažnio, sąsūkos ir interpoliacijos analoginis-skaitmeninis keitiklis (ASK). Šio keitiklio keturioms žemesniosioms skiltims panaudota sąsūka su interpoliacija, kurių koeficientai atitinkamai lygūs 8 ir 6, o keturios aukštesniosios skiltys sudarytos panaudojus lygiagrečiąją komparatorių struktūrą. ASK projektavimas ir modeliavimas atlikti su Cadence programiniu paketais. Pateikiamos dinaminės keitiklio charakteristikos, kuriose matyti, kad signalo, triukšmo bei iškraipymų santykis (SNDR) ir dinaminis diapazonas be klaidingų išėjimo harmonikų (SFDR), esant 1 MHz įėjimo signalui ir 1 GS/s taktiniam dažniui, yra atitinkamai lygūs 49,7/54,6 dB. Tačiau padidinus įėjimo signalo dažnį iki 500 MHz, šie koeficientai sumažėja iki 37,15/39,45 dB. Taip pat nustatytas ir efektyviųjų skilčių skaičius (ENOB), kuris apytikriai lygus 8, kai įėjimo signalo dažnis yra 1 MHz, o esant 500 MHz ENOB sumažėja iki 6. Atlikus statinių charakteristikų modeliavimą nustatyta, kad keitiklio diferencialinis netiesiškumas (DNL) neviršijo ±0,4 LSB, o integralinis netiesiškumas (INL) buvo mažesnis nei ±0,6 LSB. Il. 8, bibl. 6, lent. 1 (anglų kalba; santraukos anglų ir lietuvių k.).