A Novel Super Transistor-Based High-Performance CCII and Its Applications

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Abstract**—**In this paper a high-performance low-voltage low-power CMOS second-generation current conveyor (CCII) is presented. The proposed CCII is based on super transistor (ST) and enables low input impedance at X terminal and high output impedance at Z terminal. It also utilizes a novel power saving strategy in which a single NMOS cascode current mirror conveys X terminal current to Z terminal, provides high impedance at Z terminal and reduces the X terminal impedance all together resulting in a low-power and compact structure. As another advantage, only NMOS transistors are used in processing voltage and current signals granting the proposed CCII high frequency operation. PMOS transistors are used only for biasing. However, the proposed CCII cannot provide infinite impedance at Y terminal. HSPICE simulations using 0.18 μm parameters and supply voltage of ±0.9 V confirms that the proposed CCII exhibits impedances of 0.155 Ω, 1.6 MΩ and 47 kΩ at X, Z and Y terminals, respectively. Voltage and current bandwidths are also 377 MHz and 159 MHz, respectively. Some of the applications of the proposed CCII are given.

*   ***Index Terms**—**Current-mode circuits; Analog integrated circuits.***

I. INTRODUCTION

In the last decade, current-mode (CM) signal processing has become very popular [1]–[20]. It provides innovative solutions to solve the problems of analog circuits in modern technologies and shows many advantages compared to conventional voltage-mode (VM) approach. Especially, current-mode technique allows realizing low-voltage, wide dynamic range and large bandwidth analog circuits and alleviates the problems of constant gain bandwidth product [1]–[20].

One of the most important current-mode building blocks is second-generation current conveyor (CCII) (Fig. 1) which finds many applications in implementing filters, instrumentation amplifiers, voltage and current amplifiers, oscillators etc. [3]–[14]. Moreover, having one high impedance input, one low impedance input and one high impedance output, it can operate in both current and voltage modes, which provides flexibility and enables variety of circuit designs.

The voltage applied to terminal Y of CCII is replicated to its X terminal. The current supplied to X terminal is conveyed to the high impedance output terminal Z with

either positive (CCII+) or negative polarities (CCII-). Therefore, X and Y terminals exhibit very low (ideally zero) and very high (ideally infinite) impedances, respectively. However non-ideal impedances at X and Z terminals and other parasitic elements limit the performance of CCII [19]. Furthermore, CCII's frequency performance directly determines the frequency performance of all circuits implemented with CCIIs. Consequently, a high-performance CCII (with high bandwidth, very low impedance at X terminal and very high impedance at Z terminal) are needed to improve the performance of CCII based circuits. However, the demand for low-voltage low-power operation [21] makes the design of such a high performance CCII very challenging.
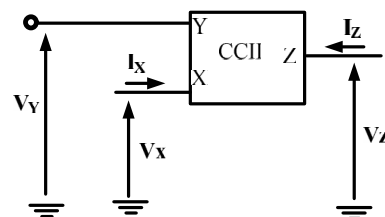

Fig. 1. CCII symbol.

$$\begin{bmatrix} I_Y \\ \cdot \\ V_X \\ \cdot \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ & \cdot & \\ \beta & 0 & 0 \\ & \cdot & \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ \cdot \\ I_X \\ \cdot \\ V_Z \end{bmatrix}. \quad (1)$$

Literature survey shows that the previously reported CCIIs are mainly based on differential pair/transconductance and translinear topologies [3]–[4], [14], [15], [18], [22], [23]. In CCIIs made of differential pairs, a high gain negative feedback loop is used to reduce impedance at X terminal. In this approach, low impedance at X terminal, infinite impedance at Y terminal and wide frequency bandwidths (for both voltage and current signals) are achieved. However most of the CCIIs made of differential pair (or transconductance amplifier) topologies suffer from low impedance at Z terminal [3], [4], [12], [22]. Most importantly the impedance at X terminal starts to increase at frequencies much lower than voltage and current bandwidths. On the other hand, CCIIs based on translinear topology are not suitable for low voltage designs because they require large supply voltage of at least $2V_{GS} + 2V_{DS}$ (with usual meaning of symbols) [15] and low impedance at

X terminal is achievable at the cost of high power consumption. In addition, they suffer from low impedance at Z terminal and poor frequency performance because both P-type and N-type current mirrors are present in the signal path.

In this paper, a new topology to design high-performance CCII is proposed. The proposed topology is based on super transistor (ST) and enables very low input impedance and very low offset voltage at X terminal and high output impedance at Z terminal. Unlike differential pair topology, impedance at X terminal remains low even at high frequencies. The proposed topology includes an interesting power saving strategy in which a single NMOS cascode current mirror serves three functions simultaneously; it conveys X terminal current to Z output, provides high impedance at Z terminal and helps further reducing the X terminal impedance by establishing a negative feedback loop. Consequently, the proposed CCII enjoys a compact structure. As another advantage, only NMOS transistors are used in processing voltage and current signals granting the proposed CCII high frequency operation. However, similar to translinear based CCIIs, its impedance at Y terminal is not infinite. As application examples, the proposed CCII, is used in implementing a current-mode instrumentation amplifier, an electronically variable voltage amplifier and an electronically variable current amplifier. This paper is organized as follows: In Section II the proposed CCII circuit and its HSPICE simulation results using 0.18 μm TSMC CMOS technology are presented. Thereafter, CCII applications are discussed in Section III. The paper is concluded in Section IV.

II. THE PROPOSED CCII

A. Circuit Description

The proposed topology is based on STs which have been used in voltage-mode signal processing to improve the output resistance and linearity of source-degenerated differential CMOS transconductors [24]. In current-mode signal processing, they have been used to design a high-performance voltage feedback current amplifier [2].

The implementation and symbol of a ST is shown in Fig. 2. It has three interesting characteristics making them highly suitable to design other current-mode building blocks especially CCIIs:

First, they exhibit very low input impedance at source terminal expressed as [24]

$$r_s \approx \frac{1}{g_{mA1} g_{mA2} g_{mA3} (r_{oA1} \| r_{oIB2})(r_{oA2} \| r_{oIB3})}. \quad (2)$$

Second, they show high voltage tracking accuracy between gate and source terminals. Voltage gain between source and gate terminals is expressed as [24]

$$A_v = \frac{v_s}{v_g} \approx \frac{1}{1+[g_{mA1}(r_{oA1} \| r_{oIB2})g_{mA2}(r_{oA2} \| r_{oIB3})]^{-1}} \approx 1. \quad (3)$$

Third, the output impedance seen from their drain is very high and is described by [24]

$$r_d \cong g_{mA1} g_{mA2} g_{mA3} (R)(r_{oA1} \| r_{oIB2})(r_{oA2} \| r_{oIB3})(r_{oA3}), \quad (4)$$

where R is the equivalent resistance connected to the source node. In (2)–(4) g_m and r_o denote the transconductance and output impedance of the related transistor or current source, respectively.
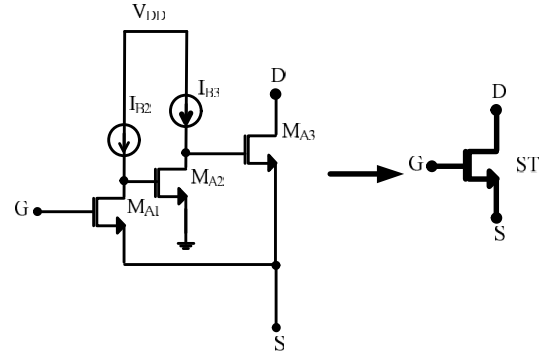

Fig 2. Implementation and symbol of Super Transistor [24].

For typical parameter values; r_s, A_v and r_d are in Ω, unity and GΩ ranges, respectively. These interesting features lead us to consider a single super transistor as a high performance CCII as is shown in Fig. 3 which has very low impedance at X terminal, close to unity gain between Y and X terminals and very high output impedance at Z terminal. Despite the intrinsic capacity of STs to operate as a CCII, up to now, they have not been employed in the structure of current conveyors. Here for the first time, we employ ST as the core part of a high performance CCII.
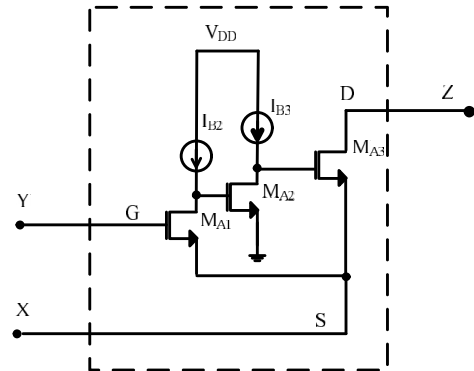

Fig 3. Super Transistor as a CCII.

As it is seen from Fig. 3, there is a DC level shift equal to V_{GSMA1} between Y and X terminals. Transistor M_{A3} also requires DC bias current. Therefore, some modifications in Fig. 3 are needed to make it a high performance CCII. Fig. 4 shows the simplified schematic of the proposed CCII which is made up of only 8 NMOS transistors (excluding bias circuitry). Transistor M_1 which is identical to M_{A1} is used to reduce DC offset voltage between Y and X terminals. For DC input, a simple analysis shows that gate voltage of M_1 and V_X can be expressed as:

$$V_{GM1} = V_Y + V_{GSM1}, \quad (5)$$

$$V_X = V_{GM1} - V_{GSMA1} = V_Y + V_{GSM1} - V_{GSMA1}. \quad (6)$$

Therefore, for $V_Y \approx 0$, offset voltage can be found as

$$V_{off} = V_X - V_Y = V_X = V_{GSM1} - V_{GSMA1}, \quad (7)$$

which can be expressed as (Appendix-A)

$$V_{off} \approx \frac{K \times \lambda}{2} \left(V_{DSMA1} - V_{DSM1} \right). \qquad (8)$$

Evidently, low offset voltage can be achieved by making V_{DSMA1} as close as possible to V_{DSM1}.

In Fig. 4 current sources I_{B2} and I_{B3} should be equal to provide matching between M_1 and M_{A1}. In addition, current sources I_{B1} and I_{B2} should also be equal because any difference between I_{B1} and I_{B2} will appear as an offset current at Y terminal.
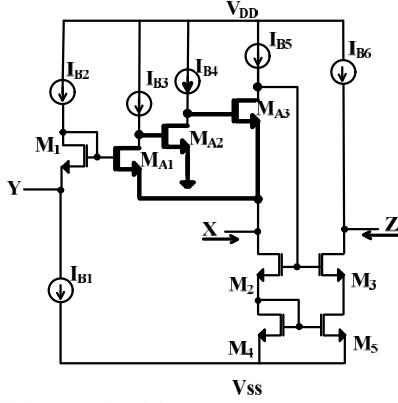

Fig. 4. Simplified schematic of the proposed CCII.

By performing a simple small-signal analysis and using (3), voltage transfer between Y and X terminals can be expressed as (Appendix-B)

$$\frac{V_X}{V_Y} \approx \frac{g_{m1} r_{oIB2}}{1 + g_{m1} r_{oIB2}} \approx 1, \qquad (9)$$

where g_{mi} and r_{oIBi} are transconductance and output resistance of related transistor and current source, respectively.

If we neglect the effect of negative feedback established by M_2–M_5 and only consider the effect of super transistor, the impedance at X terminal can be expressed as (2) (by replacing r_{oIB2} and r_{oIB3} with r_{oIB3} and r_{oIB4}, respectively). However, if a single transistor (g_{mA1}) is used instead of super-transistor, the impedance at X terminal will be

$$r'_X \approx \frac{1}{g_{mA1}}. \qquad (10)$$

Considering (9) and comparing (2) and (10), shows that innovative use of super transistor not only increases the voltage transfer accuracy between X and Y terminals, but it results in a significant reduction in X terminal impedance.

Cascode current mirror formed by transistors M_2–M_5 serves three vital functions:

First; it duplicates the current in the X terminal to the Z output (assuming that $I_{B3} + I_{B5} = I_{B6}$).

Second; it provides high impedance at Z terminal.

Third; it forms a negative feedback loop that further reduces the impedance at X terminal.

As it can be seen, several important features are provided by only 4 transistors resulting in low power consumption, compact and easy to design structure.

By considering the effect of negative feedback formed by M_2–M_5 transistors and using (2), the overall impedance at X terminal is found as:

$$r'_X \approx \frac{(1 + g_{m2} g_{m4}^{-1})}{g_{mA1} g_{mA2} g_{mA3} (r_{oA1} \| r_{oIB3})(r_{oA2} \| r_{oIB4}) r_{oIB5} g_{m2}}. \qquad (11)$$

From (11), it is evident that the proposed CCII enjoys very low impedance at X terminal.

Complete schematic of the proposed CCII is shown in Fig. 5 in which ideal current sources are implemented by simple current mirrors made of transistors M_{B0}–M_{B7}. Besides, transistors M_6–M_9 and current source I_{off} are used to provide DC current for M_2-M_5 transistors. Cascode structures made of transistors M_2–M_5 and M_6–M_9 at the output branch are used to increase impedance at Z terminal. Analysing circuit of Fig. 5, the impedance at Z terminal is found as

$$R_Z \cong (g_{m3} r_{o3} r_{o5}) \| (g_{m6} r_{o6} r_{o7}). \qquad (12)$$

The impedance at Y terminal is also found as

$$R_Y \cong r_{oB7} \| (g_{m1}^{-1} + r_{oIB2}). \qquad (13)$$

As it is seen from (13), the impedance at Y terminal is not infinite. Limited impedance at Y terminal can only cause a negligible reduction in β value of CCII. By considering R_Y, the amount of reduction will be

$$K = \frac{R_Y}{R_Y + R_S}, \qquad (14)$$

where R_S is the internal impedance of voltage source connected to Y terminal. As R_S is in ohm range, and R_Y is in kohm range, therefore, $K \approx 1$ and the limited impedance will not have a serious effect on CCII's performance. However, if larger impedances at Y terminal is required, simple current mirrors used for biasing, can be replaced with high output impedance cascode type current mirrors.
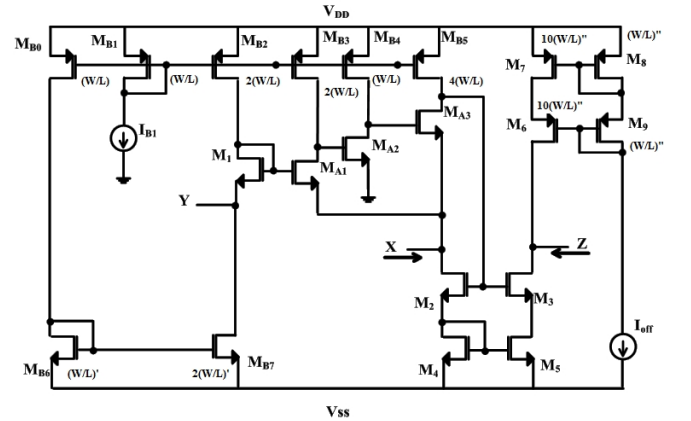

Fig. 5. Complete schematic of the proposed CCII.

B. Simulation Results

Performance of the proposed circuit of Fig. 5 is verified by HSPICE simulations using 0.18 μm TSMC CMOS process parameters under supply voltage of ±0.9 V. Transistors aspect ratios are reported in TABLE I. According to the transistors aspect ratios shown in Fig. 5, to satisfy $I_Z = I_X$ we should have $10 \times I_{off} = 6 \times I_{B1}$. The values of I_{B1} and I_{off} are set at 15 μA and 9 μA respectively. A compensation capacitor of 0.4 pF is also added between gate and drain of M_{A3} for frequency compensation.

DC transfer characteristic of X terminal voltage (V_X) against input voltage at terminal Y (V_Y) (shown in Fig. 6) is achieved while Z terminal is connected to ground. Figure 6(a) shows that maximum and minimum voltage limits at terminal X are 350 mV and −350 mV, respectively. Figure 6(b) shows that DC offset voltage at X terminal for $V_Y=0$ is also negligible value of 5.6 µV.

Figure 7 shows error voltage between X and Y terminals for different values of V_Y. Favourably, error voltage between X and Y voltage remains below 25 mV. In Fig. 8 an input sinusoidal voltage having amplitude of 100 mV and frequency of 100 kHz, is applied to Y node, and the resulting signal on X-terminal is observed. THD is only 0.31 %. By increasing frequency, the value of THD reaches to 0.23 % and 0.21 % at 1 MHz and 10 MHz, respectively.

TABLE I. TRANSISTORS ASPECT RATIOS.

Transistors	W(µm)	L(µm)
$M_{B0}, M_1, M_{A1}, M_{B4}$	18	0.27
M_{A3}, M_{B1}	18	0.27
M_{B2}, M_{B3}	36	0.27
M_{A2}	9	0.27
M_{B5}	72	0.27
M_{B6}	1.8	0.27
M_2, M_3	9	0.36
M_4, M_5	5.4	0.54
M_6, M_7	36	0.36
M_8, M_9	3.6	0.36
M_{B7}	3.6	0.27
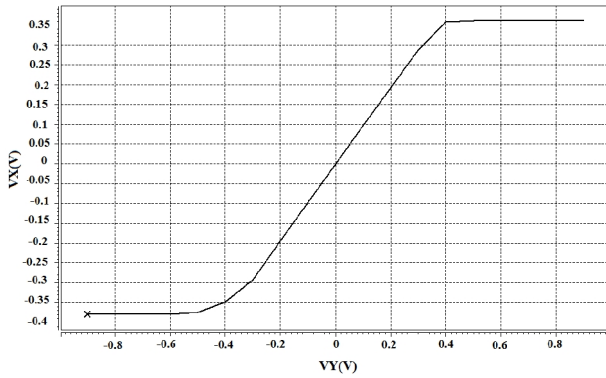
(a)
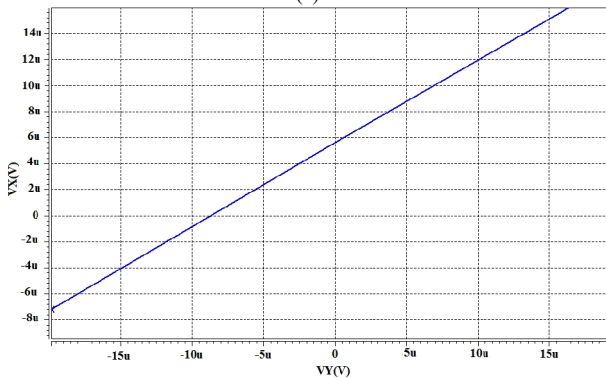
(b)

Fig. 6. V_X versus V_Y changing from a) -0.9 V to +0.9 V b) around 0 V.

The change in the Z terminal output current against the X terminal input current is also shown in Fig. 9 in which I_X is changed from −85 µA to +85 µA. Favourably, the input impedance at X terminal is 0.155 Ω which is very close to the ideal value of zero. Such low input impedance at X terminal is a direct result of using super transistor according

to (11). The impedance at Z and Y terminals are 1.6 MΩ and 47 kΩ, respectively. Total power dissipation is also 0.451 mW.
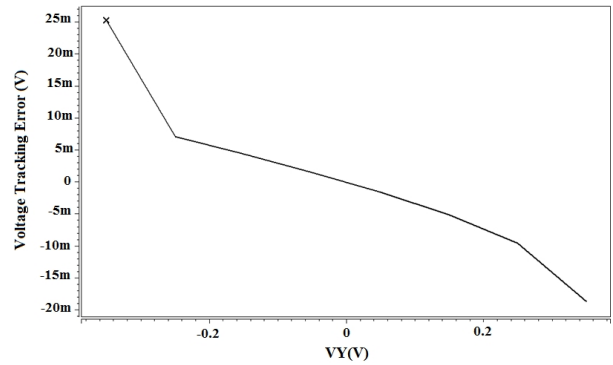

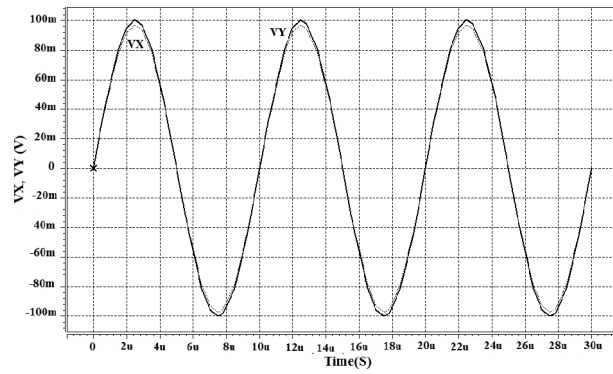Fig. 7. Voltage Error between V_X and V_Y.
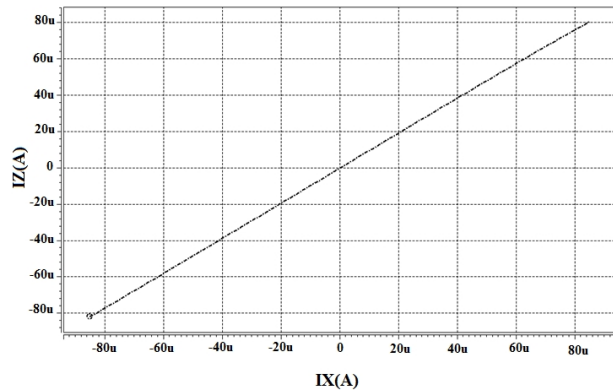

Fig. 8. V_X and V_Y in time domain.

Fig. 9. I_Z versus I_X.

The frequency response of (V_X/V_Y) is shown in Fig. 10 where, V_Y is the AC signal, X terminal is open circuited and Z terminal is grounded. The proposed CCII has a wide voltage gain -3 dB bandwidth of 377 MHz with a gain of 0.969. As it is seen, the voltage transfer response shows a peak of 2 dB. If a flat response is required, the value of compensation capacitor should be increased to 1 pF, however it will result in degradation in frequency performance. Figure 11 shows the frequency response of I_Z versus I_X where, Y and Z terminals are connected to ground and AC current signal is applied to X terminal. The proposed CCII exhibits a current gain -3 dB bandwidth of 195 MHz and current transfer gain of 0.965. The resulted high frequency performance is due to the fact that only NMOS transistors are used in processing voltage and current signals. In addition, they are all included in negative feedback loop which further improves frequency performance.
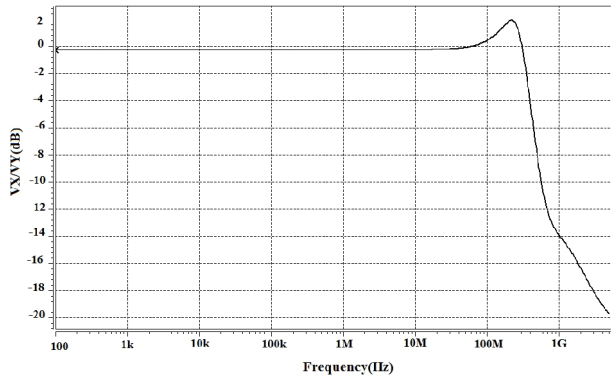
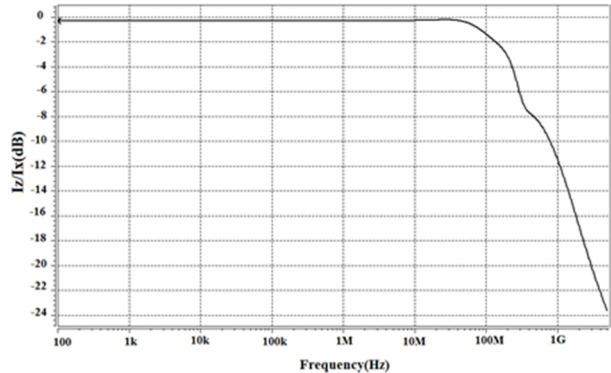Fig. 10. Frequency response of voltage transfer gain.

Fig. 11. Frequency response of current transfer gain.

Overall characteristic of the proposed CCII is compared with previously reported works in Table II. As it is seen, although CCII of [3] exhibits impedance of less than 7 Ω at X terminal, but it suffers from low voltage and current bandwidths of 10.5 MHz and 6.2 MHz, respectively. The CCII of [4] enjoys high voltage and current bandwidths but it exhibits low impedance of 147 kΩ at Z terminal and consumes 1.3 mW. The low power CCII of [12] exhibits wide voltage bandwidth of 10 GHz, but its current bandwidth is only 32 MHz. The CCII of [15], exhibits moderate frequency performance, consumes high power consumption and exhibits high impedance of 47 Ω at X terminal. The CCII of [18] also exhibits Rx value of 11.4 Ω, poor frequency performance of 16 MHz and requires high supply voltage of ±1.5 V. The proposed CCII exhibits very low impedance at X terminal which is at least 45 times smaller than that of [3], [4], [12], [15], [18], [22], [23]. Its offset voltage at X terminal is only 5.6 µV which is the smallest one in Table II. Its output impedance is 1.6 MΩ and comparable to [15] but much larger than [4]. The output impedance is high enough to enable easy cascading, however it can further be improved by utilizing another ST at output branch. The proposed CCII's power consumption is two times larger than those of [3], [12], [18] but much smaller than [4], [15]. Compared to [22], [23], the proposed CCII has better frequency performance and lower input (X terminal) impedance. As it is seen in Table II, the proposed CCII has not very high impedance at Y terminal but as it will be shown, this property will not cause any problem in most of the applications.

III. APPLICATIONS OF THE PROPOSED CCII

In this section, applications of the proposed CCII as an instrumentation amplifier, a variable-gain voltage amplifier and a variable gain current amplifier are given. In all of these applications the advantage of using high performance CCII is obvious.

A. Instrumentation Amplifier

Figure 12 shows the application of the proposed CCII to implement instrumentation amplifier of [9]. If both CCIIs are well matched and have precise voltage tracking between their Y and X terminals, high common-mode rejection ratio (CMRR) is provided. Unlike conventional voltage-mode instrumentation amplifiers, this circuit does not rely on any external resistor matching to achieve high CMRR, however ultimate limit on CMRR is determined by the mismatch between $CCII_1$ and $CCII_2$. The differential-mode voltage gain and output impedance can be described as:

$$V_{out} = \left(\frac{R_{Y1}}{R_{Y1}+R_S}\beta_1 V_{in+} - \frac{R_{Y2}}{R_{Y2}+R_S}\beta_2 V_{in-}\right)\alpha_1\beta_3 \frac{R_2\|R_{Y3}}{R_1+R_{X1}+R_{X2}}, \quad (15)$$

$$R_{out} = R_{x3}, \quad (16)$$

where R_{x3} is the x-terminal impedance of $CCII_3$, R_{Y1}, R_{Y2} and R_{Y3} are impedances at Y terminal of $CCII_1$, $CCII_2$ and $CCII_3$, respectively, and R_{S1} and R_{S2} are the internal impedances of voltage sources V_{in+} and V_{in-}, respectively. As $R_{Y3} \gg R_2$, $R_{Y1} \gg R_{S1}$, $R_{Y2} \gg R_{S2}$, R_{x1} and $R_{x2} \ll R_1$, and $\alpha, \beta \approx 1$, (15) can be expressed as

$$\frac{V_{out}}{V_{in+}-V_{in-}} \cong \frac{R_2}{R_1}. \quad (17)$$

In order to verify the performance of the instrumentation amplifier of Fig. 12, R_1 is set to 0.1 kΩ, while R_2 is varied from 0.1 kΩ to 5 kΩ. Figure 13 shows that while DC differential gain varies from 0 dB to 33 dB, -3 dB bandwidth varies only from 67 MHz (for gain of 0 dB) to 53 MHz (for gain of 33 dB). The -3 dB bandwidth proves to be approximately constant at high frequency for different gain values.

CMRR frequency performance is also shown in Fig. 14. As it can be seen, the instrumentation amplifier of Fig. 12 exhibits CMRR of 83 dB with -3 dB bandwidth of 613 kHz for different values of R_2.
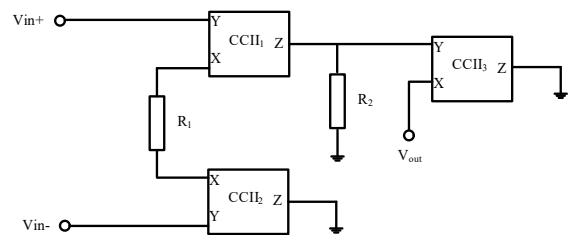

Fig. 12. Application of the proposed CCII as instrumentation amplifier [9].

For instrumentation amplifier application, using the proposed CCII results in three major improvements:

1. High CMRR because of the proposed CCII's high accuracy in transferring input signals from Y terminal to X terminal which is achieved because of the used super transistor.

2. Very low output impedance of 0.155 Ω because of very low impedance at X terminal which is achieved because of the used super transistor and negative feedback loop.

3. High frequency performance due to the high frequency performance of the proposed CCII.

TABLE II. COMPARISON BETWEEN PROPOSED CCII AND OTHER RECENT WORKS.

Parameters	[3]	[4]	[12]*	[15]	[18]	[21]	[22]	Proposed
Rx(Ω)	<7	9.6	15	42	11.4	200	27	0.155
Rz (MΩ)	NA	0.147	NA	2.24	7.2	0.560	0.89	1.6
RY	∞	∞	∞	147 kΩ	∞	∞	∞	47 kΩ
Vx/Vy BW(MHz)	10.5	810	10000	87	16	99	14	377
Iz/Iy BW(MHz)	6.2	915	32	70	NA	94	13	195
Offset voltage at X(mV)	<2.5	0.8	NA	0.2	NA	NA	NA	0.0056
PD(mW)	0.213	1.3	0.234	2.24	0.210	1.5	0.064	0.451
Technology (μm)	0.35	0.35	0.5	0.8	0.35	0.13	0.18	0.18
Input Voltage dynamic range (mV)	±650	(-1.43)-(+1.1)	(-0.63)-(+0.34)	NA	(-1)-(+0.9)	1.5	±380	±350
Input current dynamic range (μA)	±1000	±3000	±100	NA	NA**	NA	±7	±80
No. of transistors	22	20	14	28	21	25	36	21
Supply Voltage (V)	±0.75	±1.65	±1.5	3.3	±1.5	1.5	±0.4	±0.9

Note: *low power wide band version, ** Not Available.

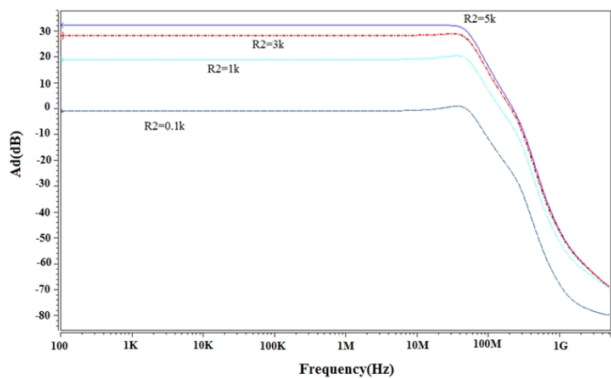Fig. 13. Frequency response of Differential-Gain of Fig. 12 for $R_1 = 0.1$ kΩ and different values of R_2.

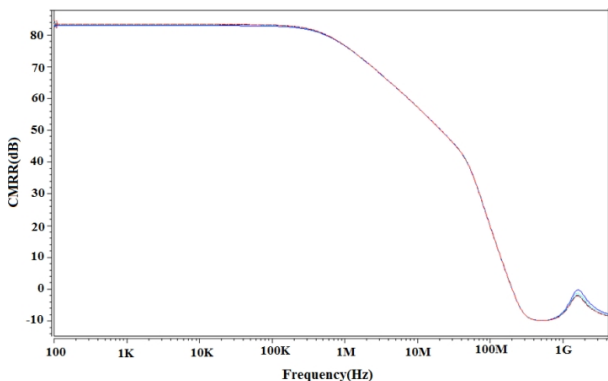Fig. 14. Frequency response of CMRR for $R_1 = 0.1$ kΩ and different values of R_2.

B. Variable Gain Voltage Amplifier

Figure 15 shows a variable-gain voltage amplifier implemented by the proposed CCII. The input voltage applied to Y_1 terminal is transferred to X_1 terminal, where it is translated to current by R_1. The output voltage and output impedance can be simply derived as:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{R_{Y1}}{R_{Y1}+R_S}\beta_1 \propto_1 \beta_2 \frac{R_2 \| R_{Y2}}{R_1} \approx \frac{R_2}{R_1}, \quad (18)$$

$$R_{out} = R_{x2}, \quad (19)$$

where R_{x2} is the X terminal impedance of $CCII_2$. To have electronic control, a variable resistor [17] is used as R_1. Therefore, the value of voltage gain can be set by control voltages V_A and $-V_A$ resulting in a high-performance electronically tunable voltage amplifier.

Figure 16 shows the frequency performance of the proposed voltage amplifier. As it can be seen from Fig. 16,

−3 dB bandwidth of the proposed voltage amplifier varies between 97 MHz to 85 MHz for different voltage gains from 10 dB to 28 dB respectively. It also exhibits very low output impedance of only 0.155 Ω.
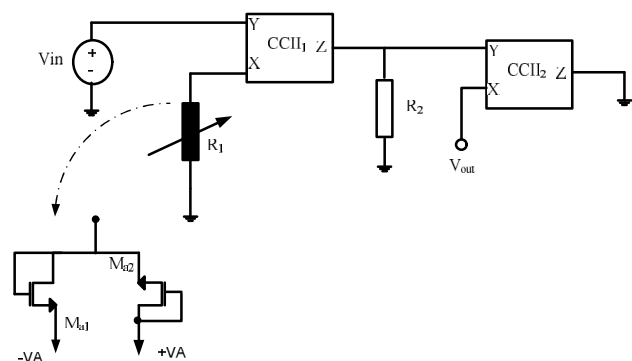

Fig. 15. Application of the proposed CCII as a high-performance variable-gain wide-bandwidth voltage amplifier.
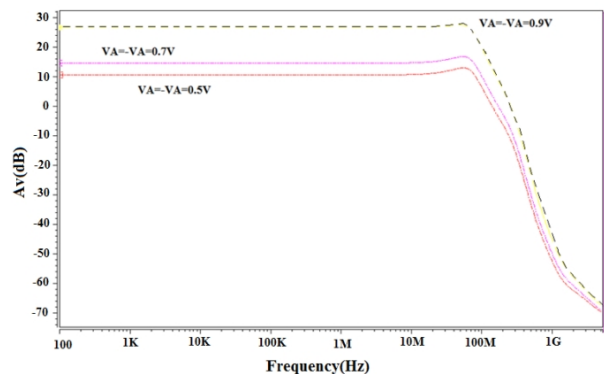

Fig. 16. Gain frequency response of the voltage amplifier of Fig. 15.

Using the proposed CCII in voltage amplifier application results in two major improvements:
1. Low output impedance equal to the X terminal impedance of the proposed CCII.
2. Very wide bandwidth as a result of the proposed CCII's high-frequency performance.

C. Variable Gain Current Amplifier

A CCII based variable-gain current amplifier is shown in Fig. 17. In current amplifier of Fig. 17, the input current applied to the low impedance X_1 terminal is transferred to the Z_1 terminal, where it is translated to voltage by R_1. The voltage produced at Z_1 terminal is copied to the X_2 terminal where it is converted again to current by R_2. The current

produced at R_2 is copied to output terminal (Z_2). The current gain, output and input impedances can be simply derived as:

$$A_i = \frac{i_{out}}{i_{in}} = \propto_1 \beta_2 \propto_2 \frac{R_1 \| R_{Y2}}{R_2 + R_{x2}} \approx \frac{R_1}{R_2}, \quad (18)$$

$$R_{out} = R_{z2}, \quad (19)$$

$$R_{in} = R_{x1}, \quad (20)$$

where R_{z2} is the Z terminal impedance of $CCII_2$. A variable resistor [17] is used as R_1 to provide electronic tuning capability for the proposed CCII-based current amplifier. In Fig. 17, current gain can be tuned by control voltages V_A and $-V_A$.
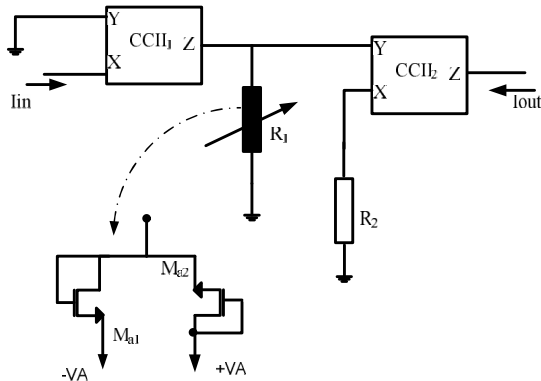

Fig. 17. Application of the proposed CCII as a high-performance variable-gain wide bandwidth current amplifier.

Figure 18 shows the frequency performance of the current amplifier of Fig. 17. Interestingly, for $R_2 = 100\ \Omega$ and different values of V_A, −3 dB bandwidth of the proposed current amplifier varies between 81.1 MHz to 90 MHz for different current gains ranging from 10.6 dB to 19 dB, respectively. The input and output impedances are also 0.155 Ω and 1.6 MΩ respectively.
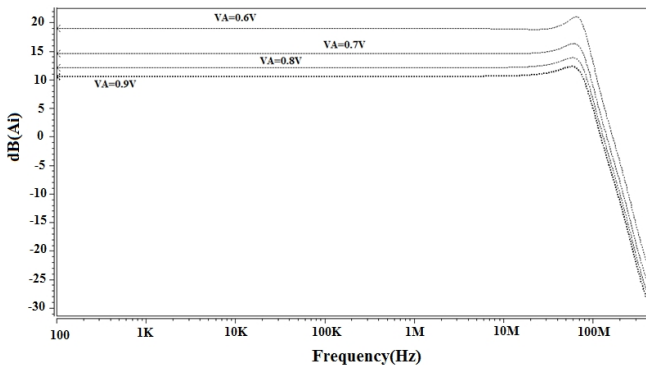

Fig. 18. Gain frequency performance of the current amplifier of Fig. 17.

Using the proposed CCII in current amplifier application results in two major improvements:

1. Low input impedance equal to the X terminal impedance of the proposed CCII and high output impedance equal to Z terminal impedance of the proposed CCII.

2. Very wide bandwidth as a result of the proposed CCII's high frequency performance.

IV. CONCLUSIONS

A new super transistor-based CCII for low-voltage high frequency applications, has been designed. The proposed

CCII can operate at low supply voltage and exhibits very low impedance at its X terminal. It also exhibits wide frequency performance for both voltage and current transferring. As other merit, the proposed topology exhibits an extremely low offset voltage at X node, therefore, the need for any offset voltage cancellation circuit is alleviated resulting in a very simple structure. The performance of the proposed CCII in applications such as instrumentation amplifier, variable-gain voltage amplifier and variable-gain current amplifier has been tested. The achieved results prove that the proposed CCII is highly suitable for wideband low-voltage low-power applications.

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APPENDIX A

For V_{GSM1} and V_{GSMA1} we have:

$$V_{GSM1} = \sqrt{\frac{I_{B2}}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1}(1+\lambda V_{DSM1})}} + V_{thM1} \approx$$

$$\approx K_1\left(1 - \frac{\lambda V_{DSM1}}{2}\right) + V_{thM1}, \qquad (A.1)$$

$$\approx K_2\left(1 - \frac{\lambda V_{DSMA1}}{2}\right) + V_{thMA1}. \qquad (A.2)$$

In which:

$$K_1 = \sqrt{\frac{I_{B2}}{\frac{1}{2}\mu nCox\left(\frac{W}{L}\right)_{M1}}}, \qquad (A.3)$$

$$K_2 = \sqrt{\frac{I_{B3}}{\frac{1}{2}\mu nCox\left(\frac{W}{L}\right)_{MA1}}}. \qquad (A.4)$$

For $K_1 = K_2 = K$ and $V_{thM1} = V_{thMA1}$ (assuming identical transistors), by inserting (A.1) and (A.2) into (7), offset voltage is found as

$$V_{off} \approx \frac{K\lambda}{2}\left(V_{DSMA1} - V_{DSM1}\right). \qquad (A.5)$$

APPENDIX B

$$\frac{V_X}{V_Y} = \frac{g_{m1}r_{oIB2}}{1+g_{m1}r_{oIB2}} \times$$

$$\times \frac{1}{1 + [g_{mA1}(r_{oA1}\|r_{oIB3})g_{mA2}(r_{oA2}\|r_{oIB4})]^{-1}} \approx$$

$$\approx \frac{g_{m1}r_{oIB2}}{1+g_{m1}r_{oIB2}} \approx 1, \qquad (B.1)$$

where g_{mi} and r_{oIBi} are transconductance and output resistance of related transistor and current source, respectively.