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On Delay Test Generation for Non-scan Sequential Circuits at Functional Level

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Introduction

Sequential circuit testing has been recognized as the most difficult problem in the area of fault detection. The difficulty comes from the existence of memory elements. With memory elements, such as latches or flip-flops, the circuit output depends not only on the current inputs but also on the operation history (circuit states). Of course, it is possible to facilitate sequential circuit testing by adding some extra hardware, which enhances the controllability and observability of the circuit. However, the test hardware increases hardware overhead and can degrade circuit performance. Thus, before using valuable chip space, test generation without adding extra hardware should be tried.

High-performance circuits with aggressive timing constraints are usually very susceptible to delay faults. As the drive towards lower power processors continues, the number of "critical" paths increase, i.e. the delay of such paths is close to the rated speed of the circuit. Small process variations and environmental changes (like temperature increase) may cause such circuits to fail at the rated clock speed. Testing high-performance circuits for timing failures is becoming very important.

Most of the proposed delay fault test techniques for sequential circuits involve test methods utilizing scan chains or variable clock speed test application. Inserting scan latches into designs is expensive in terms of chip real estate. On the other hand, testing non-scan circuits using variable clock speeds requires sophisticated testers and clock control circuitry. Due to these drawbacks, delay fault testing in industry has focussed on at-speed test application in non-scan or partial scan circuits [1].

In this paper we are going to investigate the situation when tests are generated for functional delay faults and then applied for detection of transition faults. We consider the at-speed testing of non-scan synchronous sequential circuits.

The rest of the paper is organized as follows. Section 2 presents the related work. In Section 3, we describe the new framework of test generation for non-scan sequential circuits, and Section 4 concludes the paper.

Related work

The at-speed test application has the advantage that the circuit is tested under its normal operation conditions. It has been shown that certain defects will only be detected if tests are applied at-speed [2]. Additionally, as demonstrated in [3], test application that deviates from normal operation can cause faulty behaviour that would not show up during normal operation. In general, the fault coverage for at-speed testing is lower than that for variable clock testing. Nevertheless, its simplicity of implementation makes at-speed testing the methodology of choice for most industrial ICs [1].

Some interesting papers [4–12], in which various problems of testing of non-scan synchronous sequential circuits are researched, were published in last few years.

In paper [4], a new transition fault model for synchronous sequential circuits is proposed. This model addresses the fact that delayed signal transitions span multiple clock cycles when a test sequence is applied to a synchronous sequential circuit at-speed. An advantage of this model is that it helps detect other types faults that require two-pattern tests, such as transistor stuck-open faults.

Another transition fault model for use with at-speed test sequences is defined in [5]. The model is referred to as the unspecified transition fault model since it introduces unspecified values into the faulty circuit when fault effects may occur. Fault detection potentially occurs when an unspecified value reaches a primary output. Due to the uncertainty that the unspecified value will be different from the fault-free value, an added requirement of this

model may be that a fault would be detected multiple times.

The delay fault test for non-scan synchronous sequential circuits could be constructed at the functional level using the software prototype model, as well [6, 7]. Kang et al. [6] suggested the input/output transition (TRIO) fault model for functional test selection at the register-transfer level (RTL). It is defined with respect to the primary inputs, primary outputs, and state variable of the module. However, this model is approximate because it does not stipulate toggle propagation all the way to the primary outputs.

The paper [7] presents an approach of test generation for non-scan synchronous sequential circuits based on functional delay models. The non-scan sequential circuit is represented as the iterative logic array model consisting of k copies of the combinational logic of the circuit. The value k defines a length of clock sequence. The experimental results demonstrate the superiority of the delay test patterns constructed at the functional level using the functional fault models against the transition test patterns generated at the gate level by deterministic test pattern generator. Especially, the functional delay test generation method is useful for the circuits, when the long test sequences are needed in order to detect transition faults.

Random test sequences may be used for manufacturing testing as well as for simulation-based design verification [8, 9]. It was shown in [8] that random primary input sequences achieve low fault coverage for synchronous sequential circuits due to the fact that they repeatedly assign the same values to subsets of state variables. To address this issue, in [8] a procedure is described for modifying a random primary input sequence to eliminate the appearance of input vectors that synchronize subsets of state variables. It is demonstrated that this procedure has a significant effect on the fault coverage that can be achieved by random primary input sequences.

However, the presented in [9] research shows that relatively long random test sequences exhibit better transition fault coverages than tests produced by deterministic ATPG tools. The paper [9] presents an approach for dividing of long test sequences into subsequences. The application of this approach allows increasing the fault coverage of the initial random generated test sequence and minimizing the length of the test by eliminating subsequences that don't detect new faults.

Under the approach presented in [10], the input vectors comprising the test sequence are fixed in advance. The process of generating the test sequence consists of ordering a set of precomputed input vectors such that the resulting test sequence has as high a fault coverage as possible. The test generation process thus searches a limited set of input vectors for an appropriate order instead of exploring a search space that is limited only by the number of primary inputs of the circuit. However, only stuck-at faults are considered in both papers [8, 10].

For synchronous sequential circuits, one important issue is their initialization, which means the sequential circuit must start from a known initial state for it to operate correctly, as well as when generating tests for circuit, or when verifying the functional properties. The paper [11] addresses to this problem. A method for finding shortest length reset sequences using circuit emulating software prototypes is proposed. The novelty and research value of the method comes from using software that emulates circuits instead of using manufactured chips. Such method does not use logical structure of the chip itself and test generation may start earlier in the manufacturing process.

Framework of test generation for non-scan sequential circuits

We performed a variety of experiments on non-scan version of ITC'99 sequential synchronous benchmark circuits. Based on gained experience and experimental results, we are going to propose a new framework of test generation for non-scan sequential circuits. We consider functional level delay faults. The models of the benchmark circuits are written in C programming language. The random search is used for test pattern generation.

We present synchronous sequential circuit as iterative logic array. Let a one generic cell of the iterative logic array model have a set of primary inputs $X = \{x_1, ..., x_i, ..., x_n\}$, a set of primary outputs $Y = \{y_1, ..., y_j, ..., y_m\}$, a set of bits of previous state $Q = \{q_1, ..., q_l, ..., q_v\}$, and a set of bits of next state $P = \{p_1, ..., p_k, ..., p_v\}$. We define a functional delay fault of synchronous sequential circuit as follows:

Definition 1. A functional delay fault is a tuple (I, O, tI, tO), where I is a primary input x_i (i=1, …, n) or a bit of previous state q_l (l=1, …, v) of the generic cell, O is a primary output y_j (i=1, …, m) or a bit of next state p_k (l=1, …, v), tI is a rising or falling transition at I, and tO is a rising or falling transition at O.

Thus, four functional delay faults are associated with every I/O pair, and the total number of faults is 4*(n+v)*(m+v).

In this paper, we use the term "subsequence", which is defined in [9] as follows:

Definition 2. The subsequence is a sequence of input patterns which starts with a set of initialisation patterns.

The subsequence is composed of two parts of input patterns: the first part Sub(In) is a set of initialisation patterns that lead the circuit to the known state and the second part Sub(test) is a set of test patterns [9]. The number of input patterns in Sub(test) defines the length of the subsequence. In case of presentation of sequential circuit as iterative logic array, the length of the subsequence corresponds to the number of generic cells in the iterative logic array. All ITC'99 benchmark possess *Reset* lines, therefore, there are no initialisation problems, and in all cases the initialisation part Sub(In) of subsequences is comprised of one pattern only.

The length of the test subsequence is very important factor. If the length is too small, some circuit states will not be visited, and the corresponding faults will not be detected. On the other hand, if the length of the subsequences is too big, some states will be visited repeatedly but that will not sensitize a new path and no new faults will be detected [9]. Next, we are going to

propose an approach for determining the length of the test subsequence.

The idea is very simple: we randomly generate small number of test subsequences of particular length and count the number of detected functional delay faults; by gradually increasing the length of subsequence we repeat this operation until the number of detected functional delay faults stabilises; the length of subsequence at stabilisation point is than taken for further generation of test.

For example, let us consider the circuit b13. The dependence between subsequence length and number of detected functional delay faults is presented in Table 1.

Table 1. Example b13

Length	100	500	1500	2000	2500	3000	3500	4000
Detected FD	187	250	296	312	339	330	342	344

The subsequence lengths are provided in the row under heading "Length", and the numbers of detected functional delay faults are shown in the row under heading "Detected FD". There were generated 10 random subsequences for each case. From Table 1 we can see that the number of detected functional delay faults stabilises beginning at subsequence length 2500. Therefore, for circuit b13 the subsequence length of 2500 was chosen for test generation.

Results of application of proposed approach to several ITC'99 sequential benchmark circuits are shown in Table 2. For each circuit, circuit name (Circuit), found subsequence length and for comparison subsequence length presented in [9] (App. [9]) are provided. The obtained subsequence lengths correlate with those from [9] where much more sophisticated procedure of subsequence length finding was presented and gate-level descriptions of the circuits were used.

Table 2. Obtained subsequence lengths for ITC'99 benchmark circuits

Circuit	b04	b06	b07	b08	b09	b10	b11	b12	b13	b14
Length	10	8	200	40	40	30	2700	1000	2500	800
Appr. [9]	-	-	194	38	41	21	2492	958	2986	812

As it is well known, random search requires some termination condition to be defined. The simplest termination condition is the number of randomly generated test subsequences, but this condition says nothing about the quality of found solution. The ratio of detected faults may be another one condition. However, the number of detectable functional delay faults is not known. It is worth to relate the condition of the termination of random search dynamically to the number of the last selected subsequence. The generation can be terminated when the total number of generated random subsequences exceeds the number of the last selected subsequence multiplied by a coefficient K.

We performed two independent test generations using coefficient K=2 and one test generation using K=5. The results of this experiment are summarised in Table 3. The columns under heading "Det. FD" indicate the numbers of detected functional delay faults and the columns under heading "F. c." display transition fault coverages expressed in per cent. Recall, the functional delay faults are functional level faults whereas the transition faults are gate-level faults.

First sighting is that there is not strong dependence between functional and gate-level fault coverages, i.e. higher numbers of detected functional delay faults don't indicate higher transition fault coverages. For example, look at the results for circuits b10, b13 and the row "Average". Next and most important sighting is that long (using high values of coefficient K) random generation not necessarily leads to higher gate-level fault coverages, compare the on average transition fault coverages of tests T1 and T3.

Table 3. Random test generation results

Circuit	Generation 1, K=2 (Test T1)		Generation 2, K=2 (Test T2)		Generation 3, K=5 (Test T3)	
	Det. FD	F. c.	Det. FD	F. c.	Det. FD	F. c.
b04	1797	84.17%	1797	84.17%	1797	83.79%
b06	89	89.62%	89	89.94%	89	89.62%
b07	297	48.33%	297	48.15%	300	48.69%
b08	205	79.66%	205	75.85%	205	77.86%
b09	526	72.23%	526	73.01%	526	73.67%
b10	291	78.86%	292	78.40%	292	78.22%
b11	899	78.10%	899	78.06%	899	78.06%
b12	620	35.41%	617	35.15%	620	35.41%
b13	346	63.06%	348	62.62%	348	62.24%
b14	17558	77.45%	17275	77.45%	17643	77.64%
Average	2262.8	70.69%	2234.5	70.28%	2271.9	70.52%

One of the approaches for deriving tests to achieve high defect coverage is based on the generation of n–detection tests [12, 13]. An n-detection test is one where each fault is detected either by n different tests, or by the maximum number of different tests that can detect the fault if this number is smaller than n. Thus, we tried to improve the quality of test by merging tests T1 and T2 and so achieving 2-detection of functional delay faults. The results of this experiment are presented in Table 4.

Table 4. Comparison of test generation approaches

Circuit	T1+T2	TetraMax	Best of approaches [4] and [7]
b04	84.39%	83.01%	79.03%
b06	90.57%	84.59%	-
b07	48.78%	0.00%	-
b08	80.51%	69.70%	-
b09	73.89%	71.13%	65.93%
b10	79.14%	78.31%	76.55%
b11	78.17%	51.42%	79.13%
b12	35.90%	6.60%	34.33%
b13	63.33%	19.66%	63.43%
b14	78.22%	40.70%	76.76%
Average	71.29%	50.51%	-
Average selected	70.43%	50.12%	67.88%

For each circuit, circuit name (Circuit), transition fault coverage of the 2-detection test T1+T2 (T1+T2), transition fault coverage of test generated by deterministic commercial ATPG TetraMAX (TetraMAX) and the best transition fault coverage of two approaches presented in [4] and [7] (Best of approaches [4] and [7]) are provided. In row under heading "Average selected" only data of the circuits b04, b09 – b14 are used for calculations.

The application of 2-detection tests allowed us to achieve best transition fault coverages in all cases if we compare them with 1-detection tests T1, T2 and T3. The quality of obtained tests highlights the comparison with other approaches. Our test produces much better fault coverage on average than TetraMAX and methods proposed in [4] and [7].

Now based on gained experience and experimental results, we propose a framework of test generation for non-scan sequential circuits:

1. Find the subsequence length. Use for this purpose small number of randomly generated test subsequences and gradually increase the length of subsequence until the number of detected functional delay faults stabilises. Take length of subsequence at stabilisation point for further generation of the test;

2. Perform two independent random test generations for functional delay faults. Terminate each generation when the total number of generated random subsequences exceeds the number of the last selected subsequence multiplied by a number 2;

3. Merge the two obtained test into one test.

Conclusions

We investigated the application of tests that are generated at functional level for detection of gate-level transition faults. Based on experimental results, we developed a framework of test generation for non-scan sequential circuits. The provided comparison with experimental results of other approaches demonstrates the effectiveness of proposed framework.

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E. Bareiša, V. Jusas, K. Motiejūnas, R. Šeinauskas. Nuoseklių schemų vėlinimo testų generavimas funkciniame lygmenyje // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2011. – Nr. 3(109). – P. 67–70.

Nuoseklių schemų testavimas yra didžiausia gedimų aptikimo schemose problema. Šiame straipsnyje nagrinėjamas testų, sudarytų funkciniame lygmenyje, pritaikymas struktūrinio lygmens perėjimo gedimams aptikti. Remiantis eksperimentiniais rezultatais, buvo pasiūlytas metodas nuoseklių schemų vėlinimo testams generuoti. Straipsnyje pateikti palyginimai su kitais žinomais metodais rodo pasiūlyto metodo efektyvumą. Bibl. 13, lent. 4 (anglų kalba; santraukos anglų ir lietuvių k.).