A Novel Design of Low-Voltage VDIBA and Filter Application

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***Abstract*—In this study, a low-voltage low-power design of previously introduced analog signal processing element called as Voltage Differencing Inverting Buffered Amplifier (VDIBA) is presented. Level shifter current mirrors are used in the circuit design in order to accomplish the low-voltage low-power operation. The configuration operates only with ±0.4 V supply voltages and consumes power 569 µW at the bias current 50 µA. Also, low-voltage transconductor which has highly linear g_m is executed with the use of bulk-driven quasi-floating gate (BD-QFG) and source degeneration techniques. The simulations of the introduced circuit have been performed with 0.18 µm TSMC CMOS technology by SPICE. The theoretical approaches have been confirmed by the simulation results.**

***Index Terms*—MOS integrated circuits; analog integrated circuits; operational amplifiers; VDIBA.**

I. INTRODUCTION

In recent times, the use of the battery-operated equipments such as tablets, mobile phones, smart watches and portable medical equipment has pervaded in the world. Furthermore, IC technology has inclined to make smaller device size. Thus, channel lengths of the MOS transistors have been attained to the level of nanometers. The novel MOS technologies with channel lengths about level of nanometers are capable of operating with low voltages. Therefore, low voltage-low power (LVLP) circuit design comes into prominence in the analog circuit technology [1], [2].

Numerous novel active elements which are using differential input signals have been employed in design of diverse analog signal processing applications. These active elements can be classified in two groups such as operating with differential input current and differential input voltages. Current Differencing Buffered Amplifier (CDBA) and Current Differencing Transconductance Amplifier (CDTA) use the differential input currents, whereas Voltage Differencing Transconductance Amplifier (VDTA), Voltage Differencing Current Conveyor (VDCC) and Voltage Differencing Buffered Amplifier (VDBA) employ differential input voltages [3]–[12]. An active element VDIBA increasing the popularity has presented in the previous study [13]. This topology has simple structure and electronic adjustability in wide range. VDIBA consists of two blocks such as Operational Transconductance Amplifier (OTA) and unity gain Inverting Buffered Amplifier (IBA). Therefore, this structure has a current output terminal as well as a voltage output terminal. Although various VDBA / VDIBA structures have been proposed in [14]–[17], none of these are not suitable for low voltage low power circuit applications.

In this study, a new low-voltage VDIBA structure has been proposed. This circuit operates with lower supply voltages using level shifter PMOS current mirrors as an active load. Also, bulk-driven quasi-floating gate (BD-QFG) technique is used to improve the linearity [18]. Additionally, as an application of the proposed VDIBA, a current controlled universal filter has been designed. Finally, the suggested VDIBA and the filter application have been simulated by SPICE. Simulation results have supported the outcomes of the theory. The proposed structure can operate with ±0.4 V and uses up low power. Moreover, the proposed structure not only has a desirable frequency response, but also exhibits good linearity.

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II. PROPOSED VDIBA STRUCTURE

The schematic symbol and the equivalent model of the VDIBA are indicated Fig. 1. The VDIBA involves two voltage inputs, a voltage and a current output.

The VDIBA can be defined below [13]:

$$\begin{bmatrix} I_{v+} \\ I_{v-} \\ I_Z \\ V_{W-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & -\beta & 0 \end{bmatrix} \begin{bmatrix} V_{v+} \\ V_{v-} \\ V_Z \\ I_{W-} \end{bmatrix}, \quad (1)$$

where $-\beta$ and g_m are the voltage transfer gain and the transconductance value of the VDIBA, respectively. For the ideal VDIBA, β is equal to one.

The proposed VDIBA is exhibited in Fig. 2. In order to carry out operating with low supply voltage, a level shifter

PMOS current mirror has been composed with employing M1, M2 and M3 transistors [19], [20]. Additionally, C3 capacitor is employed to extend bandwidth of the PMOS current mirror. M4 transistor is used to provide bias current for the current mirror. This current should be quite low. In order to obtain quite low bias current, M4 transistor is used as reverse diode connection. Also, a basic current mirror has been constituted by M11, M12 and M13 transistors. The principle of the BD-QFG with the help of NMOS transistors is used in the proposed circuit [18]. These transistors are M5 and M6. M7 and M8 transistors are employed to carry out high value resistance at the BD-QFG transistors. C1 and C2 are input capacitances between quasi-floating-gates and input terminals of the QFG-MOS transistors. To improve the linearity for the transconductance behavior of the VDIBA, M9 and M10 transistors are used for source degeneration via MOS transistors [21]–[23]. The inverting buffered block of the VDIBA is composed of M14 and M15 transistors.

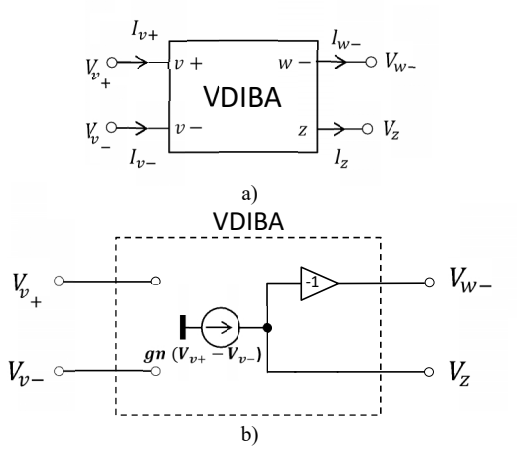

Fig. 1. Circuit symbol of the VDIBA (a), and the equivalent model of the VDIBA (b).

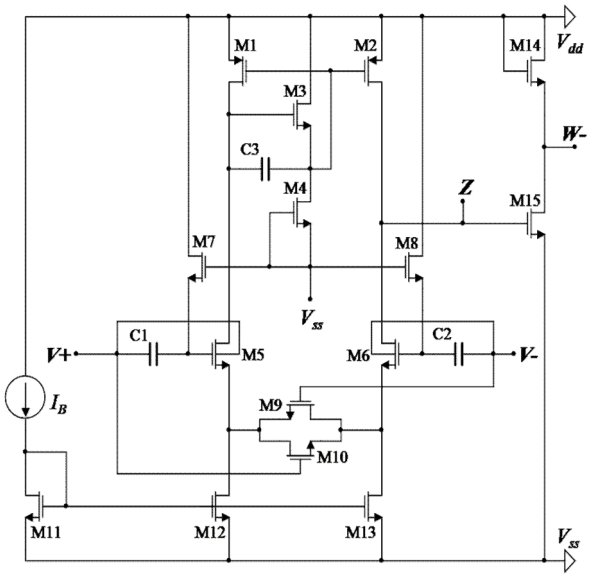

Fig. 2. The suggested LVLP VDIBA.

The transconductance (g_m) of the NMOS transistor can be written as [24]

$$g_m = k_n\left(V_{GS} - V_{TH}\right), \tag{2}$$

where k_n is the NMOS transistor's transconductance parameter. Also, the transconductance of the N type BD-QFG transistor can be given as [18]

$$g_{mBD-QFG} = k_n\left[\left(C_{in}/C_T\right)+\left(C_{BC}/C_{GC}\right)\right]\left(V_{GS} - V_{TH}\right), \tag{3}$$

where C_{BC} and C_{GC} are total bulk channel capacitance and total gate channel capacitance, respectively. Also, C_{in} and C_T are input capacitance between quasi-floating-gate and input-terminal of the QFG-MOS transistor, total input capacitance, respectively [18]. Here, the transconductance parameter of the BD-QFG transistor can be obtained as

$$k_{nBD-QFG} = k_n\left[\left(C_{in}/C_T\right)+\left(C_{BC}/C_{GC}\right)\right]. \tag{4}$$

In Fig. 2, if it is assumed that M5, M7 and M9 are identical to M6, M8 and M10, respectively, in order to simplify the formulation, the following parameter can be assigned as

$$b = \left(4k_{n9} + k_{nBD-QFG}\right)\Big/\left(4k_{n9}k_{nBD-QFG}\right), \tag{5}$$

where k_{n9} is the transconductance parameter of M9 and M10. Also, $k_{nBD-QFG}$ is the transconductance parameter of two BD-QFG transistors which are employed as differential pairs. Considering (2)–(5), the output current expression of the VDIBA is obtained as

$$I_Z = \left[\left(I_B V_{in}\right)/\left(bg_m\right)\right]\sqrt{1-\left[V_{in}/\left(2bg_m\right)\right]^2}, \tag{6}$$

where I_B is the biasing current and V_{in} is the differential input voltage between v+ and v- terminals of the VDIBA [18], [21]–[23].

III. Simulation Results

The simulation results of the introduced VDIBA structure have been obtained by SPICE using the 0.18 μm CMOS technology parameters. The simulations have been performed with ±0.4 V supply voltage. The channel dimensions of the transistors employed in proposed VDIBA are shown in Table I. C1, C2 and C3 capacitors depicted in Fig. 2 have been selected as equal to 5 pF, 5 pF and 1 pF, respectively.

TABLE I. CHANNEL DIMENSIONS OF TRANSISTORS.

Transistor	L (μm)	W (μm)
M1, M2	0.2	15
M3	2	100
M4	2	30
M5, M6	5	14
M7, M8	3	6
M9, M10	5	4
M11-M13	1	18
M14, M15	0.5	60

Figure 3 shows the plot of I_Z versus V_{in} for the proposed VDIBA. It is shown in Fig. 3 that the linear operation range of g_m value for the introduced structure can be obtained as about ±0.3 V. Here, V_{in} is differential input voltage (Vv_+–Vv-). Moreover, the transconductance can be adjusted by the I_B.

DC voltage characteristic of *Vw*- and *Vz* against V_{in} for the proposed VDIBA are shown in Fig. 4. This graph has been obtained for 1 KΩ load resistance at port Z.

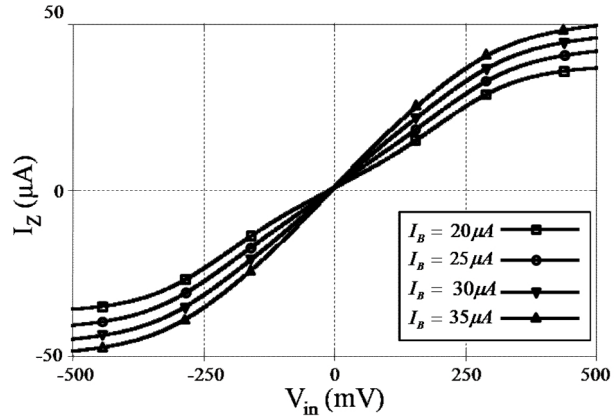

Fig. 3. The transfer curve of the VDIBA.

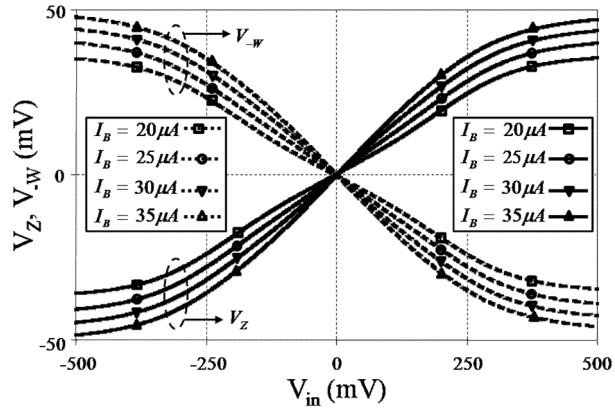

Fig. 4. DC voltage characteristic of V_{w-} and V_z against V_{in} for different biasing currents.

The maximum value of the input terminal voltages without causing remarkable distortion are approximately obtained as ±300 mV. Also, the input offset voltage is obtained as 646 μV.

Figure 5 depicts the g_m value versus I_B current. It is seen in Fig. 5 that, the g_m of the structure can be adjusted between 57 μS and 223 μS during the I_B is altered from 15 μA to 50 μA.

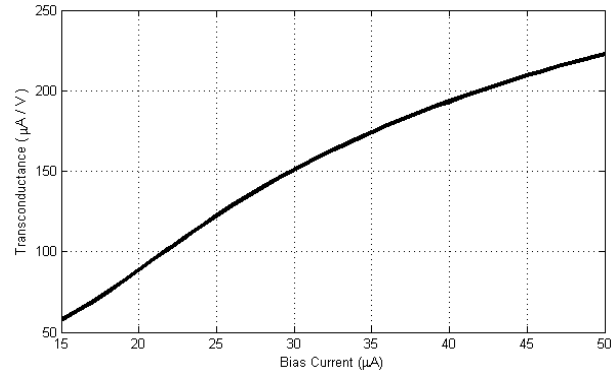

Fig. 5. Transconductance value relates to I_B.

Figure 6 depicts the frequency performance of the proposed VDIBA. From Fig. 6(a) and Fig. 6(b), it is seen that the -3 dB cut-off frequencies of the OTA and IBA stages are about 1.124 GHz and 23.58 GHz, respectively. According to these graphs, the cut-off frequency of the proposed VDIBA can be obtained as 1.124 GHz. Considering in the literature, this value is preferable.

Figure 7 depicts the frequency behavior of the introduced structure for several temperature values. The g_m value varies from -72.45 dBS to -74.52 dBS, while the temperature is altered from 0 °C to 75 °C. This performance can be considered as acceptable.

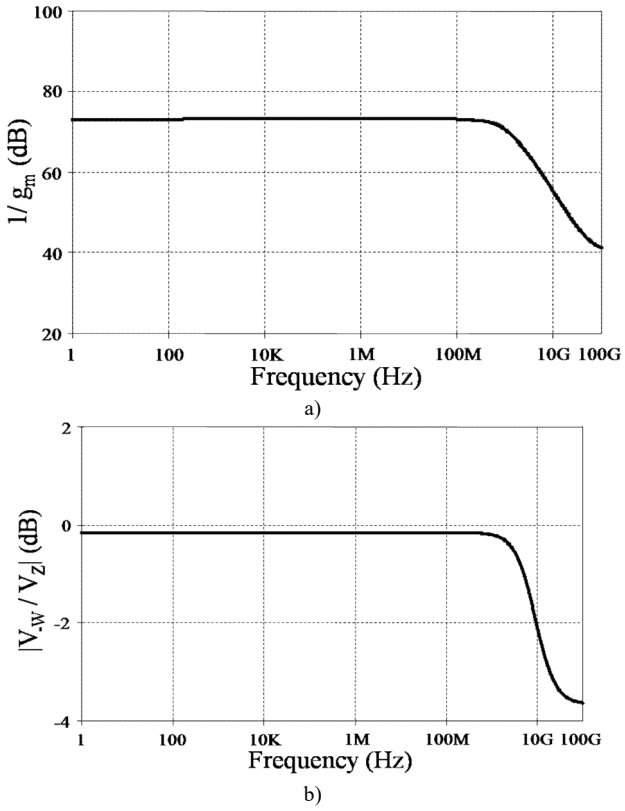

Fig. 6. Frequency response of the VDIBA's OTA stage (a), and frequency response of the VDIBA's IBA stage (b).

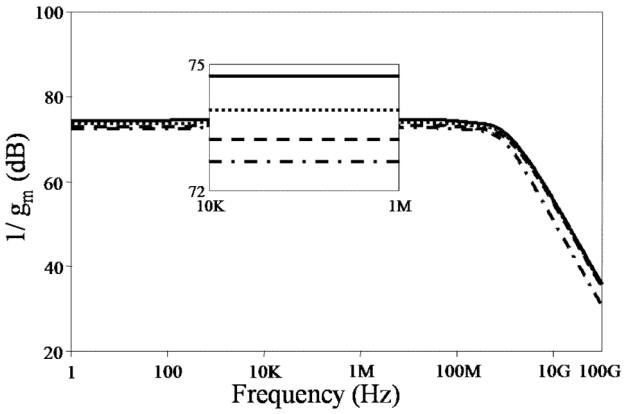

Fig. 7. Frequency response of the VDIBA for several temperature values.

In Table II, the introduced VDIBA has been compared to the other VDIBA circuits in previous works. The proposed structure operates only at ±0.4 V as supply voltages with total power dissipation of 569 μW. It is seen that the proposed VDIBA operates with the lowest supply voltages, and uses up less power than the others. Hence, this circuit is quite suitable for the low power applications. Moreover, the proposed structure's bandwidth is wider than the others. Considering the gain of IBA stages, the proposed VDIBA shows a good performance. For VDIBA structures, impedance value of the port Z is desired as high as possible.

TABLE II. PERFORMANCE PAMARAMETERS OF VDIBAS.

	This study	**[13]**	**[16]**
CMOS technology	0.18 µm	0.18 µm	0.18 µm
Numbers of transistors	13 MOS + 2 FGMOS	6 MOS	5 MOS + 1 FGMOS
Supply voltage	±0.4 V	±0.9 V	±0.75 V
Power dissipation	569 µW	10.5 mW	1.5 mW
Linear input range of OTA stage	±300 mV	±200 mV	±250 mV
Input voltage / Supply voltage for OTA stage (%)	75 %	22 %	33 %
Linear input range of IBA stage	-400 mV to +160 mV	-900 mV to +500 mV	Not reported
Input voltage / Supply voltage for IBA stage (%)	70 %	77 %	Not reported
Bandwidth	1.124 GHz	226 MHz	220 MHz
Gain of IBA	-0.981	-0.922	-0.985
Transconductance (g_m)	223 µS ($@I_B = 50\mu A$)	600 µS ($@I_B = 100\mu A$)	582 µS ($@I_B = 100\mu A$)
Input terminal impedance (R_{in})	51.57 MΩ ($@I_B = 50\mu A$)	Not reported	Not reported
Output impedance for port Z (R_Z)	22.3 KΩ ($@I_B = 50\mu A$)	131.93 KΩ ($@I_B = 100\mu A$)	132.4 KΩ ($@I_B = 100\mu A$)
Output impedance for port -W (R_{-W})	111 Ω ($@I_B = 50\mu A$)	42.36 Ω ($@I_B = 100\mu A$)	Not reported
Input offset voltage	646 µV	Not reported	Not reported

Therefore, other VDIBA structures exhibit better performance. Resistance value of the port W- is a low impedance output. In terms of port W- impedance, the proposed structure is satisfactory but not as much as structure given in [13]. The input impedance of the proposed structure is obtained acceptably high such as 51.57 MΩ.

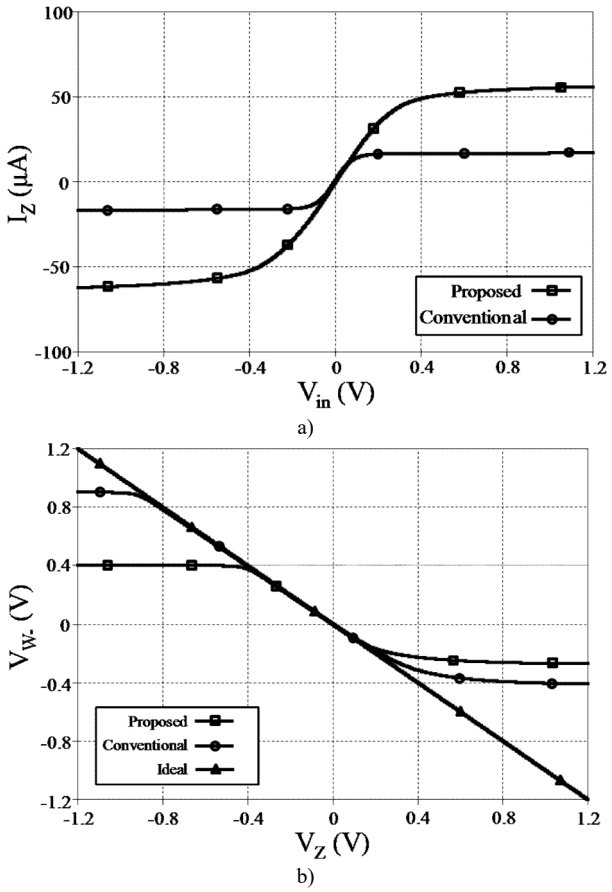

Fig. 8. I_Z-Vin characteristic of VDIBAs (a), and V_{W-} -V_Z characteristic of VDIBAs (b).

For the proposed and conventional [13] VDIBA, the dynamic input range of OTA and IBA stages are shown in Fig. 8(a) and Fig. 8(b). Considering the OTA stages, dynamic input ranges of the proposed VDIBA and the conventional VDIBA [13] are ±0.3 V and ±0.2 V as clearly shown in Fig. 8(a) for ±0.4 V and ±0.9 V supply voltages, respectively. This graph is obtained for equal g_m values. In terms of IBA stages, ratios of the dynamic input range to supply voltage are 70 % and 77 % for proposed and conventional VDIBA, respectively. The proposed structure exhibits good performance. Linear input range of IBA stage is quite acceptable for low voltage low power applications.

IV. VDIBA BASED CURRENT CONTROLLED UNIVERSAL FILTER

The designed VDIBA based current controlled universal filter structure is displayed in Fig. 9. The multiple-input single-output filter structure has three inputs to exhibit the high pass (HP), band pass (BP) and low pass (LP) filter characteristics. The filter can operate with low supply voltages such as ±0.4 V. For that reason, the proposed filter structure is convenient for low voltage applications.

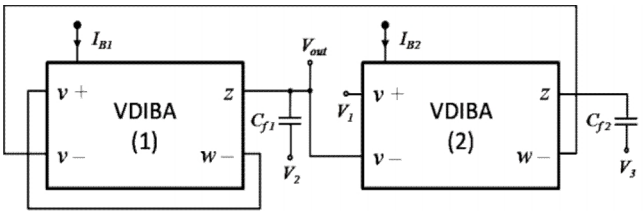

Fig. 9. VDIBA based current controlled universal filter.

The filter structure employs two VDIBAs and two capacitors. The output functions of the filter can be obtained as

$$V_{out} = \left[s^2 V_2 + s\left(g_{m1}/C_{f1}\right)V_3 + \left(\left(g_{m1}g_{m2}\right)/\left(C_{f1}C_{f2}\right)\right)V_1\right] / \left[s^2 + s\left(g_{m1}/C_{f1}\right) + \left(\left(g_{m1}g_{m2}\right)/\left(C_{f1}C_{f2}\right)\right)\right], \quad (7)$$

where g_{m1} and g_{m2} are the transconductances of the VDIBAs. Assuming that all biasing currents are equal, the transconductance of the VDIBAs can be written as $g_{m1} = g_{m2} = g_m$. In this case, the quality factor and cut-off frequency of the structure can be attained as

$$Q = \sqrt{C_{f1}/C_{f2}}, \quad (8)$$

$$w_0 = g_m/\sqrt{C_{f1}C_{f2}}. \quad (9)$$

From (8) and (9), it is realized that the cut-off frequency can be tuned by the biasing current I_B independently of quality factor.

In Table III, input voltage combinations are given for the different filter characteristics.

TABLE III. INPUT VOLTAGE COMBINATIONS FOR THE DIFFERENT FILTER CHARACTERISTICS.

Filter Type	V1	V2	V3
LP	Vin	0	0
HP	0	Vin	0
BP	0	0	Vin

Figure 10 indicates the frequency responses of the designed filter for the LP, HP and BP configurations. Herein, C_{f1} and C_{f2} are taken as 5 pF. Also, g_m values of VDIBA are chosen as 65 µS.

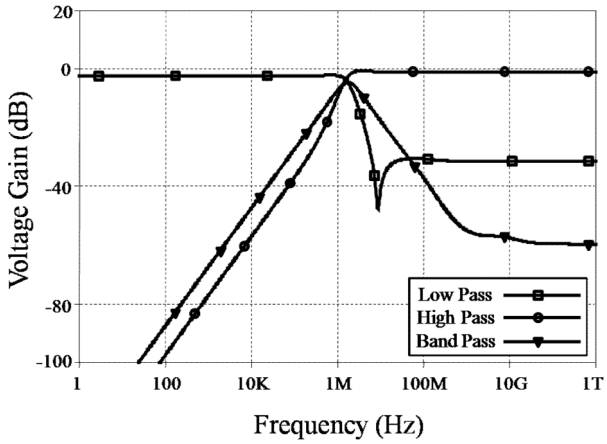

Fig. 10. Frequency responses of the filter for the LP, HP and BP configurations.

The frequency behavior of the HP filter for the several biasing currents is depicted in Fig. 11. Herein, C_{f1} and C_{f2} are taken as 5 pF. It can be observed in Fig. 11 that the filter can be electronically adjusted for different I_B flows.

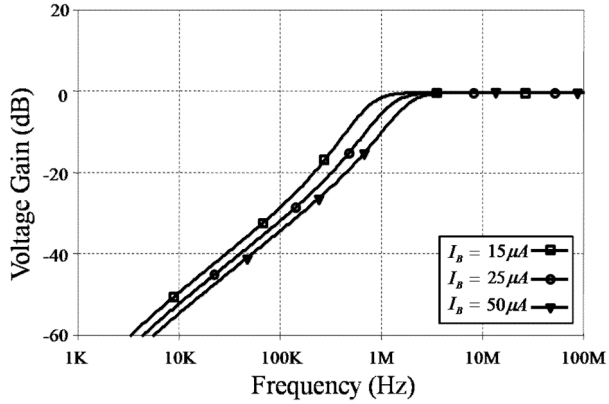

Fig. 11. Frequency responses of the HP filter configurations for different biasing current.

The major advantage of the proposed filter is that the structure can operate with low supply voltage such as ±0.4 V. Also, any resistive elements are not employed in the filter structure. In addition to this, the filter can be controlled electronically by the biasing currents. Therefore, the proposed circuit is convenient for low voltage low power applications, IC technologies and current controlled structures.

V. CONCLUSIONS

In this study, a novel low voltage low power VDIBA based on bulk-driven quasi floating-gate technique and level shifter current mirror has been suggested. Additionally, to prove the functionality of the proposed VDIBA, a universal filter has been designed with using proposed circuit. The simulations of the proposed structure and the filter have been carried out using 0.18 µm TSMC CMOS technology parameters by SPICE. The simulation results confirm the theoretical approach. In addition, the proposed structure has been compared to the other VDIBA structures, in the literature. Hence, the advantages of the proposed structure have been exhibited. The introduced VDIBA is capable of operating with ±0.4 V supply voltage and only dissipates power as 569 µW. Also, the bandwidth of this structure is about 1.124 GHz. Furthermore, the proposed VDIBA is convenient for the IC technology, because of the fact that the proposed design has not involved any resistive element. Consequently, it is figured out that the suggested VDIBA is fairly appropriate structure for the analog integrated circuits and LVLP applications.

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