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The Efficient Solution of Parasitic Voltage Annulment in Electronic Low Resistance Comparator

R. Radetic
Serbian Transmission System, Nade Dimic, 40, 19210, Bor, Serbia
M. Pavlov, D. R. Milivojevic
Mining and Metallurgy Institute Bor,
Zeleni bulevar bb, 19210 Bor, Serbia, phone: +381 30 435 109, e-mail: dragan.milivojevic@irmbor.co.rs

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Introduction

For low resistance measurement the comparison method is often in use. This principle understands the comparison of the unknown (measured) resistance, R_X with a known, referent one R_R. Standard methods for measurement and low resistance comparison are based on Thompson (Kelvin) bridges [1]. The high quality multimeters can also be used for this kind of measurement [2, 3]. Authors have realized electronic low resistance comparator as a very precise instrument for resistance measuring based on comparison with referent (known) resistor [4].

The measuring unit is realized by integration of a‘few main electronic modules (Fig. 1).

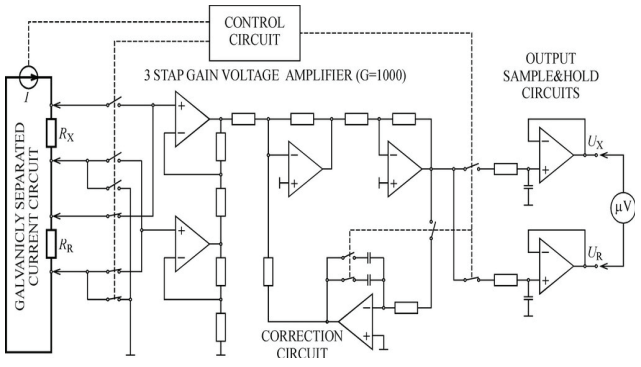

Fig. 1. Overall block diagram of chopper stabilized comparator

During the measuring process, in the voltage on referent resistor (R_R) and measuring one (R_X), the parasitic (unwanted) voltages are added. That makes the measuring result worse.

The problems occur by development and realization of the multirange instrument. The solutions to overcome these problems are described below.

Designing and developing the fixed measuring range unit, there is a possibility to choose the values of all elements (resistors and capacitors) so to eliminate the parasitic voltages, using standard electrical correction circuit (Fig. 1).

Standard correction circuit

The function of correction circuit in Fig. 1 is to operate by elimination of all voltages – non-products of measuring current through referent and measured resistor. The amplifiers offset voltages are dominant disturbances here. Sometimes they could reach 100 μV. By the careful choice of elements values those voltages can be decreased to approximately 50 μV. But it steels the great value for such precise instruments [5]. The intention is to measure the voltage values with resolution of about 0.01 μV.

To explain its function, the correction circuit is shown in more details in Fig. 2.

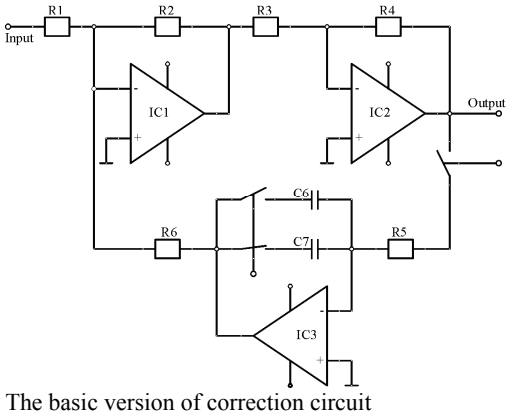

Fig. 2. The basic version of correction circuit

For the circuits in the Fig. 2 the voltage-amplifying rate is defined by values of resistors R_1, R_2, R_3, and R_4 (the

values 1 kΩ, 10 kΩ, 10 kΩ and 91 kΩ are chosen). The capacitors C_6 and C_7 of 0.47 μF and a great resistance R_6=10 MΩ give good time constant to provide small relative influence of capacitance self-discharging. It means that the output voltage will be stabile for longer period of time. The defined elements give the time constant T of 240 ms. The effective time constant takes 2.5 s, because the time of capacitance charging is just one step (1/10 of measuring cycle time) [5]. For the realized instrument, (with one measuring range) the values of the used elements (resistors and capacitors) were chosen so that the time constant is about 2.5 s. By constant voltages, the capacitor is charging through resistor according of exponential low. Within the period of one time constant (T) 63.2% of total capacity is being charged. After two time constants 13.5% remains and so on. After 9 constants T, remains about 0.01% of final value, which is quite enough in our case. The switch is on at only one step of measuring cycle [6]. Therefore it is necessary to pass 9 time constants to decrease the parasitic voltage from 100 μV to 0.01 μV (0.01%). This takes more than 20 s. It is considerable long time. The conditions for a minimal influence of parasitic AC voltage are determined by the experiment. Finally, all of projected performances for a fixed measuring range instrument are proved in practice.

The improved correction circuit

When the low resistance comparator with more measuring ranges was developing and designing, the need for different voltage amplifying occurred, depending of measuring range. However, the described circuit could not be used. To overcome the arising difficulties the next solution is proposed.

Electric circuit shown in Fig. 3 could do the annulment of parasitic voltages, independent on amplifying. In great extent, such solution eliminates the parasitic voltage which is not an effect of a measuring current flow through the referent and measuring resistors [7]. At the same time, it makes the instrument measuring (response) time shorter as well.

The measuring process is completed in ten cycles. Two of them are used for the input parasitic voltage annulment: one for R_R and the other one for R_X [4]. A controller, based on a decade (Jonson) counter, controls all analog switches. It is driven by network supply frequency signal (50 Hz), one step is 20 ms, and the measuring cycle (ten steps) takes 200 ms. It provides rate of 5 measurements in a second.

Along with the DC parasitic voltage component in measuring (input) voltage, there is also an AC component (50 Hz). It could be shown that the annulated voltage depends on the phase difference between controller and supply network and its influence on result is significant. To decrease (annul) that effect, the phase synchronization of the controller clock with network frequency is done.

The circuit IC1 with resistors R_1 and R_2 operates as an output amplifier for measuring voltages with amplifying equal to 1 [6].

The new annulment circuit encircles the offset voltages of that circuit, as of all previous amplifying stages. The chopper stabilized integrated circuit IC2 with very small offset voltage (about 1 μV) is chosen as the first stage of correction circuit (Fig. 3). It runs as an integrator together with the capacitor C_1 and resistor R_3. The circuit IC3 with capacitor C_2 is a voltage follower with very great input resistance. Its input voltage offset is not critical. The whole correction circuit operates as following:

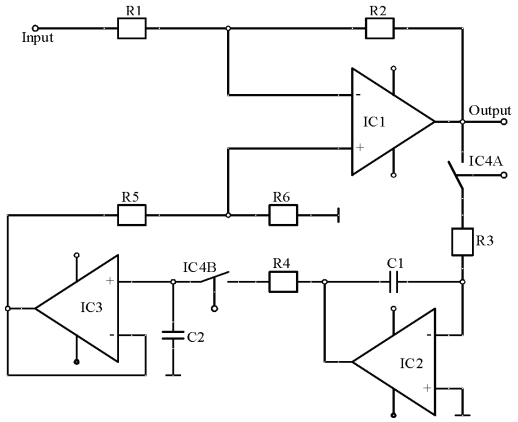

Fig. 3. The improved correction circuit

At the step of annulment the IC1 output voltage comes to input of IC2. Assume that is an initial state and the capacitor C_1 is discharged (U_{INT0} = 0), after first integration the IC2 output voltage is

$$U_{INT1} = -\frac{1}{C_1 R_3}\int_0^T U_{Out0}\,dt = -\frac{U_{Out0}T}{C_1 R_3}, \qquad (1)$$

where T is the integration time (the duration of one controller step, 20 ms).

At the following step the switch IC4A is off and IC4B on, and the capacitor C_2 is charging by U_{Int1} voltage. In order to reach the full capacitor charging, the time constant R_4C_2 has to be much smaller (ten or more times) than switch on time period. At the same step of measuring cycle the same voltage moves to the input of IC1 amplifier and the resultant parasitic voltage in the next step U_{Out1} is:

$$U_{Out1} = U_{Out0} - \frac{U_{Out0}T}{C_1 R_3}\frac{R_2}{R_1}\frac{R_6}{R_5 + R_6}, \qquad (2)$$

$$U_{Out1} = U_{Out0}\left(1 - \frac{T}{C_1 R_3}\frac{R_2}{R_1}\frac{R_6}{R_5 + R_6}\right). \qquad (3)$$

Because of input IC3 voltage decreasing (voltage on $C2$) at the time, to make the influence of that voltage changes as small as possible, the rate R_5/R_6 has to be very small, $R_5/R_6 \ll 1$. Now the expression (3) becomes

$$U_{Out1} \approx U_{Out0}\left(1 - \frac{T}{C_1 R_3}\frac{R_2}{R_1}\frac{R_6}{R_5}\right), \qquad (4)$$

assigning the value in bracket with δ we got

$$U_{Out1} \approx U_{Out0}\,\delta \qquad (5)$$

and after k annulment steps the output voltage can be present as

$$U_{Outk} \approx U_{Out(k-1)}\delta = U_{Out(k-2)}\delta^2 = U_{Out0}\,\delta^k \,. \qquad (6)$$

It could be seen that amplifier output voltage, which represents the zero level value, is progressive decreasing after every measuring step. This voltage has to be zero and it implies the next relation

$$\delta = 1 - \frac{T}{C_1 R_3}\frac{R_2}{R_1}\frac{R_6}{R_5} = 0\,. \qquad (7)$$

Once the conditions above are completely satisfied, after the first step (integration), the total parasitic voltage annulment would be achieved. Still, using the standard elements values, the condition (7) couldn't be satisfied without addition adjustment (tuning). For example, if the choice of elements should (be such to) give δ=0.1, after the first step of measuring cycle (0.2 s) the 90% of parasitic voltage would be eliminated. The 10% remains. After the second step 1% and after 4 steps, the wanted 0.01% will be reminded. It takes only 0.8 s, (Fig. 5). The coarse element choosing, as described, gives incomparable shorter (0.8 s) response time than the circuit in *Fig. 2* (20 s).

To eliminate the influence of AC parasitic network voltage it would be useful to synchronize the controller clock signal with the network frequency. In that case the mean value of voltage (and its harmonics) becomes zero [7].

In the Fig. 2 and Fig. 3 is shown an overall diagram of correction circuit. In the realized instrument it is more complex, because the same amplifiers are used for booth measuring (referent and measuring resistor). The realized instrument, has five measuring ranges: 0,01 Ω, 0,1 Ω, 1 Ω, 10 Ω and 100 Ω. The necessary amplifying for (every one) each is defined and carried out in previous amplifier stages. The particular amplifier with unique amplifying rate equals 1 is integrated in annulment circuit. The realized circuit for parasitic voltage annulations is presented in more detailed schema in Fig. 4.

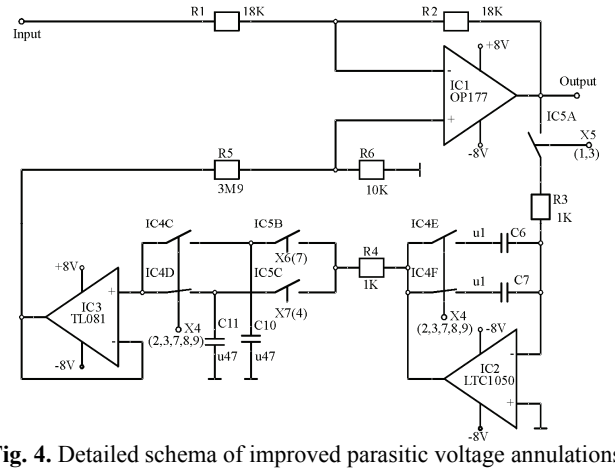

Fig. 4. Detailed schema of improved parasitic voltage annulations circuit

Symbol X assigns the analog switches inputs and the numbers in brackets present the ordinal numeral of measuring cycle steps, when the switch is on (signal is high). By the described analyses [8, 9] has covered not only the annulations circuit, than the complete process of stationary state establishing, including AD converter and output hold circuits, known as the ramp up period (ready for measuring) [8].

Validation of proposed method

The method of simulation was used to illustrate the effects of improved parasitic voltage annulment circuit in Fig. 4. To make the difference of stationary state establishing visible on the screen, for R_3 is set 20% greater value, R_3=1,2 kΩ, instead of 1 kΩ (in realized instrument).

For the discrete elements values shown in Fig. 4 and by the usual real conditions: U_{DC}=10 mV, U_{AC}=3 mV, 50 Hz, ϕ=0^0, the output voltages are shown on diagram in *Fig. 5*.

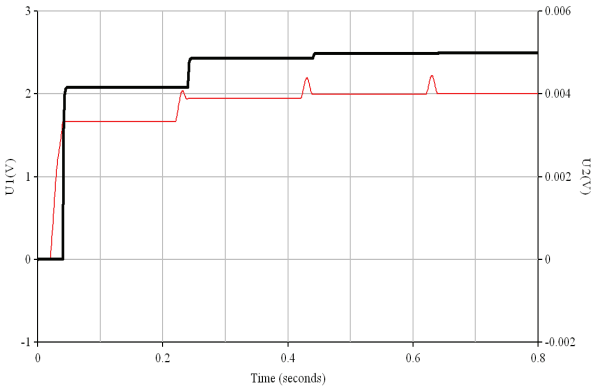

Fig. 5. The stationary state establishing diagram

U_1 – (red thin line) is the IC2 output voltage, U_2 – (black bold line) is the voltage on + no inverted IC1 input point. The positive effect is evident: the stationary state establishing to reach level of 30 ppm takes now about 3 s, instead of more than 10 s by previous solution. In real conditions, when R_3=1 kΩ (realized instrument in Fig. 6), both voltage curves in *Fig. 5* are coincided.

Fig. 6. The picture of realized instrument

Table 1. Performances of realized instrument

Measuring Range	10 mΩ	100 mΩ	1 Ω	10 Ω	100 Ω
Measuring Current	2 A	0.4 A	80 mA	16 mA	3.2 mA
Resolution 6/7 digits	10nΩ/ 1nΩ	100nΩ/ 10 nΩ	1μΩ/ 0.1 μΩ	10μΩ/ 1 μΩ	100μΩ/ 10 μΩ
Comparison Error (ppm)	5	1 / 0.1	1 / 0.1	1 / 0.1	1 / 0.1

Based on described solution, the realized low resistance comparator, *Fig. 6* reaches measuring resolution of 1 ppm in range of 0.01Ω to 100Ω, Table 1.

Conclusion

The paper presents an efficient method of parasitic voltage annulations in case of low resistance measuring. The problem occurred by the improvement of fixed range instrument to use different resistance ranges was easy and efficiently overcome. Using the proposed solution the initially goal is achieved: the unit becomes a multirange instrument, without big costs and a complex modification and extension. That was not the primary aim, nevertheless the time of the stationary state establishing is significant reduced. However, this improved the instrument performances, Table 1.

Mentioned instrumentation method is usually used in the Laboratories where high precision of metal resistances is required and is necessary for determining its elementary characteristics [10]. In addition, there are several applications where high sensitivity is a requirement, and such a method is very useful in such cases. There are several instruments that use similar measurement method to the one presented in the paper (HP 3458 System Multimeter, Keithley 8 1 /2 -digit Model 2002 High Performance Digital Multimeters) However, the measurement scale of those instruments is significantly less than one proposed here.

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References

1. **Kible B. P., Legg D. J.** A generalized Wheatstone bridge for comparing 1–Ω resistors. – IEEE Trans. Instrum. Meas., 1985. – Vol. 34. – P. 282–284.
2. **Wavetek Corporation.** – Data Sheet, 1997. – 9 p.
3. **Keithley Instruments Inc.** Low Level Measurements Handbook: Precision DC Current, Voltage, and Resistance Measurements (6^{th} ed.). – 2004. – 244 p.
4. **Radetic R.** Low resistance electronic comparator, PhD thesis. – University of Novi Sad, Faculty of Technical Sciences, Novi Sad, Serbia, 2009. – 150 p.
5. **Nuckolls B.** Practical Low Resistance Measurements // – Aero Electric Connection, 2004. – P. 1–6.
6. **Radetic R. M., Milivojevic D. R.** Chopper Stabilized Low Resistance Comparator Sensors, 2009. – No. 9(4). – P. 2491–2497.
7. **Radetic R. M., Milivojevic D. R., Despotovic V. M.** Optimization of Measuring Current for Chopper Low Resistance Comparator // Measurement Science Review, 2010. – Vol. 10. – No. 1. – P. 22–24.
8. **Barney G. C.** Intelligent instrumentation – Great Britain Prentice Hall International, 1988. – 467 p.
9. **Norton Harry N.** Handbook of Transducers. – Englewood Cliffs, NJ 07632, Prentice Hall, Inc., 1998. – 554 p.
10. **Vitorov V. V., Kharapov F. I.** Processing the Result of a Check of Measuring Instruments Using Stable Methods of Parameter Estimation Lincoln // Measurement Techniques, 2008. – Vo. 51. – No. 4. – P. 366–369.

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The article describes an efficient solution of parasitic voltage annulment applied in low resistance comparison. By development and design the low resistance comparator with many measuring ranges, occurred some difficulties with parasitic voltages. Theirs influence on measuring result is not negligible. To eliminate those disturbances, the analog voltage integration method is used. That is the way to nullify the parasitic voltages. Also, this electric circuit eliminates the influence of AC disturbances, which are consequence of network power supply (50 Hz frequency), independently of intensity of voltage amplifying. Ill. 6, bibl. 10, tabl. 1 (in English; abstracts in English and Lithuanian).

R. Radetic, M. Pavlov, D. R. Milivojevic. Efektyvus būdas mažos varžos komparatoriaus parazitinei įtampai panaikinti // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2012. – Nr. 5(121). – P. 59–62.

Aprašomas efektyvus būdas mažos varžos komparatoriaus parazitinei įtampai panaikinti. Projektuojant mažos varžos komparatorių, turintį daug matavimo diapazonų, iškilo problemų su parazitinėmis įtampomis. Jų įtakos matavimo rezultatui negalima paneigti. Siekiant pašalinti šiuos trūkumus, taikomas analoginis įtampos integravimo metodas. Tai leidžia panaikinti parazitines įtampas. Be to, elektrinė grandinė panaikina kintamosios įtampos trikdžių dėl maitinimo tinklo dažnio (50 Hz) įtaką nepriklausomai nuo įtampos stiprinimo. Il. 6, bibl. 10, lent. 1 (anglų kalba; santraukos anglų ir lietuvių k.).