Differential Second-Order Voltage-Mode All-Pass Filter Using Current Conveyors

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[1]***Abstract*—In this paper, a new circuit solution of analogue pseudo-differential second-order all-pass filter operating in the voltage mode is presented. Pseudo-differential, since both input and output terminals are differential, however, the circuit topology features single-ended structure. As active elements the differential difference current conveyors and second-generation current conveyors are advantageously used. The proposed filter features quality factor control without disturbing the pole-frequency using single passive element. The designed circuit is less complex compared to fully-differential solutions by maintaining sufficient common-mode rejection ratio. The behaviour of the filter is described by means of symbolic analysis and also by simulations using the UCC-N1B integrated circuit. Furthermore, the performance of the proposed pseudo-differential filter has been validated by experimental measurements.**

***Index Terms*—Analogue signal processing, all-pass filter, pseudo-differential, current conveyor, voltage-mode.**

I. INTRODUCTION

The frequency filters can be found in any electronic device and hence can be considered as the most frequently used function blocks while processing analogue signals. Although various types and topologies of frequency filters can be found in the open literature, still significant attention is paid to their design, where the new solutions follow different requirements, such as universality, multifunction, controllability, active element type, low power consumption, low supply voltage, high common mode rejection, *etc*. [1].

From the requirements listed above, mainly the type of the active element is considered, since based on the active element type chosen to implement the required circuit, the low power consumption and/or low supply voltage of the final function block can be also achieved [2], [3]. Besides the design of function blocks using advanced types of active elements, the design of differential filters gains an increased attention as such circuits feature the advantage of immunity from common mode noise signals, enhanced dynamic range, lower harmonic distortion, and reduce the effect of coupling between various blocks once compared to basic single-ended solutions [4], [5]. However, once describing the performance of any differential function block, only the input and output signals are assumed to be differential and from the mathematical point of view the inner structure of the function block is hidden. Therefore, the proposed circuits can be referred to as true- (or fully-) and pseudo-differential function blocks if the inner structure of the function block is also differential or rather remains single-ended, respectively. The true-differential function blocks generally feature very high common-mode rejection ratio, but the complexity of the circuit topology significantly increases [4]–[8]. On the other hand, the pseudo-differential structures are less complex from the viewpoint of their implementation and are still capable to ensure sufficiently high common-mode rejection ratio [9]–[13]. In practice, combined with true-differential circuits, the pseudo-differential function blocks can be used as last section(s) of front-end analogue signal processing path, where very high common-mode rejection ratio is no more required.

From various types of filters, the all-pass filters are widely used in analogue signal processing in order to transmit signals at frequencies equally well and change only the phase [14]. Based on that all-pass filters are used to correct the phase shift caused by analogue filtering operations without changing the amplitude of the applied signal or to delay on purpose the signal being processed. However, once designing pseudo-differential all-pass filters, the authors pay attention mainly to first-order solutions only [9]–[11]. In [12] a pseudo-differential second-order current-mode universal filter using seven active (Current Differencing Current Conveyors) and ten passive elements is presented, where only high-, low- and band-pass responses can be directly obtained. Another multifunction second-order pseudo-differential filter using three differential difference current conveyors (DDCC) and seven passive elements has been presented in [13]. This solution also offers only high-, low- and band-pass responses, and therefore, to obtain a band-stop or all-pass response additional circuitry is required. To the best knowledge of the authors, the only solution of pseudo-differential second-order all-pass filter has been presented in [15]. Although only single DVCC (Differential Voltage Current Conveyor) is employed in this

Manuscript received 7 March, 2016; accepted 24 April, 2016.
Research described in this paper was financed by the Czech Science Foundation under grant No. 16-11460Y and National Sustainability Program under grant LO1401. For the research, infrastructure of the SIX Center was used.

solution, three resistors and three capacitors, only one being grounded, are required. Furthermore, to obtain proper frequency response two matching conditions must be fulfilled, which is also a disadvantageous feature of the circuit from [15].

In this paper, using current conveyors as active elements, we focus on the design of the pseudo-differential second-order all-pass filter working in the voltage mode. The proposed structure uses three active elements and five passive elements, all being grounded. The advantageous features of the filter are high input impedance, no matching conditions, high common-mode rejection ration and the adjustability of the quality factor via single resistor without disturbing the pole-frequency of the filter.

II. THE DDCC AND CCII DESCRIPTION

The differential difference current conveyor (DDCC), whose electrical symbol is shown in Fig. 1(a), is a six-terminal network with one low-impedance current input X, three high-impedance voltage inputs Y1, Y2, Y3, and two high-impedance current outputs Z1, Z2. For ideal active element the relationship between the terminal currents and voltages is described as follows [2]:

$$v_{\mathrm{X}} = v_{\mathrm{Y1}} - v_{\mathrm{Y2}} + v_{\mathrm{Y3}}, \tag{1}$$

$$i_{\mathrm{Y1}} = i_{\mathrm{Y2}} = i_{\mathrm{Y3}} = 0, \tag{2}$$

$$i_{\mathrm{Z1}} = i_{\mathrm{X}}, \quad i_{\mathrm{Z2}} = -i_{\mathrm{X}}. \tag{3}$$

The second-generation current conveyor (CCII) is generally a four-terminal network as shown in Fig. 1(b). Compared to DDCC, the CCII features only single high-impedance voltage input terminal Y and the relation between the terminal currents and voltages for ideal CCII is given as [2]:

$$v_{\mathrm{X}} = v_{\mathrm{Y}}, \tag{4}$$

$$i_{\mathrm{Y}} = 0, \tag{5}$$

$$i_{\mathrm{Z1}} = i_{\mathrm{X}}, \quad i_{\mathrm{Z2}} = -i_{\mathrm{X}}. \tag{6}$$

Taking into consideration the non-idealities of the active elements, the relations between terminal voltages and currents of DDCC can be expressed as:

$$v_{\mathrm{X}} = \beta_1 v_{\mathrm{Y1}} - \beta_2 v_{\mathrm{Y2}} + \beta_3 v_{\mathrm{Y3}}, \tag{7}$$

$$i_{\mathrm{Z1}} = \alpha_1 i_{\mathrm{X}}, \; i_{\mathrm{Z2}} = -\alpha_2 i_{\mathrm{X}}, \tag{8}$$

where $\beta_j = 1 - \varepsilon_{vj}$ and $\alpha_k = 1 - \varepsilon_{ik}$ (for $j = \{1, 2, 3\}$ and $k = \{1, 2\}$) are the voltage and current gains of the DDCC, whereas $|\varepsilon_{vj}| << 1$ and $|\varepsilon_{ik}| << 1$ denote the voltage and current tracking errors, respectively. Similarly, the non-ideal behaviour of the CCII can be defined as follows:

$$v_{\mathrm{X}} = \delta v_{\mathrm{Y}}, \tag{9}$$

$$i_{\mathrm{Z1}} = \gamma_1 i_{\mathrm{X}}, \quad i_{\mathrm{Z2}} = -\gamma_2 i_{\mathrm{X}}, \tag{10}$$

where $\delta = 1 - \varepsilon_v$ and $\gamma_k = 1 - \varepsilon_{ik}$ (for $k = \{1, 2\}$) are the voltage and current gains of the DDCC, whereas $|\varepsilon_v| << 1$ and $|\varepsilon_{ik}| << 1$ represent the voltage and current tracking errors, respectively. Note that the currents flowing into the input voltage Y terminals of the active elements are assumed to be zero due to in practice high input impedance of these terminals.

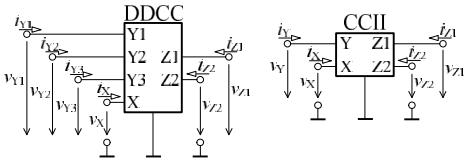

Fig. 1. Circuit symbols of (a) DDCC, (b) CCII.

III. PROPOSED ALL-PASS FILTER

For sake of description and analysis of the proposed pseudo-differential all-pass filter, the following notation is assumed [14]

$$v_{\mathrm{id}} = v_{\mathrm{i1}} - v_{\mathrm{i2}}, \quad v_{\mathrm{ic}} = \frac{v_{\mathrm{i1}} + v_{\mathrm{i2}}}{2}, \quad v_{\mathrm{od}} = v_{\mathrm{o1}} - v_{\mathrm{o2}}, \tag{11}$$

where v_{id}, v_{ic} and v_{od} denote differential-mode input, common-mode input and differential-output voltage, respectively. The differential input signal v_{id} is simply the difference between the two input signals v_{i1} and v_{i2}, whereas the common-mode input signal v_{ic} is the average of the two input signals. The differential-output voltage v_{od} is then represented as

$$v_{\mathrm{od}} = A_{\mathrm{dm}} v_{\mathrm{id}} + A_{\mathrm{cm}} v_{\mathrm{ic}}, \tag{12}$$

where A_{dm} and A_{cm} are the differential and common-mode gains, respectively. To evaluate the rejection of common-mode signals in preference to differential signals, common-mode rejection ratio (*CMRR*) is used

$$CMRR = 20 \log \left| \frac{A_{\mathrm{dm}}}{A_{\mathrm{cm}}} \right|. \tag{13}$$

The proposed pseudo-differential frequency filter is shown in Fig. 2. Assuming ideal active elements defined by (1)–(6), the output voltages v_{o1} and v_{o2} can be expressed as follows:

$$v_{\mathrm{o1}} = \frac{s^2 C_1 C_2 R_1 R_2 R_3 + R_3}{s^2 C_1 C_2 R_1 R_2 R_3 + s C_2 R_1 R_2 + R_3} v_{\mathrm{id}} + 0 \cdot v_{\mathrm{ic}}, \tag{14}$$

$$v_{\mathrm{o2}} = \frac{s C_2 R_1 R_2}{s^2 C_1 C_2 R_1 R_2 R_3 + s C_2 R_1 R_2 + R_3} v_{\mathrm{id}} + 0 \cdot v_{\mathrm{ic}}. \tag{15}$$

According to (11), for differential output voltage v_{od} it holds

$$v_{\mathrm{od}} = \frac{s^2 C_1 C_2 R_1 R_2 R_3 - s C_2 R_1 R_2 + R_3}{s^2 C_1 C_2 R_1 R_2 R_3 + s C_2 R_1 R_2 + R_3} v_{\mathrm{id}} + 0 \cdot v_{\mathrm{ic}}. \tag{16}$$

Comparing (15) to (12), the differential gain A_{dm} of the proposed pseudo-differential filter is

$$A_{\mathrm{dm}} = \frac{s^2 C_1 C_2 R_1 R_2 R_3 - sC_2 R_1 R_2 + R_3}{s^2 C_1 C_2 R_1 R_2 R_3 + sC_2 R_1 R_2 + R_3}, \qquad (17)$$

whereas the common-mode gain A_{cm} is zero, and therefore the common-mode rejection ratio (8) is infinitely high.

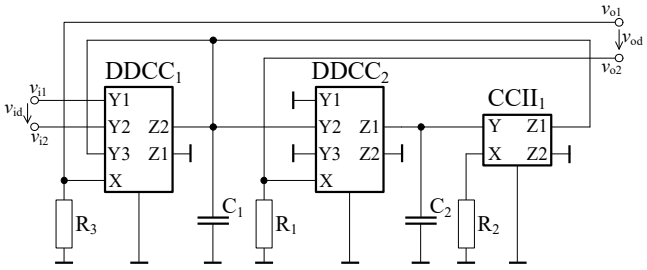

Fig. 2. Proposed pseudo-differential voltage-mode second-order all-pass filter.

From (12) it can be seen that a second-order all-pass filter is obtained from the proposed filter without any matching conditions. The angular pole-frequency ω_0 and quality factor Q of the filter are given as:

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}}, \qquad (18)$$

$$Q = R_3 \sqrt{\frac{C_1}{C_2 R_1 R_2}}, \qquad (19)$$

while the pass-band voltage gain in the whole frequency range is unity. From (13) it can be seen that the quality factor Q of the filter can be adjusted independently of the angular pole-frequency ω_0 changing the value of the resistor R_3, similarly as in [16], and in case of pseudo-differential all-pass filters has not been presented so far. To offer such feature, the use of five passive elements is obligatory. The use of $DDCC_1$ is also obligatory to obtain a differential input, similarly as *e.g.* in [13]. Furthermore, since the input signal is directly applied to the Y terminals of $DDCC_1$, the circuit features high input impedance, which is advantageous once connecting the circuit in cascade to other voltage-mode function blocks. Also, no capacitors are connected to the low-impedance terminals X of the active elements and hence, as shown later, no additional parasitic poles are created in the transfer function once non-ideal active elements are assumed. Note that the $DDCC_2$ can be generally replaced by an inverting second generation current conveyor (ICCII) [17] and hence more simple solution can be presented. However, for sake of further analysis described below, we assume the solution as shown in Fig. 2.

Taking into consideration the non-idealities of the active elements as described by (7)–(10), the reanalysis of the proposed filter yields the following differential and common-mode gains:

$$A_{\mathrm{dm}} = \frac{\beta_1 + \beta_2}{2} \frac{s^2 C_1 C_2 R_1 R_2 R_3 - s\alpha_2\beta_2 C_2 R_1 R_2 + \alpha_1\beta_2\gamma_1\delta R_3}{s^2 C_1 C_2 R_1 R_2 R_3 + s\alpha_3\beta_3 C_2 R_1 R_2 + \alpha_1\beta_2\gamma_1\delta R_3}, \qquad (20)$$

$$A_{\mathrm{cm}} = (\beta_1 - \beta_2) \cdot \frac{s^2 C_1 C_2 R_1 R_2 R_3 - s\alpha_2\beta_2 C_2 R_1 R_2 + \alpha_1\beta_2\gamma_1\delta R_3}{s^2 C_1 C_2 R_1 R_2 R_3 + s\alpha_3\beta_3 C_2 R_1 R_2 + \alpha_1\beta_2\gamma_1\delta R_3}, \qquad (21)$$

where for sake of simplicity the non-ideal parameters of $DDCC_1$ and $DDCC_2$ were assumed to be equal.

According to (13), the common-mode rejection ratio of the filter using non-ideal active elements is

$$CMRR = 20\log\left|\frac{\beta_1 + \beta_2}{2(\beta_1 - \beta_2)}\right|, \qquad (22)$$

and hence to ensure high rejection of common-mode voltage at the output, the voltage tracking errors ε_{vj} must be of such values to maintain $\beta_1 \approx \beta_2$.

Due to the non-ideal voltage and current gains of the active elements, the angular pole-frequency ω_0 and quality factor Q are affected:

$$\omega_0 = \sqrt{\frac{\alpha_1\beta_2\gamma_1\delta}{C_1 C_2 R_1 R_2}}, \qquad (23)$$

$$Q = \frac{R_3}{\alpha_3\beta_3}\sqrt{\frac{\alpha_1\beta_2\gamma_1\delta C_1}{C_2 R_1 R_2}}, \qquad (24)$$

however, it is obvious that the feature of adjusting Q independently of ω_0 changing the value of the resistor R_3 remains.

IV. Simulation Results and Experimental Measurements

To verify the behaviour of the proposed pseudo-differential second-order all-pass filter, first the SPICE simulations have been performed, where the active elements DDCCs and CCII were implemented using the macro-model of UCC-N1B integrated circuit [18], [19].

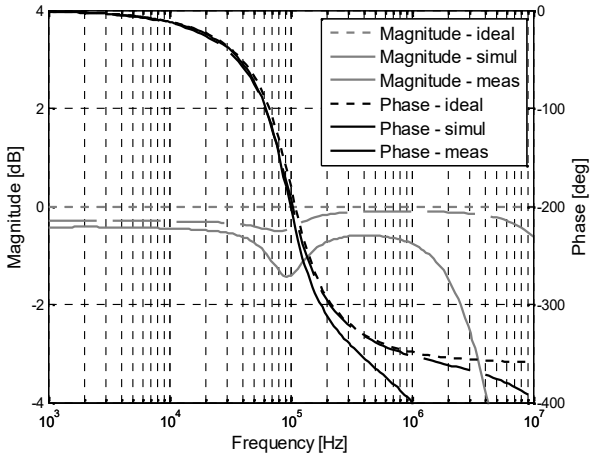

Fig. 3. Magnitude and phase response for f_0 = 100 kHz and Q = 1.

Assuming $C_1 = C_2 = C$ and $R_1 = R_2 = R$, for the pole-frequency of 100 kHz and capacitors C = 1 nF, using (18), (19) the values of resistors R_1 and R_2 are 1.6 kΩ. The magnitude and phase response of the filter is shown in

Fig. 3, whereas the value of the resistor R_3 was 1.6 kΩ to obtain unity quality factor (*i.e.* $Q = 1$).

From the simulation results (dashed line) it can be seen that the pole-frequency has dropped to approx. 95 kHz. Such reduction in pole frequency is caused by the real properties of the active elements and could be already expected from (23), (24) since the product of the voltage and current gains is $\alpha_1\beta_2\gamma_1\delta = 0.9192$ (see Table I). The pass-band gain is very close to unity (*i.e.* 0 dB) with the ripple of approx. 0.51 dB. The drop in magnitude at frequencies above 5 MHz is caused by the limited bandwidths of the voltage and current gains of the UCC-N1B (see Table I) that has been used to implement the required active elements' types.

TABLE I. NON-IDEAL PARAMETERS OF DDCC AND CCII ACCORDING TO THE PROPERTIES OF UCC-N1B [18].

Gain	[-] (typical)	Bandwidth	[MHz] (minimal)
Voltage gain β_1	0.975	$f_{-3dB-\beta1}$	40
Voltage gain β_2	0.968	$f_{-3dB-\beta2}$	46
Voltage gain $\beta 3$	1.009	$f_{-3dB-\beta3}$	44
Voltage gain δ	0.999	$f_{-3dB-\delta}$	32
Current gain α_1	0.965	$f_{-3dB-\alpha1}$	43
Current gain α_2	1.029	$f_{-3dB-\alpha2}$	49
Current gain γ_1	0.985	$f_{-3dB-\gamma1}$	45
Current gain γ_2	1.043	$f_{-3dB-\gamma2}$	48

In Fig. 4 the phase response for selected values of quality factor is shown. It can be seen that varying the resistor R_3 to adjust the required value of quality factor does not have any or very minor effect on the pole-frequency f_0 since for different values of Q the phase shift of −180 deg is approx. always at frequency 95 kHz. Similarly, in Fig. 5 the group delay is given where for selected values of quality factor {0.5; 1; 2} the group delay changes as {7.1; 3.6; 1.8} μs.

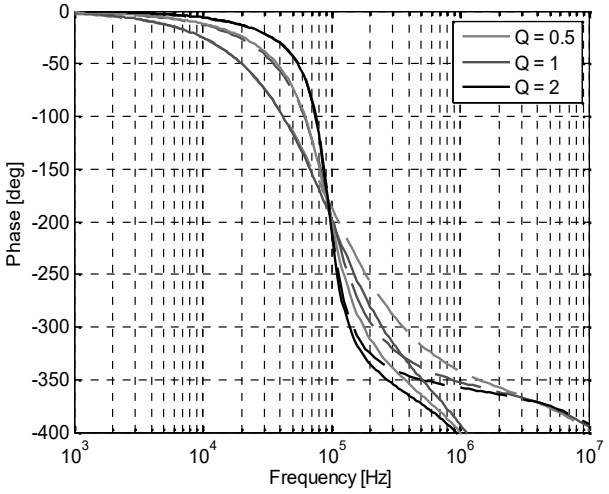

Fig. 4. Phase response of the filter for Q = {0.5; 1; 2} obtained by simulations (dashed line) and experimental measurements (full line).

According to (16) and using the typical values of the voltage gains β_1 and β_2 (Table I), the theoretical value of *CMRR* of the pseudo-differential filter is approx. 43 dB (dotted line). Note that from [9]-[13] and [15], only [13] determines the value of *CMRR*, which is approx. 62 dB. As can be seen from Fig. 6, the common-mode rejection ratio obtained by means of simulations (dashed line) agrees well to the expected value and is constant up to frequency approx. 1 MHz. Above this frequency the *CMRR* decreases, which is mainly caused by different bandwidth limitations of the corresponding voltage gains β_1 and β_2.

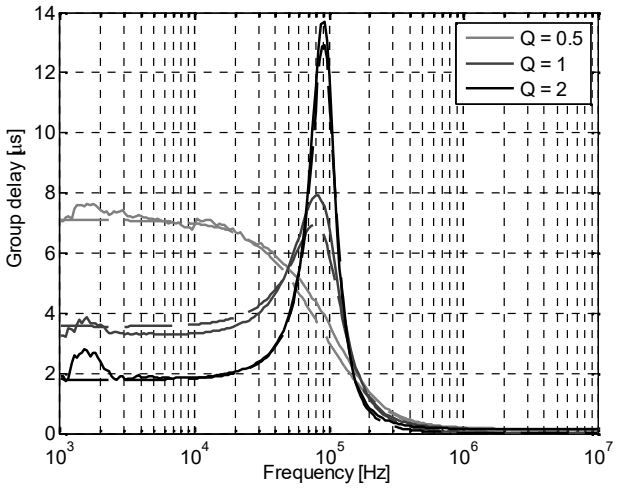

Fig. 5. Group delay of the filter for Q = {0.5; 1; 2} obtained by simulations (dashed line) and experimental measurements (full line).

The behaviour of the proposed frequency filter has been evaluated also by means of experimental measurements. To perform the experimental measurements the network analyser Agilent 4392A has been used. To measure the performance of the proposed pseudo-differential filter, single-ended to differential and differential to single-ended voltage convertors have been implemented using AD8476 [20], AD8271 [21] and AD8429 [22] integrated circuits as shown in Fig. 7.

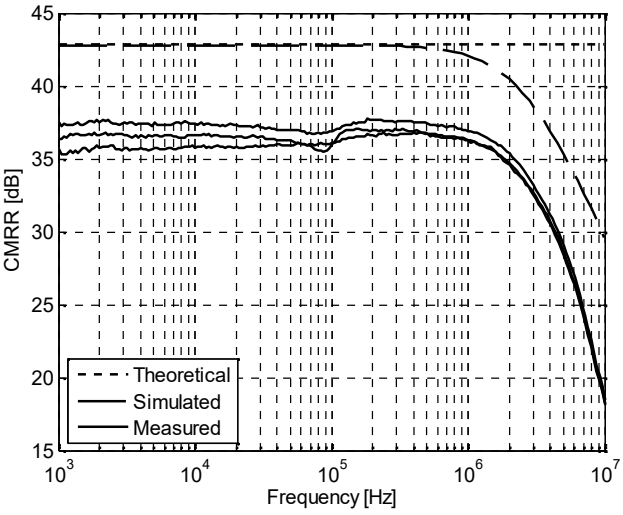

Fig. 6. Common-mode rejection ratio (*CMRR*) of the filter.

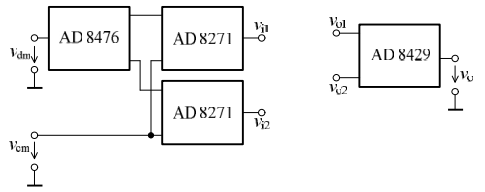

Fig. 7. Single-ended to differential (a); Differential to single-ended voltage convertor (b).

The magnitude and phase responses of the pseudo-differential filter for the values $f_0 = 100$ kHz and $Q = 1$, obtained by experimental measurements, are shown in Fig. 3 (full line) and compared to simulation results.

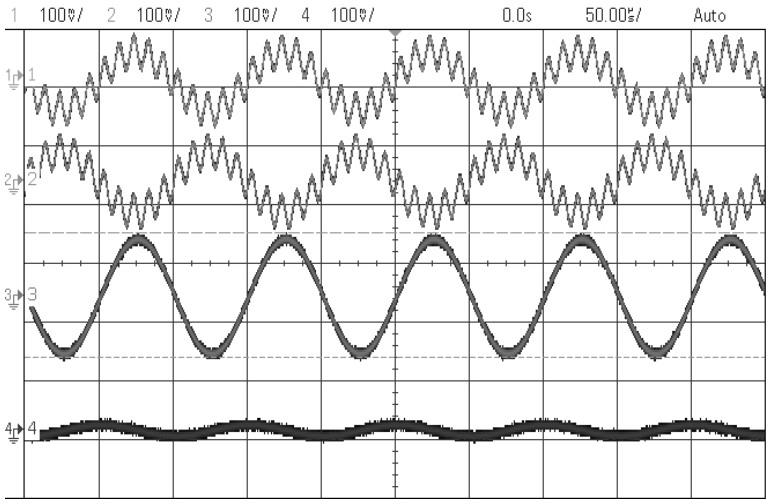

Fig. 8. Time-domain analysis of the pseudo-differential filter: trace 1 – v_{i1}, trace 2 – v_{i2}, trace 3 – v_{o1}, trace 4 – v_{o2} for v_{dm} 10 kHz, 200 mVpp and v_{cm} 100 kHz, 50 mVpp, 100mV/div, 50 µs/div.

Also here it can be seen that the pole-frequency f_0 has dropped by approx. 5 kHz from the theoretical value, similarly as it was observed during simulations. The pass-band gain shows a ripple of approx. 1 dB and decreases significantly above the frequency 3 MHz. Such drop in magnitude is mainly caused by the bandwidth limitation of AD8476, which is 6 MHz [20].

The measured phase and group delay (full line) of the filter for the values of quality factor set to Q = {0.5; 1; 2} are shown in Fig. 4 and Fig. 5, respectively. Also here significant agreement of the measurements with the simulation results can be observed. Inaccurate values of the group delay at low frequencies are caused by the selected IF (intermediate frequency) filter bandwidth of the network analyser that has been set to 30 Hz.

The common-mode rejection ratio of the pseudo-differential filter has been also evaluated by means of experimental measurements, where the results are shown in Fig. 6 and compared to theoretical value and simulations. It can be seen that for the selected values of the quality factor the measured *CMRR*s are very similar. The *CMRR* of the filter reached by measurements has decreased from its theoretical value to approx. 36 dB. This can be due to the fact that the theoretical value of *CMRR* is determined using typical values of voltage gains β_1 and β_2 (Table I), whereas in case of the UCC-N1B used for measurements, the difference between β_1 and β_2 was higher.

The proposed filter has been also analysed in the time domain. In Fig. 8, the voltages v_{i1} (trace 1), v_{i2} (trace 2), v_{o1} (trace 3) and v_{o2} (trace 4) of the filter are shown. The applied differential input voltage v_{dm} was 10 kHz, 200 mVpp, whereas the common mode voltage v_{cm} was 100 kHz, 50 mVpp. It can be seen that in the output voltages v_{o1} and v_{o2} the common mode signal is significantly suppressed as they mainly contain only the 10 kHz component.

V. CONCLUSIONS

In this paper new current conveyor based voltage-mode pseudo-differential second-order all-pass filter has been described. The filter uses two differential difference current conveyors and one second generation current conveyor as active elements and five passive elements – two capacitors and three resistors, whereas all are grounded. The proposed frequency filter features the possibility to control the quality factor Q independently of the angular pole-frequency ω_0 using single resistor. Furthermore, no matching condition of passive elements is required, the filter features high input impedance and high common mode rejection ratio. The behaviour of the filter has been verified by means of SPICE simulations and furthermore, by experimental measurements. The active elements have been implemented using the integrated circuit UCC-N1B. Both the simulation and experimental results prove the functionality of the proposed filter as they agree very well to the theoretical expectations. The value of *CMRR* reached by simulations is approx. 43 dB, which has decreased to approx. 36 dB in case of experimental measurements, is still sufficient and hence the pseudo-differential filters can be considered as the useful function blocks for analogue signal processing.

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