Log-domain Universal Biquad Filter Design Using Lossy Integrators

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***Abstract*— In this paper, a new current mode low voltage log domain Class A universal biquad filter is proposed. The proposed circuit is derived from the block diagram based on Kerwin-Huelsman-Newcomb (KHN) circuit using lossy integrators. The circuit can provide second-order low pass, band pass and high pass filter characteristics. State space method and translinear principle is used for circuit synthesis. The natural frequency *f*₀ and quality factor *Q* of the circuit is electronically tunable by varying amplitudes of the current sources. PSpice simulation results are given in order to verify the theoretical analysis. The simulations are performed with both ideal transistor models and AT&T CBIC-R type real transistor models.**

***Index Terms*—Active filters; analog circuits; bipolar transistor circuits; current-mode circuits.**

I. INTRODUCTION

The Kerwin-Huelsman-Newcomb (KHN) biquad has low sensitivity performance, low component spread and good stability characteristics [1], [2]. Two lossless integrators with feedback loops and a summer block establishes the classical KHN circuit that can function as three fundamental filters; low pass, high pass and band pass filters. There are many KHN biquad filters have been proposed in the literature synthesized by both voltage mode and current mode synthesis methods [3]–[12].

Current-mode operation offers greater linearity, lower power consumption and a wider bandwidth than voltage-mode operation counterparts [8]. Log domain filters are known as new generation current mode circuits which have drew attention of investigators since a general state space synthesis method had been proposed by Frey [13], [14]. Log domain filters are an important alternative because they have low voltage, low power consumption, high linearity and electronically tunable characteristics in continuous time active filter design [15], [16]. Log domain circuits are in the category of Externally Linear Internally Nonlinear (ELIN) circuits [17]. Based on the principles of translinear circuits, the operations in log domain circuits are nonlinear, while the transfer function is kept to be linear [13], [17].

Log domain filters use companding in signal processing idea [18], [19]. The input current is compressed by a logarithmic function using a bipolar transistor. A bipolar transistor's emitter-base voltage is logarithm of the current of the device. The output voltage is expanded by applying the signal to a bipolar transistor's base-emitter junction. The output current is exponential of the output voltage. The transfer function is linear because output function is the reverse function of the input function. Companding in signal processing offers a large scale of dynamic range [19].

The aim of this study is to gain the advantages of KHN circuit structure, log-domain characteristics and companding idea listed above. The major difference of the proposed circuit from original KHN structure is lossy integrators that are used for our design.

The proposed circuit in this work is designed for Class A operations. There are various works for Class A and Class AB log domain filter circuits in the literature [20]–[24].

In this paper, a new current mode log domain Class A universal filter based on KHN biquad is synthesized by using the state-space synthesis method [13], [15].

II. DESIGN

The original KHN biquad circuit consists of integrator blocks, summer blocks and feedbacks. The idea of modifying KHN block diagram by using lossy integrators is proposed by R. Arslanalp [25]. By using this idea, the proposed block diagram is shown in Fig. 1. Proposed work handles this block diagram and it is synthesized in log domain in order to gain advantages of log domain. In the block diagram, y_{LP}, y_{HP}, y_{BP} yields to low pass filter output, high pass filter output and band pass filter output respectively:

$$y_1 = u + \left(2 - \frac{1}{Q}\right) y_2 - \left(2 - \frac{1}{Q}\right) y_{LP}, \tag{1}$$

$$y_2 = \frac{\omega_0}{s + \omega_0} y_1, \tag{2}$$

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$$y_{LP}=\frac{\omega_0}{s+\omega_0}y_2=\frac{\omega_0^2}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}u, \tag{3}$$

$$y_{HP}=u-y_2+\left(1-\frac{1}{Q}\right)y_{BP}=\frac{s^2}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}u, \tag{4}$$

$$y_{BP}=y_2-y_{LP}=\frac{\omega_0 s}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}u. \tag{5}$$

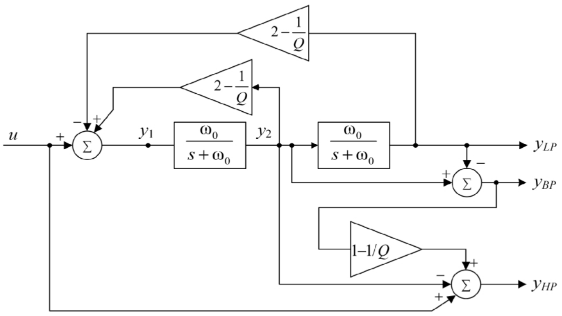

Fig. 1. Proposed universal biquad filter block diagram [20].

III. LOSSY INTEGRATOR

Realization of the lossy integrator and multiplier blocks are needed to design the Class A log domain circuit based on Fig. 1. The circuit is operating in current-mode so there is no need to design current summer blocks.

The log domain lossy integrator design procedure is the first step. The lossy integrator block will be synthesized by general state-space method of Class A log domain circuits explained in [13], [21]. Let the following transfer function to establish the lossy integrator

$$H(s)=\frac{y(s)}{u_0(s)}=\frac{\omega_0}{s+\omega_0}, \tag{6}$$

where ω_0 is the cut off frequency of the filter.

The state space representations of (6) are shown below:

$$\dot{x}=-\omega_0 x+\omega_0 u_0, \tag{7}$$

$$y=x, \tag{8}$$

where x is the state variable, u_0 is the input, y is the output. Suppose that the following mapping functions are applied to the state and input variables:

$$u_0=I_s e^{v_0/Vt}, \tag{9}$$

$$x=I_s e^{v_1/Vt}. \tag{10}$$

By using (7)–(10) and multiplying with

$$\frac{CV_t}{I_s e^{v_1/V_t}}. \tag{11}$$

we have:

$$C\dot{v}_1=-I_f+I_f e^{(v_0-v_1)/V_t}, \tag{12}$$

$$y=I_s e^{v_1/V_t}, \tag{13}$$

where $I_f=\omega_0 C V_t$, and V_t is the thermal voltage of the transistor.

(12) can be written as follows

$$C\dot{v}_1=-I_f+I_s e^{(v_0+V_f-v_1)/V_t}. \tag{14}$$

where $V_f=V_t\ln\left(\frac{I_f}{I_s}\right)$.

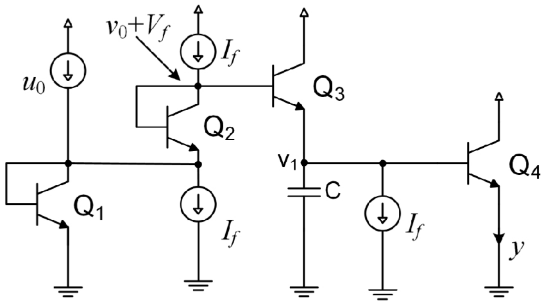

Fig. 2. First order Class A log domain lossy integrator.

The left side of the (14) can be considered as a grounded capacitor's current which is connected to the node that has voltage of v_1. The right side of (14) can be realized by a current source and a bipolar transistor that its base is connected to the node which has a voltage of v_0+V_f and its emitter is connected to the node which has a voltage of v_1. The circuit synthesized with these considerations is shown in Fig. 2.

IV. CURRENT MULTIPLIER

The second step is synthesizing a current multiplier. The circuit design procedure is based on translinear principle [26]. The following equation defines the current multiplier block

$$i_{OUT}=\frac{I_{DC1}}{I_{DC2}}i_{IN}. \tag{15}$$

The realization of current multiplier circuit based on translinear principle is shown in Fig. 3.

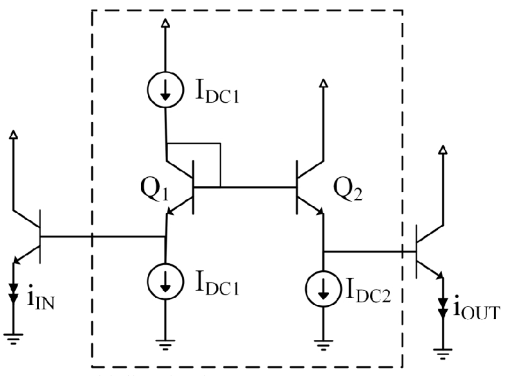

Fig. 3. Current multiplier circuit.

By using the designed circuits in Fig. 2 and Fig. 3 in the block diagram of Fig. 1, the whole circuit designed shown in Fig. 4.

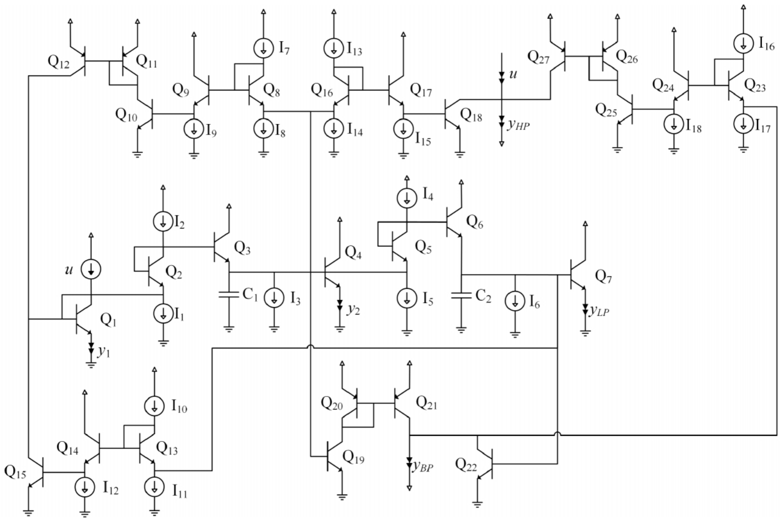

Fig. 4. Class A log domain universal biquad filter.

V. SIMULATION RESULTS

The designed log domain universal biquad filter is simulated in PSpice by using ideal transistors that are default BJT models with BF = 10000. This simulation is made to check whether results obtained from theoretical works and simulation results are in agreement. Input current u consists of DC and sinusoidal parts because of the Class A operation. DC part of the input is set to be I_f, the sinusoidal part is set to be $0.1I_f$. The supply voltage is 2.25 V. The values of capacitances of lossy integrators are chosen to be $C_1 = C_2 =$ 24.6 nF. The values of current sources I_1-I_6, I_9, I_{12}-I_{18} are set to be I_f; I_7, I_8, I_{10}, I_{11} are set to be $(1-1/Q)I_f$ where $I_f =$ 500 µA. This yields a pole frequency of f_0 = 125 kHz for PSpice simulations whereas calculated value of this parameter from $I_f = \omega_0 C V_t$ is also f_0 = 125 kHz. The simulation results are in agreement with theoretical results so the next step is to perform simulations by using AT&T CBIC-R type real transistor models in [13]. Because of the nonlinearities of the real transistor models, the current gain values of some blocks in Fig. 1 are lower than expected. To overcome this problem, some transistors' area values and some current sources' values are slightly modified.

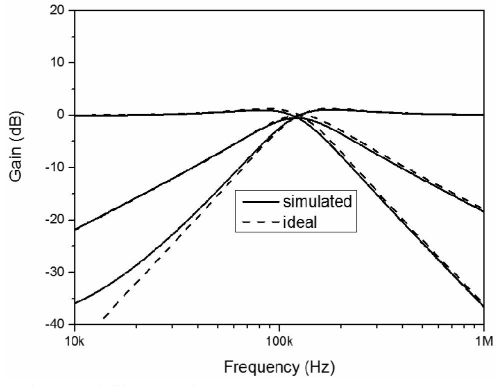

Fig. 5. Fundamental filters' gain responses.

The first simulation is performed for AC response of the circuit with pole frequency of f_0 = 122 kHz and quality factor Q = 1. The filter responses of all fundamental filter characteristics are obtained. The gain characteristics of fundamental filter responses (lp, hp and bp) are given in Fig. 5. The figure shows that the ideal and the simulated results are in accordance with each other. The pole frequency and the quality factor is adjustable by varying values of the current sources. These characteristics give us the advantage of using this circuit for wide frequency areas without any modification on circuit structure. In Fig. 6 the quality factor Q is electronically set to 2. If Q is set greater than 2, the difference between simulations with ideal models and real models gets higher due to circuit limitations. In Fig. 7 it is shown that the center frequency f_0 is swept two decades by only varying the values of current sources which I_f is set to 5 µA for f_0 = 1.3 kHz, I_f is set to 50 µA for f_0 = 13 kHz, I_f is set to 500 µA for f_0 = 122 kHz where the amplitude of the sinusoidal part of input signal is set to $0.1I_f$.

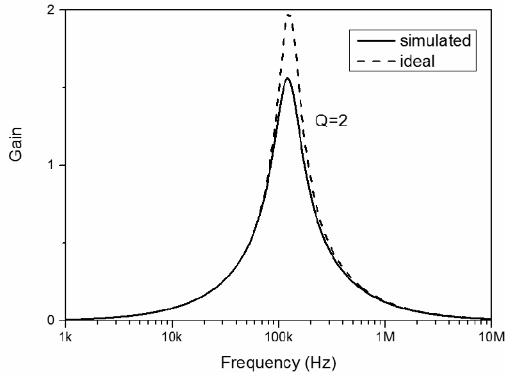

Fig. 6. Tunable Q for band pass filter.

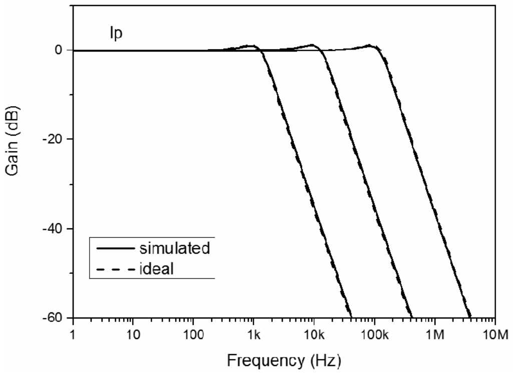

Fig. 7. Tunable f_0 for low pass filter.

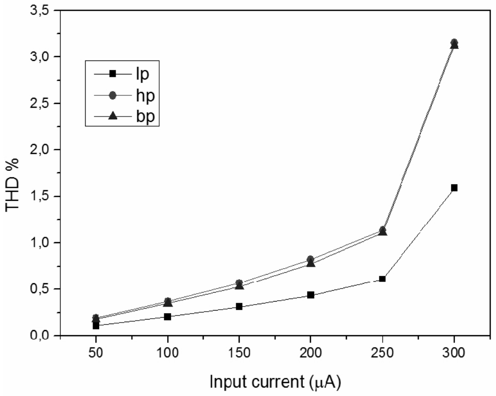

Fig. 8. THD values.

THD of the output signal was measured for all filter responses for some input current values. The results are shown in Fig. 8. DC offset of the input u is set to 500 μA, sinusoidal part of input signal is swept from 50 μA to 300 μA.

VI. CONCLUSIONS

In this study, a Class A log domain filter based on KHN structure is designed to obtain low pass, high pass and band pass filter characteristics. It is the first time that lossy integrators are used to design this type of filter circuit. Lossy integrator block and multiplier block have been synthesized in order to realize the circuit. Lossy integrator block is synthesized by state space synthesis method and translinear circuit theory. Multiplier block is also synthesized by translinear circuit theory. The filter's quality factor Q and the pole frequency f_0 is electronically tunable by only varying values of the DC current sources. The circuit can perform universal filter responses namely low pass, high pass and band pass. The filter circuit is simulated in PSpice by using both ideal and real transistor models. The simulation results verify the validity of the designed circuit. Both time domain and frequency domain results show that the designed filter has the advantages of electronic tunability of quality factor Q, the pole frequency f_0 and also the good stability behavior of KHN structure.

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