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Implementation of Sense Amplifier in 0.18-µm CMOS Process

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Introduction

In RFID transponders, embedded nonvolatile memories (NVM) like EEPROM are essential. Reading and writing operations of EEPROM are usually the edge factors in low-power RFID transponders [1, 2]. The power of the EEPROM sense amplifier must be lower to increase RFID reading space [3]. In EEPROM, the read access time is a key factor to determine the read path, which is strongly affected by the Sense Amplifier (SA). One of the main challenges for new generation non-volatile memories is to develop a robust and high-speed read circuit with a low power supply voltage. As the power supply becomes lower, the design of a high-speed low-power sense amplifier becomes very critical [4].

At present, current-type sense amplifiers have been extensively implemented for EEPROM sensing. Usually, current-comparing methods are used frequently than voltage-type sense amplifiers due to the advanced speed and steadfastness [5]. However, large power consumption, increasing sensing time and extra control logic to prevent incorrect read out current are some of the drawbacks of this conventional current sensing method. These limitations are inapplicable to the low-power RFID transponders. Moreover, voltage-type sense amplifiers necessitate lower current and power than current-type sense amplifiers [5, 6].

A number of voltage type SA have been designed so far to accomplish the reduced NVM sensing current. However, researchers experienced the reading consistency issues at lower power supply voltage and higher reading current [6]. Liu et. al. implemented a low cost, low power and highly reliable voltage SA in SMIC 0.35µm CMOS process [7]. The research showed that with the power supply 3.3V, the charging time required for the voltage SA is 35ns and the highest average current consumption during the sense period is 40µA. However, the lowest power supply voltage required for the design was 1.4V. Nevertheless, at present this lowest voltage is not satisfactory low for RFID transponder.

In this research, a low voltage SA for EEPROM memories in RFID tag is designed to attain the lower reading current and power where low voltage sensing method has been used to achieve better circuit performance, and decreasing sensing time.

EEPROM and sense amplifier

Though the floating-gate devices has many limitations, but low power design on circuit level is still the best solution for RFID applications [8].

To direct logic operations, the control unit, row and column decoders and high-voltage switches are used inside EEPROM. On the other hand, the charge pump used to generate a high voltage for writing operations. The sense amplifiers are useful for sensing the *'0'* and *'1'* bit. Whereas, input/output (I/O) interfaces are used as a carrier for output data.

Several researchers [3, 5, 9] demonstrates the design of conventional SAs by using current sensing method. Fig. 1 shows the circuit diagram of the conventional sense amplifier.

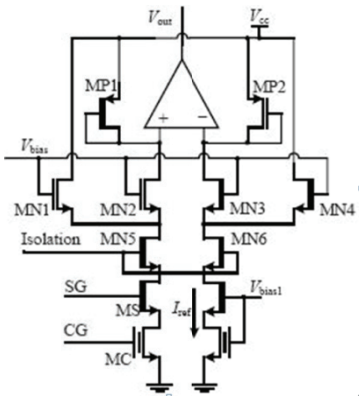

Fig. 1. Conventional sense amplifier [3, 5, 9]

In the conventional SA circuit, the measurement of *'0'* and *'1'* are classified by using a differential circuit for

steadiness between the read out current and a reference current. However, the circuit has some drawbacks:

1) High power consumption is pointed as the most common problem of the conventional SA. A large reference current I_{ref} is required by the conventional SA circuit to differentiate between *'0'* and *'1'* data, which is typically the average of the read out currents. Tens of μA reference current is needed for steadiness. Thus, a large amount of read out current: I_{ref} ε ($nI_{ref,}$ $3nI_{ref}$) is required for the conventional SA for reading parallel data. Where, n is the number of bits read out in parallel [7];
2) Floating gate transistor changes the *'0'* and *'1'* current levels by attribute degeneration. Thus, for *'0'* and *'1'* the perfect selection of I_{ref} is differed from the initial average of the read out currents. Therefore, a minor variation between the read out current and the reference current for one level to other is produced. This distinction of the current, results an amplified sensing time [10];
3) The conventional SA circuit is constructed with many floating gate transistors, which stores charge. Hence, it is important to use an extra control logic circuit to prevent incorrect read out current and correctly manage the charge stored on key nodes.

However, to reduce the sensing time and to make the power consumption lower, a low voltage sense amplifier is essential for non-volatile memories like EEPROM in RFID tag. Moreover, to avoid incorrect read out current, the low voltage sense amplifier will not require an extra control logic circuit.

Voltage type sense amplifier design

The Compact Model (CM) of the Floating Gate (FG) devices has been used in conventional SA for circuit simulations. However, this compact model experienced two main limitations. First, thin gate oxide transistors with lightly or medium Doped Drain (LDD/MDD) diffusions are the main aim of MOS compact model. More than 7nm thickness is used as the oxide of the FG devices while the source and drain junction usually abrupt. As a result, the existing transistor models might become essential to adapt with this same type of devices. Second, between the control gate node and the source, drain and body nodes, few coupling capacitance are exists. Moreover, two neighbor cells may be affected by the coupling capacitance as memory cells are getting closer and smaller one to the other. Based on these limitations, a voltage-mode sense amplifier is designed with only one capacitor between the control gate node and the source, drain and body nodes. This method reduces the effect of coupling capacitance between the transistors. Moreover, this method is useful to achieve the lower sensing power/current and higher reading fidelity without speed deprivation compared to the conventional sense amplifier.

Fig. 2 shows the improved designed SA circuit composed of charge controlling and voltage sensing circuits. The memory cell consist of a floating gate transistor MC and a select transistor MS. To reduce the coupling capacitance between two adjacent memory cells only one capacitor has been used between the control gate and the FG node (which is the gate of the MOS transistor MC).

In the modified sense amplifier, the selected sensing path is controlled by the control gate (CG) and transistor MC and a selecting gate (SG) with the transistor MS. The task of the decoders is to control this selecting gate and the terminal CG is determined by a voltage between the two thresholds of memory cells.

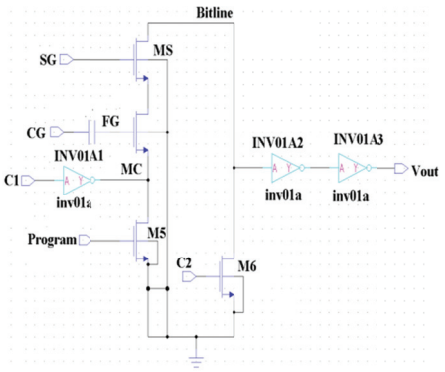

Fig. 2. The circuit diagram of the proposed low voltage sense amplifier

For the improved voltage-type SA, the EEPROM memory cell implemented in 27°C operating conditions of the CEDEC 0.18 μm process. The threshold voltage of transistor MC is set to 1.5V to store a *'0'* signal; and the threshold voltage is set to −1V to store a *'1'* signal. Fig. 2 shows that the operation states of this SA are controlled by the three control terminals: A, B and C.

This modified voltage sense amplifier has two states: working state and out-of-work state. In the out-of-work state, to ensure the drain and source of the memory cell are at low level, all the three inputs A, B and C are set to *'1'*. On the other hand, for the working state, the CG and the SG are set as:

$$V_{CG} = (P + Q)/2\,, \tag{1}$$

$$V_{SG} = Vdd, \tag{2}$$

where P is the threshold voltage of the MC when storing a *'0'* signal, and Q when storing a *'1'* signal.

At the beginning to turn off N2 and N3 transistor, inputs C and B are set to *'0'*. After that, A is set to *'0'*. At this time, V_{out}=0 when the stored signal of MC is *'0'*. Additionally, when the stored signal is *'1'*, the BL (bit line) is charged to

$$V_{BL} = \min(V_{dd} - V_{tms}, 1.5 - V_{tmc}), \tag{3}$$

where V_{tms} is the threshold voltage for MS transistor, and V_{tmc} is the threshold voltage for transistor MC.

The stored signal *'1'* will be generated correctly at V_{out} as long as

$$V_{BL} > \frac{V_{dd}}{2}\,. \tag{4}$$

In Fig. 2, for sensing the stored voltage *'0'* or *'1'* at transistor MC, the drain and source of MOS transistors employ bidirectional diffusion [11]. This voltage mode SA

enables costs to be reduced; since it has no bias circuit. The parasitic capacitance is utilized as the charging load at the drain of N3 transistor. To decrease the charged voltage, the threshold voltage of the two inverter composed of NMOS transistors N4, N5 and PMOS transistors P2, P3 have been added. This will result a shorter charging time of BL and makes the lower read power dissipation. Additionally, the newly designed voltage type SA is capable of resisting the degeneration features of the floating gate transistor by using a voltage sensing method rather than a current sensing method. The transient current and charges for charging in one read process are described respectively:

$$\frac{\partial(V_{BLT}\, C_{N3})}{\partial t} = \beta\,(V_{CG} - V_{tmc} - V_{BLT})^2\,, \qquad (5)$$

$$\int_0^T \beta\,(V_{CG} - V_{tmc} - V_{BLT})^2 dt = C_{N3}\,(V_{CG} - V_{tmc})\,, \qquad (6)$$

where V_{BLT} is the transient voltage of the BL,C_{N3} is the parasitic capacitance at the drain of N3 , and T is the charging time $\beta = \mu_n\, C_{ox}\, W/(2L)$.

Using equation (5) and (6), the average charging time and current can be obtained during one read period.

Results and discussion

The 27°C operating condition for the modified voltage-type sense amplifier and the conventional sense amplifiers have been designed and simulated in CEDEC 0.18-µm CMOS process. Simulations is executed to evaluate the circuit performance of the modified sense amplifiers with the previously reported voltage-type SA [12]. The transistors involved in the sensing circuitry were of equal size *W/L= 0.18µ/0.18µ.* The significant design factors are C1=0.1pF, SG=3V and CG=1.5V.

By using the critical design parameters listed in above table the output data (V_{out}) for the modified SA is shown in Fig. 3 under 2.6V power supply voltage. As shown in Fig. 4, the modified voltage type SA reads *'0'* data at the beginning. At 0.4µS the SA reads *'1'*. The circuit is also able to work >2.6V, but above this operating voltage, the circuit experience noises.

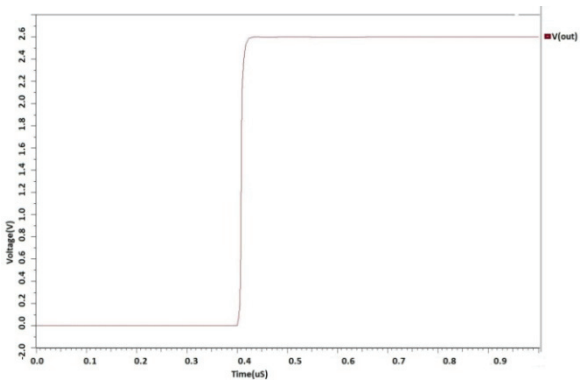

Fig. 3. Simulation results of voltage SA for a 2.6V power supply

Furthermore, depending on the principle of the memory cell, V_{CG} in equation (1) is the best value for voltage sensing and a lower voltage can be set for V_{CG}. Using equation (2) and regulating the threshold voltage of the inverter in Fig. 3, the modified voltage mode SA is capable of operating at voltages as low as 1V. The V_{out} data for a 1V power supply voltage are shown in Fig. 4.

The simulation results in Fig. 4 shows that the voltage required by the voltage-type SA can be significantly reduced from 2.6V to 1V, where the voltage was controlled by CG. In order to show the correct behavior of the voltage-type SA, the power supply voltage is set to 1V and the capacitive load to 0.1 pF.

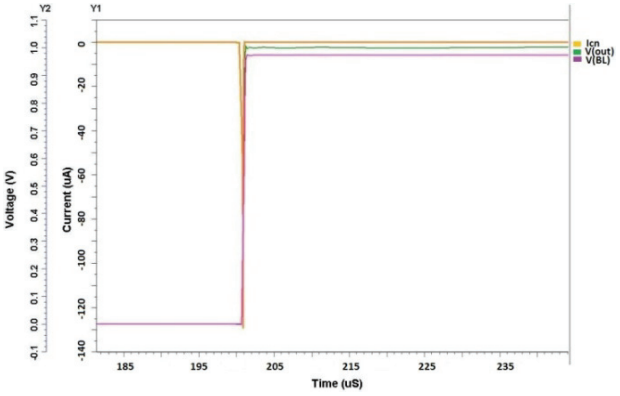

Fig. 4. Simulation results of the average current I_{cn}, V_{out} and V_{BL}

The corresponding current consumption for the modified voltage-type SA is also shown in Fig. 4. Here the average current consumption during the read period is only 43µA for the maximum clock speed of 20MHz. This feature is useful for some electronic systems focused on low voltage and low power such as RFID transponder.

Fig. 4 also presents a comparison results among the Vout data, the average current consumption during the read period, and the corresponding bit line voltage under 1V power supply voltage. The figure further proves that the SA is capable of operating at a voltage as low as 1V. The circuit is also able to work <1V, but in this operating voltage, the circuit experience noises.

Generally, the required working temperature range of the RFID tag is from −25°C to 85°C. As, the modified voltage-type SA circuit is able to work within the temperature range from −25°C to 125°C. Therefore, this modified circuit has no power differentiation in working temperature of RFID tag.

A comparisons study of voltage-type sense amplifiers between this work and Liu et. al with minimum and maximum voltage level is shown in Table 1. From the study, it is shown that the circuit is able to work within 1V to 2.6V power supply voltages, which is lower than the Liu et. al.

Table 1. Comparison study of voltage-type sa between liu et. al. and this work

Research	Vdd (Min)	Vdd (Max)	CMOS Technology
Liu et. al.	1.4V	3.3V	0.35 µm
This Work	1V	2.6V	0.18 µm

The modified low voltage-type SA circuit layout is designed in CEDEC 0.18-µm CMOS process. In Fig. 5, the completed chip layout of the modified low voltage SA is presented. In this layout, the capacitor connected with the control gate transistor is about 0.1pF. This small capacitor

only takes a small area of the circuit to reduce the cost of the whole chip. In this research, *W/L = 0.18μ/0.18μ* is the size for each cell of the MOS transistors, which also proves that the modified SA circuit size is lower than the circuit size designed by Liu et. al.

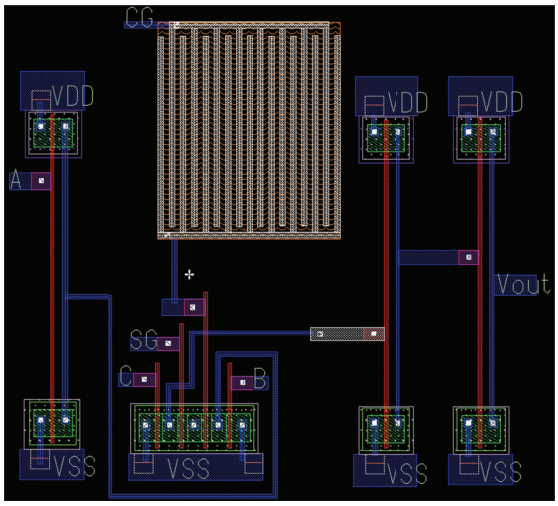

Fig. 5. A layout design of the low voltage-type SA

Conclusions

An improved design and a comparative study of low voltage SA circuit using a voltage sensing method is presented in this research. The modified circuit has been designed by using the CEDEC 0.18-μm CMOS embedded EEPROM process. In this research, the bidirectional conduction between the drain and source of MOS transistors is used to sense the stored voltage *('0'/'1')* at the floating gate transistors. According to the research results, it has been proven that, the circuit is capable of working over a voltage range from 1V to 2.6V power supply. The results also verify that the modified voltage-type SA required lower reading current/ power than the voltage-type SA designed by Liu et. al. Moreover, the simulation results confirm that this low voltage SA is free from the power delineation caused by the temperature change. Additionally, the circuit size reduced significantly by using small transistors and capacitors.

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Sense Amplifier is one of the major circuits in CMOS nonvolatile memories. The aim of this research is to implement Sense Amplifier in 0.18μm CMOS process to achieve both the lower reading power and superior reliability for sensing operation. In RFID transponder, EEPROM are used to store data. Memory access time, power dissipation and the reliability of an EEPROM is vigorously influenced by the features of the SA. Current type SA experience the larger current or power dissipation problems, which is not suitable for low voltage applications of RFID transponder. The proposed voltage-type SA is able to execute under a very low power supply voltage (VDD) between 1V to 2.6V VDD. The SA circuit implemented within the temperature range from -25^{0}C to 125^{0}C. The compact layout design has been carried out to evaluate the efficiency of the circuit. The modified low voltage-type SA is appropriate for low-voltage applications like RFID EEPROM. Ill. 5, bibl. 10, tabl. 1 (in English; abstracts in English and Lithuanian).

L. F. Rahman, M. B. I. Reaz, M. A. M. Ali, M. Marufuzzaman. Šuntinio stiprintuvo įdiegimas 0,18 μm CMOS procese // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2012. – Nr. 4(120). – P. 113–116.

Šuntinis stiprintuvas (ŠA) yra viena iš pagrindinių CMOS atminties grandžių. Tyrimo tikslas – 0,18 μm CMOS procese įdiegti šuntinį stiprintuvą, siekiant sumažinti skaitymo galią ir padidinti jutimo operacijos patikimumą. RFID transponderyje EEPROM naudojama duomenims saugoti. Atminties informacijos išrinkimo trukmė, galios suvartojimas ir EEPROM patikimumas labai priklauso nuo ŠA savybių. Srovinio tipo ŠA sukelia didesnių srovių ar galios, kurios yra netinkamos žemos įtampos RFID transponderio taikomosioms sistemoms, išskaidymo problemų. Pasiūlytas įtampos tipo ŠA gali veikti esant labai mažai įtampai – nuo 1 V iki 2,6 V. ŠA grandynas skirtas temperatūrų nuo -25 ^{0}C iki 125 ^{0}C sričiai. Modifikuotas žemos įtampos SA yra tinkamas mažos įtampos aplikacijoms kaip RFID EEPROM. Il. 5, bibl. 10, lent. 1 (anglų kalba; santraukos anglų ir lietuvių k.).