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Simulink Model of Parallel Resonant Inverter with DSP Based PLL Controller

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***Abstract*—Resonant converters can operate at high switching frequencies with low switching losses. However, in order to reduce switching losses resonant frequency has an important role in the design. In this study, a DSP based closed loop phase locked loop (PLL) control algorithm for parallel resonant inverter is designed and simulated with MATLAB/Simulink. The validity of the Simulink model of current source inverter is tested for different loads and gain values obtained from Jury's stability. The developed DSP controlled parallel resonant inverter tracks the resonant frequency and achieves soft switching.**

***Index Terms*—Phase locked loop, resonant frequency tracking, current source inverter, MATLAB/Simulink.**

I. INTRODUCTION

Power density of the converters can be increased by increasing the switching frequency. Current fed and voltage fed converters are the most widely used topologies for high frequency resonant power conversion. Among them current source topology has short circuit protection capability, and power switches can be driven with a simple gate drive circuit. Current source parallel resonant topology is used in many applications such as induction heaters [1]–[5], inverters [6]–[10], dc-dc converters [11]–[13], electronic ballasts [14], battery chargers [15] *etc*.

In parallel resonant inverters it is necessary to keep the output voltage and inverter current in phase to achieve the soft switching conditions. For this purpose resonant converters can be controlled by using self-oscillating driver [16] or a phase locked loop (PLL) Integrated Circuit (IC) [1]. Alternatively high speed microcontrollers allow the designers to design sensitive and closed loop control systems for power electronic applications [17]. In addition monitoring the parameters or over current/voltage, over temperature protection of the system can be implemented by using microcontroller in digitally controlled converters. Recently, DSP based PLL control system for series resonant inverter is presented before [17], [18].

In this paper, a current source parallel resonant inverter is analysed and a PLL algorithm is designed for a DSP controller based inverter circuit. The MATLAB/Simulink model of the inverter is controlled with a PLL block. Stability of the system is tested with Jury's stability method and the inverter is controlled and simulated for different load conditions. Simulation results show that switching frequency of the current source inverter changes automatically and tracks the resonant frequency for different conditions.

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II. CURRENT SOURCE INVERTER

The current source parallel resonant inverter and its equivalent circuit are shown in Fig 1. The inverter consists of a filter inductor (Lf), two unidirectional power switches and parallel RLC circuit. The voltage source (V) with the filter inductor can be represented by a current source; Fig. 1(b) shows the equivalent circuit with the current source.

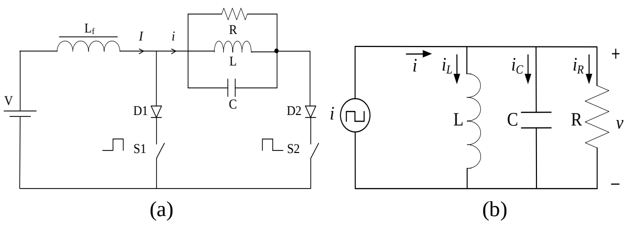


Fig. 1. The current source inverter (a); equivalent circuit (b).

In steady state, approximately constant dc current is switched and power switches feed the parallel RLC resonant circuit with a square wave current. The output voltage and power of the system are functions of the switching frequency (*f*). Maximum power transfer can be achieved when the switching frequency equals the resonant frequency (f_r) [4]. The resonant frequency and switching frequency are given by:

$$\omega_r = \frac{1}{\sqrt{LC}} = 2\pi f_r, \quad (1)$$

$$\omega = 2\pi f. \quad (2)$$

In the inverter, the fundamental component of the generated square wave current is as follows [11], [13]:

$$i_1(t) = I_m \sin \omega t, \quad (3)$$

$$I_m = \frac{2}{\pi} I. \quad (4)$$

For $\omega = \omega_r$, the resonance circuit behaves like a purely resistive load and the switch current is in phase with the load voltage. Therefore zero voltage switching (ZVS) can be accomplished. Figure 2 shows the switch current and voltage waveforms for the resonance mode.

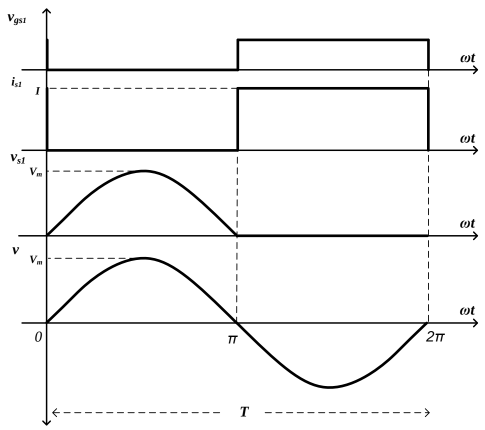


Fig. 2. The current and voltage waveforms of S1 ($\omega = \omega_r$).

Loaded quality factor of the parallel resonant circuit at the resonant frequency is

$$Q = R / \omega_r L. \tag{5}$$

The phase angle φ between the resonant circuit input current (i) and output voltage (v) can be calculated by

$$\varphi = \arctan\left[Q(\omega / \omega_r - \omega_r / \omega)\right]. \tag{6}$$

III. DSP-BASED PLL CONTROL SYSTEM

A. Mathematical Model

Phase locked loop (PLL) circuits automatically track the resonant frequency to keep the soft switching under different load conditions. In order to provide soft switching conditions, the phase difference between the output voltage and the resonant input current should be zero. To control the phase angle and to accomplish the PLL concept, the mathematical model described in [17], [18] is applied to a parallel resonant inverter. Output voltage and MOSFET gate signal are used as reference and compared with an XOR gate. The error in the phase difference is defined as

$$e(k) = x_f(k) - 1/2, \tag{7}$$

where x_f is the average value of the filtered output of the XOR gate. In steady state x_f can be expressed as a function of φ

$$x_{f,ss} = \varphi / \pi = u_f, \tag{8}$$

where u_f is the average value of the filter input by using low pass filter. According to passive low pass filter circuit x_f is related to u_f and filter components, state equations can be derived as

$$\frac{dx_f}{dt} = -\frac{1}{\tau_f} x_f + \frac{1}{\tau_f} u_f. \tag{9}$$

In the equation $\tau_f = RC$ is the time constant of the low pass filter. u_f is a function of the phase difference φ and the switching period (T) of the resonant input current. Considering the steady state operation of the resonant load in the inverter, the following relationship can be obtained between φ and T

$$\varphi(T) = \tan^{-1}\left(RC\frac{2\pi}{T} / 1 - \left(\frac{2\pi}{\omega_r T}\right)^2 \right). \tag{10}$$

In (10) it is assumed that the load voltage is nearly sinusoidal. Equation (9) can be discretized as follows:

$$x_f(k+1) = a\,x_f(k) + b\frac{\varphi(T(k))}{\pi}, \tag{11}$$

$$a = e^{\frac{-T}{\tau_f}}, \Rightarrow b = (1-a). \tag{12}$$

Equation (13) gives the new operation period

$$T(k+1) = T(k) + K_c e(k+1), \tag{13}$$

where K_c is the integral gain and according to [17] its range can be calculated by Jury's stability test as follows

$$0 < K_c < \left(\frac{1+a}{1-a}\right) 2\pi^2 RC. \tag{14}$$

B. DSP Control Unit for Parallel Resonant Inverter

The block diagram of the overall system is shown in Fig. 3. DSP control unit consists of discrete time integrator (DTI), voltage controlled oscillator (VCO), XOR logic gate, low pass filter (LPF), adder, sample and hold unit (S/H), logic invert gate and zero cross detector (ZCD). This DSP control unit can be implemented by TMS28F335.

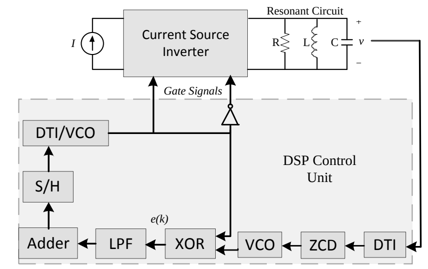


Fig. 3. Block diagram of DSP controlled parallel resonant inverter.

The output voltage of the inverter is detected and discretized. The MOSFET gate signal is compared with the output voltage and phase difference between two signals is detected with XOR. The logic output is filtered to dc value by low pass filter. The phase difference error is discretized and new period is calculated. The new MOSFET drive signal is generated with the VCO. As a result, the inverter tracks the resonant frequency.

IV. SIMULINK MODEL OF DSP CONTROL UNIT

MATLAB/Simulink model of DSP based PLL control algorithm is shown in Fig 4.

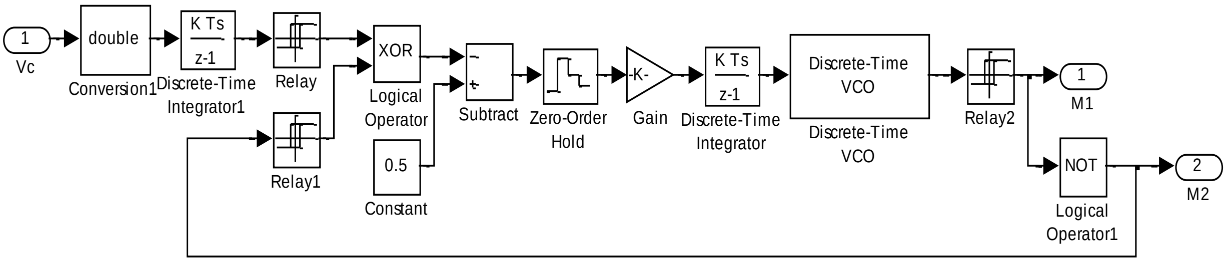


Fig. 4. MATLAB/Simulink model of the closed-loop PLL unit (PLL Block).

Figure 5 shows the simulation circuit of the parallel resonant inverter with PLL block. The output voltage is detected with a voltage sensor and applied to the PLL unit. The initial frequency (f_i) of the system is selected at a suitable value.

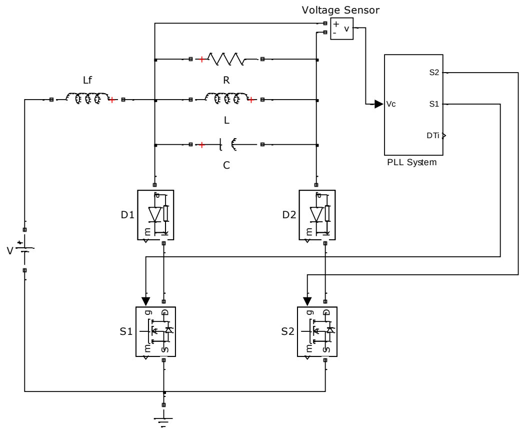


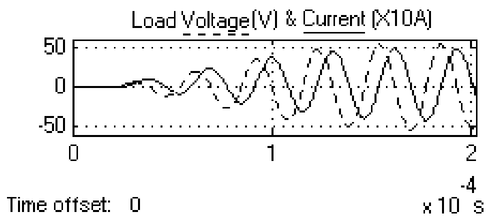
Fig. 5. The parallel resonant inverter circuit and PLL block.

To test the validity of DSP based PLL controller in parallel resonant inverter, two different load parameters are simulated in MATLAB/Simulink. Simulated system parameters are given in Table I.

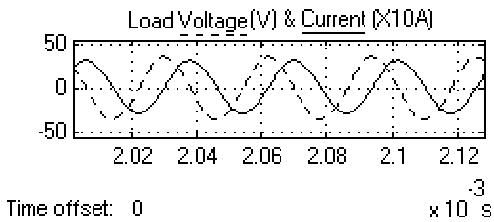
TABLE I. SYSTEM PARAMETERS.

Load	R(Ω)	L(μH)	C(μF)	$L_f(\mu H)$	V(V)	f_i (kHz)
Load A	150	60	0.44	600	12	33
Load B	300	60	0.22	600	12	33

Figure 6 shows the Simulink simulation results of the load voltage and current waveforms for start-up and steady state for Load A (K_c = 20 μs).



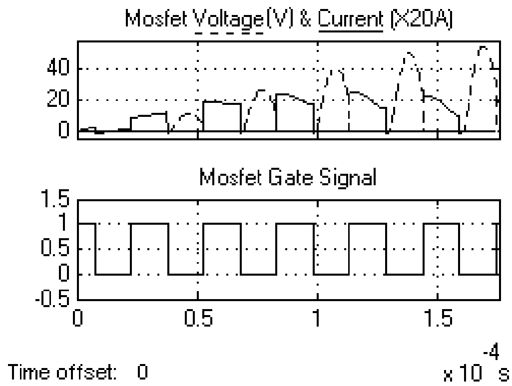
(a)



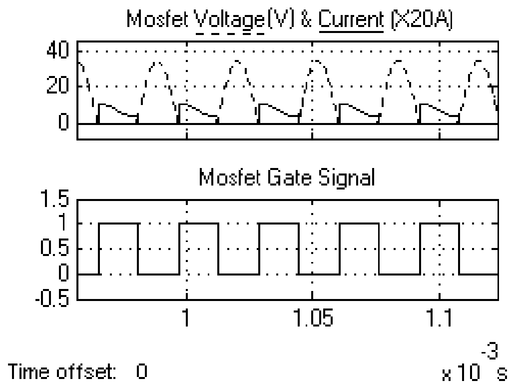
(b)

Fig. 6. Load voltage and current waveforms for Load A: (a) – start-up; (b) – at resonance.

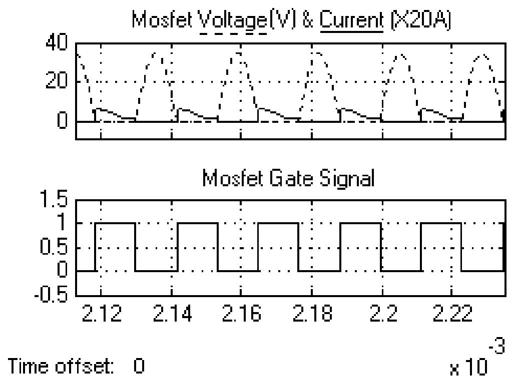
MOSFET gate signals, MOSFET voltage and current simulation results for Load A and Load B are shown in Fig. 7 (K_c = 20 μs). ZVS is achieved when the switch frequency is locked to the resonant frequency.



(a)



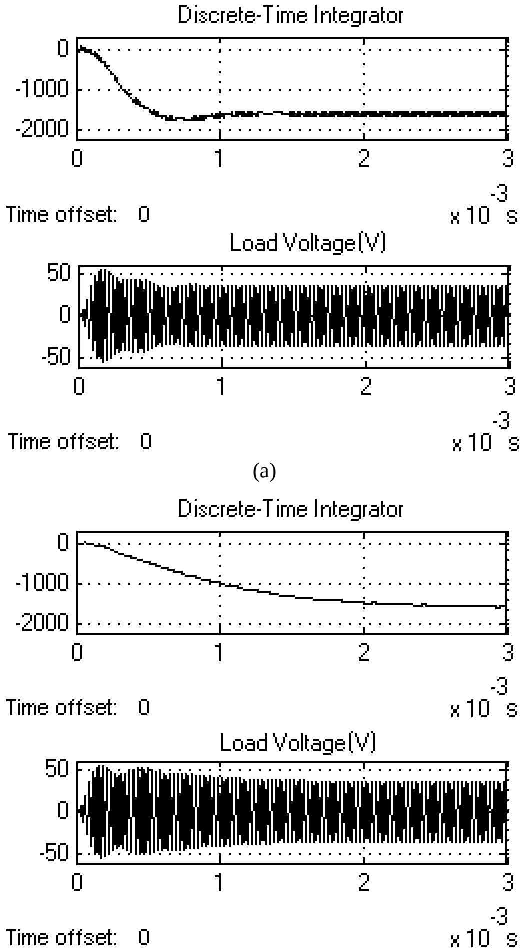
(b)



(c)

Fig. 7. Voltage and current(x20) waveforms of the MOSFET: (a) – start-up (Load A);)b) – at resonance (ZVS) (Load A), (c) – at resonance (ZVS) (Load B).

Discrete time integrator output and the output voltage waveforms for different K_c values are given in Fig. 8 (for Load A).



(b)

Fig. 8. The discrete-time integrator output and the output voltage waveforms: (a) – K_c = 20 µs; (b) – K_c = 5 µs.

As shown in the figures, ZVS is achieved for different loads and integration gains. Comparison of the calculated and the simulated results for the parallel resonant inverter is given in Table II.

TABLE II. CALCULATED AND SIMULATED RESULT.

Parameters		**Calculated**	**Simulated**
Load A	V_{max} (V)	37.68	35.65
	f (kHz)	30.975	31.025
	φ (°)	0	2.3
Load B	V_{max} (V)	37.68	35.75
	f (kHz)	43.806	43.975
	φ (°)	0	7.9

V. CONCLUSIONS

In this paper a DSP based PLL control algorithm is applied to a parallel resonant inverter. A MATLAB/Simulink model of the current source inverter and PLL unit is set and simulation results for different load conditions are compared. According to the simulation results, the designed PLL algorithm for the parallel resonant inverter tracks the resonant frequency perfectly for different quality factors and resonant parameters. The system performance is tested for different DTI parameters. The PLL controlled parallel resonant inverter tracks the changes in the phase difference between the output signal and the inverter current and achieves ZVS automatically. The simulation results show that the DSP controlled system is steady, for the integration gains (K_c) between 0 and 36 µs.

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