New Current-Mode Class 1 Frequency-Agile Filter for Multi Protocol GPS Application

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***Abstract*—Recently, due to their cost, accuracy, and integrability of conventional current-mode (CM) on-chip integrated filters working in radio frequency region, frequency-agile filters (FAFs) have started taking great interest in multi-standard transceivers, encrypted communication, cognitive radio, software defined radio structures, and global positioning system applications. By following the most recent trend in the literature, this paper proposes the first class 1 CM FAF using high-performance analog building block so-called positive-type electronically controllable second-generation current conveyor (ECCII+), two resistors, and two grounded capacitors. The theory and the proposed 2nd-order CM FAF are supported by both regular and post-layout simulations performed using CADENCE Spectre tool with TSMC 0.18 µm level-49 CMOS technology process BSIM3v3 parameters. Furthermore, corner and Monte-Carlo analyses are given to prove the accuracy of centre frequency of the CM FAF.**

***Index Terms*—Analog electronics, active filter, current conveyor, ECCII, frequency-agile filter (FAF), tunable circuit, post-layout simulation.**

I. INTRODUCTION

Electronically tunable filters play important role in several industrial applications. Usually, the centre frequency of tunable filters is changed to compensate the drifts (thermal, technological, etc.) [1]. If the variation of centre frequency is expected to be carried out over a very wide frequency range, reconfigurable filters can be used for compensation. Recently introduced frequency-agile filters (FAFs) by Fabre *et al.* are special type of reconfigurable filters that have property for agility, i.e. during the transmission of the signal in order not to disturb the signal processing the hop between two consecutive frequencies are able to be carried out very quickly [2]–[4]. In general, class *n* FAFs can be designed by using standard implementation schemes [2]. The main application areas of FAFs are multi-standard transceivers (MST), encrypted communication, cognitive radio, software defined radio structures, and global positioning systems (GPSs). It is well-known that sub-blocks of MSTs are low-noise amplifier (LNA), mixer, reconfigurable or adjustable filter, and analog-to-digital converter. Integrated circuit realization of reconfigurable LNAs is not easy to provide even nowadays. Also, RF filters are not easy to reconfigure in integrated form. In transceiver systems, design of reconfigurable structures can be over cost. Similarly, in GPS systems for positioning of different continents, discrete filter structures could be used. Their size, price, complexity and power consumption can be reduced by on-chip integration of FAF. Moreover, architectures' parameters can be still modified in order to be able to adapt to the specifications of different protocols and standards [5]–[7]. Only limited number of FAF topologies using active building blocks (ABBs) working in current-mode (CM) exist in open literature [2], [8]–[10]. It is known that CM circuits show some advantages against voltage-mode circuits such as inherent wider bandwidth, simpler circuitry, lower power consumption, and wider dynamic range [11]. In [2], the intrinsic input resistance R_x of current-controlled second-generation current conveyor (CCCII) is with advantage used for centre frequency hoping in wide frequency range of class 1 and class 2 band-pass filters. In [8], in order to obtain a CM class 1 FAF, the basic class 0 filter employing two current differencing transconductance amplifiers (CDTAs) and two capacitors is extended with electronically controllable second-generation current conveyor (ECCII) functions as amplifier *A*. In CDTA-based class 1 FAF [9], the g_m sub-block of the 2nd CDTA is used for frequency hoping while in [10] additional operational transconductance amplifiers are used as amplifier sub-circuits. Moreover, reference [10] also introduces both class 1 and class 2 FAFs employing recently introduced voltage differencing transconductance amplifiers (VDTAs) [12], [13].

By following the most recent trend in the literature, the main aim of this paper is to present a new CM class 1 FAF using four ECCII+s, two resistors, and two grounded capacitors. The performance of the FAF structure was analyzed using both regular and post-layout simulations in CADENCE Spectre tool. Usually, in integrated filters a

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deviation on the designed filters' centre frequency is significant [14]. In order to prove its accuracy, corner and Monte Carlo (MC) analyses have been also performed.

II. CIRCUIT DESCRIPTION

A. Description of FAF and Implementation Schemes

A FAF is such reconfigurable filter, which has the property of agility, i.e. in order to not disturb the signal processing during the transmission of the signal, the hop between two consecutive frequencies f_1 and f_2 must be able to be carried out very quickly [2]–[4]. Its implementation is based on such classical 2nd-order frequency filter structure, which provides at least band-pass and low-pass responses as it is depicted in Fig. 1. In theory, this 2nd-order filter is called as class 0 FAF and the transfer functions $F_{BP0}(s)$ and $F_{LP0}(s)$ can be expressed as:

$$F_{BP0}(s)=\frac{I_{BP0}}{I_{IN}}=\frac{a's}{1+as+bs^2}, \quad (1)$$

$$F_{LP0}(s)=\frac{I_{LP0}}{I_{IN}}=\frac{d's}{1+as+bs^2}, \quad (2)$$

where a and b are real positive constants to ensure stability of the filter and a' and d' are real positive constants that allow to determine the characteristic parameters of the filter.

Class 1 FAF given in Fig. 2 can be obtained from basic 2nd-order filter by amplifying the low-pass output current I_{LP0} by adjustable gain A, which is added to the input current I_{IN} of previous circuit. Now the new input current of the filter is I_E, which is given by the formula $I_E = I_{IN} - A \cdot I_{LP0}$. The output I_{BP1} remains band-pass response and its corresponding transfer function $F_{BP1}(s)$ is

$$F_{BP1}(s)=\frac{I_{BP1}}{I_E}=\frac{\frac{a's}{(1-Ad')}}{1+\frac{as}{(1-Ad')}+\frac{bs^2}{(1-Ad')}}. \quad (3)$$

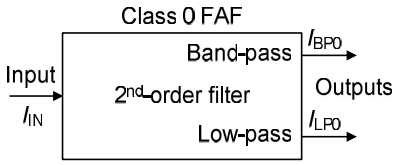

Fig. 1. Basic 2nd-order CM filter providing two different outputs.

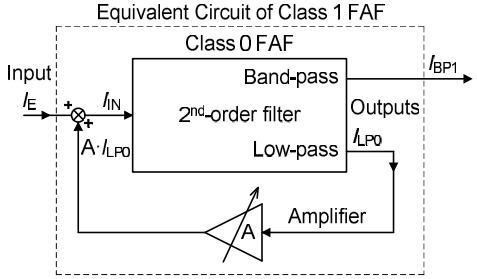

Fig. 2. Class 1 FAF made from the basic 2nd-order filter shown in Fig. 1.

Relationships between the characteristic parameters of both class 0 and class 1 FAFs are listed in Table I. Note that for basic filter (class 0 FAF), the gains of both outputs will be greater than or equal to unity, i.e. $a' \geq a$ and $d' \geq 1$. It can be also observed that once the parameters of the starting filters are set, the f_{0A} of the class 1 FAF can be modified only by the value of gain A of the amplifier. In addition, class 1 FAF will be stable provided that $1 - Ad'$ remains positive.

TABLE I. PARAMETERS OF CLASS 0 AND CLASS 1 FAFS.

	Class 0 FAF	**Class 1 FAF**
Centre frequency	$f_0=\frac{1}{2\pi\sqrt{b}}$	$f_{0A}=f_0\sqrt{(1-Ad')}$
Q-factor	$Q=\frac{\sqrt{b}}{a}$	$Q_A=Q\sqrt{(1-Ad')}$
BP gain	$G_{BP0}=\frac{a'}{a}$	$G_{BPA}=G_{BP0}$
BP: –3 dB bandwidth	$\Delta f=\frac{a}{2\pi b}$	$\Delta f_A=\Delta f$
LP gain	$G_{LP0}=d'$	–

B. Description of ECCII+

The ECCII+ is a four-terminal ABB, which circuit symbol and model are shown in Fig. 3 [15], [16]. Using standard notation, the relationships between its port currents and voltages can be described by the following set of equations:

$$i_Y = 0, \quad (4)$$

$$v_X = v_Y, \quad (5)$$

$$i_Z = k \times i_X. \quad (6)$$

From (4)–(6) and the circuit model in Fig. 3(b) it can be seen that the ECCII+ has a high-impedance (ideally ∞) voltage input terminal Y, a low-impedance (ideally 0) current input terminal X, and a high-impedance (ideally ∞) current output terminal Z. Note that the current gain between X and Z terminals can be made tunable by the coefficient k, which property makes the ECCII+ attractive ABB for CM FAF design.

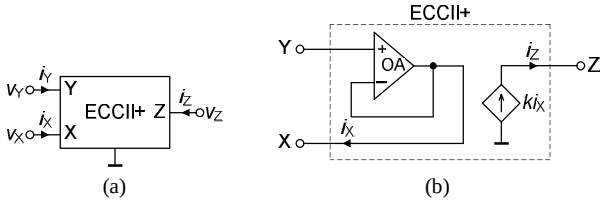

Fig. 3. Circuit symbol (a), model of ECCII+ (b).

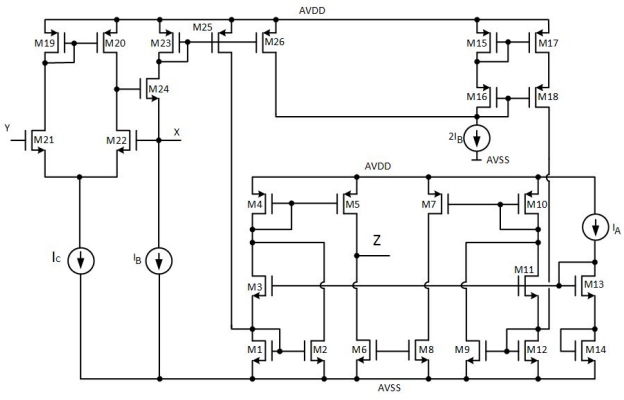

Fig. 4. CMOS ECCII+ internal structure [15].

The CMOS implementation of the ECCII+ is shown in Fig. 4 [15], where transistors M_{19}–M_{22} and current source I_C form a voltage follower stage, which forces the voltage at port X to follow the voltage at port Y, i.e. $v_X \cong v_Y$. Transistor M_{24} functions as a current follower stage and also provides a low output resistance at port X. Both stages together can be considered as a grounded voltage-to-current (V/I) converter. For precision V/I conversion we have assumed that the pairs of transistors M_{21} and M_{22}, M_{22} and M_{24}, M_{15} and M_{17}, M_{16} and M_{18}, and M_{23}, M_{25}, and M_{26} are well matched, the current mirrors have a unity gain, and all transistors operate in saturation region. The current at the port Y is zero, i.e. $i_Y \cong 0$, because the input impedance of the MOSFET is very high. Remaining group of transistors M_1-M_{14} form the output current amplifier stage, which provides current gain tunability between X and Z terminals by using current sources I_A and I_B and the output current i_Z can be calculated as

$$i_Z = n\left(\frac{I_B}{2I_A}\right)\times i_X = k\times i_X, \tag{7}$$

where k is the small-signal current gain of the amplifier stage and it can be controlled electronically by means of dc bias currents I_A and I_B. Note that the parameter n (current multiplication factor of the current mirrors) can be used to increase the dynamic range of the current gain k to the maximum value $k \le 2n$.

The input/output terminal resistances of the CMOS ECCII+ shown in Fig. 4 can be found as:

$$R_X \simeq \frac{(g_{m21}+g_{m22})(g_{d20}+g_{d22})}{g_{m21}g_{m22}g_{m24}}, \tag{8}$$

$$R_Y \simeq \infty, \tag{9}$$

$$R_Z \simeq \frac{1}{g_{d5}+g_{d6}}, \tag{10}$$

where g_{di} and g_{mi} denote the drain transconductance and transconductance of the i-th CMOS transistor, respectively.

C. Proposed ECCII+ Based CM FAF

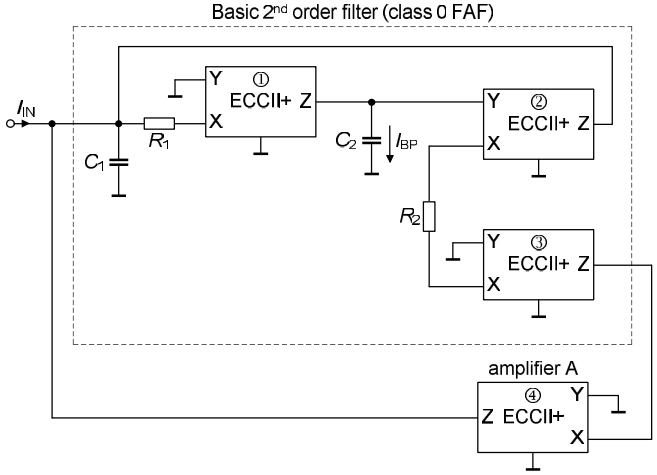

Fig. 5. Proposed frequency-agile filter structure with ECCII+s.

For CM class 1 FAF design the basic 2nd-order dual output filter structure in [16] was used. The proposed new filter employing four ECCII+, two resistors, and two capacitors is shown in Fig. 5. In the feedback path the [4]ECCII+ with tunable coefficient k_4 functions as an amplifier with tunable gain A. Note that this filter corresponds to the case of negative value of A. Assuming $k_1 = k_2 = k_3 = 1$ and $k_4 = A$, routine analysis of the circuit gives the following band-pass transfer function $F_{BP1}(s)$

$$F_{BP1}(s) = \frac{I_{BP}}{I_{IN}} = \frac{\dfrac{sC_2R_2}{(1-A)}}{1+\dfrac{sC_2R_2}{(1-A)}+\dfrac{s^2C_1C_2R_1R_2}{(1-A)}}. \tag{11}$$

The gain G_{BPA} at f_{0A} of this band-pass response is unity and the centre frequency (f_{0A}) and quality factor (Q_A) of the filter are:

$$f_{0A} = \frac{1}{2®}\sqrt{\frac{1}{C_1C_2R_1R_2}}\sqrt{(1-A)}, \tag{12}$$

$$Q_A = \sqrt{\frac{C_1R_1}{C_2R_2}}\sqrt{(1-A)}, \tag{13}$$

which by choosing the capacitors C_1 and C_2 and resistors R_1 and R_2 identical, i.e. $C_1 = C_2 = C$, $R_1 = R_2 = R$, simplify to

$$f_{0A} = \frac{1}{2®CR}\sqrt{(1-A)}, \tag{14}$$

and

$$Q_A = \sqrt{(1-A)}. \tag{15}$$

As it can be above seen both the f_{0A} and Q_A change simultaneously by the gain A.

III. Simulation Results

To verify the theoretical study, the behaviour of the ECCII+ and the new CM 2nd-order band-pass class 1 FAF shown in Fig. 4 and Fig. 5 have been verified in CADENCE Spectre design environment with dc power supply voltages equal to $AV_{DD} = -AV_{SS} = 0.9$ V and bias currents $I_A = 37$ μA, $I_B = 20$ μA, and $I_C = 10$ μA. In the design, transistors were modelled by the TSMC 0.18 μm level-49 CMOS technology process BSIM3v3 parameters. In the CMOS ECCII+ structure all transistors‘ aspect ratio were examined according to dc operating conditions and were selected equally $W/L = 24$ μm/0.36 μm.

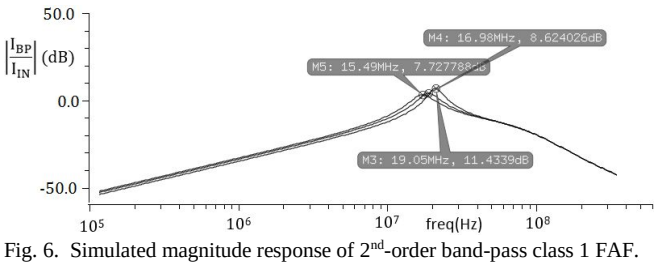

Fig. 6. Simulated magnitude response of 2nd-order band-pass class 1 FAF.

First of all, the performance of the ECCII+ was tested by AC analysis and the maximum operating frequency of the

ECCII+ was found $f_{max} \approx 224$ MHz. Secondly, the performance of the proposed new CM 2nd-order band-pass class 1 FAF was verified. In the structure the passive component values were selected as $C_1 = C_2 = 5$ pF and $R_1 = R_2 = 1$ kΩ. Figure 6 shows simulated magnitude response of proposed class 1 FAF. The centre frequency is varied for $f_{0A} \cong \{19.05; 16.98; 15.49\}$ MHz for bias currents $I_A = \{65; 85; 95\}$ µA, respectively.

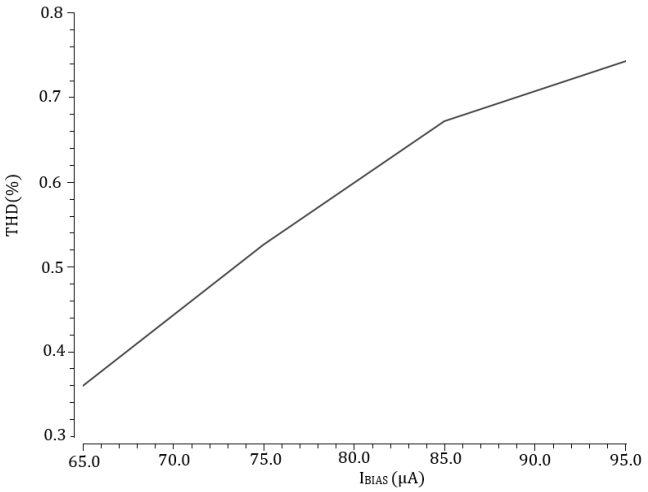

Fig. 7. THD characteristics of band-pass class 1 FAF.

The total harmonic distortion (THD) for the proposed FAF is shown in Fig. 7. During simulations a sinusoidal current input signal with 20 MHz frequency was applied to the FAF while the input current amplitude was changed between 65 µA to 95 µA. The THD values 0.36 %–0.75 % were obtained with connecting 2 kΩ resistive load to the output.

In order to prove the accuracy of centre frequency f_{0A}, corner and Monte Carlo analyses have been performed. During designing CMOS circuits it is useful to consider conditions of process, voltage, and temperature. In general, process variations can be taken into account since a PMOS is not as fast as a NMOS or vice versa. In corner analysis, this is given as SS, SF, FS, FF (slow-slow, slow-fast, etc.) and/or TT (typical-typical). Also supply voltage variation may occur during operation. Last of all, it is clear that performance can change with temperature. Therefore, the circuits are simulated for performance across the "corner points" of process, voltage, and temperature to validate the circuit operates under all performance conditions. The proposed FAF has also undergone MC analysis with setting biasing current $I_A = 65$ µA, because for this value was achieved the maximum f_{0A}. In corner analysis, the even corners SS, FF, and TT have been considered and positive/negative supply voltage values and the temperature were respectively set ±{0.81 to 0.99} V and {–50 to +120}°C. Obtained simulation results are given in Fig. 8. In order to find mean value and standard deviation of centre frequency, the MC analysis histogram is given in Fig. 9. The mean value of f_{0A} is found as 17.4635 MHz and standard deviation 3.89745 MHz, which is close to the f_{0A} of the designed FAF.

In addition, the performance of the proposed CM 2nd-order class 1 FAF was verified by post-layout simulations in CADENCE Spectre tool. The layout of the ECCII+ from Fig. 4 is shown in Fig. 10. Its total area is 1582.22 µm^2.

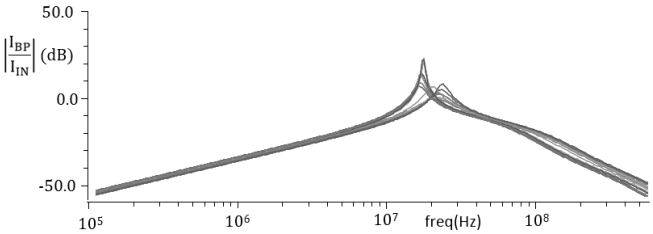

Fig. 8. Corner analysis results of band-pass class 1 FAF.

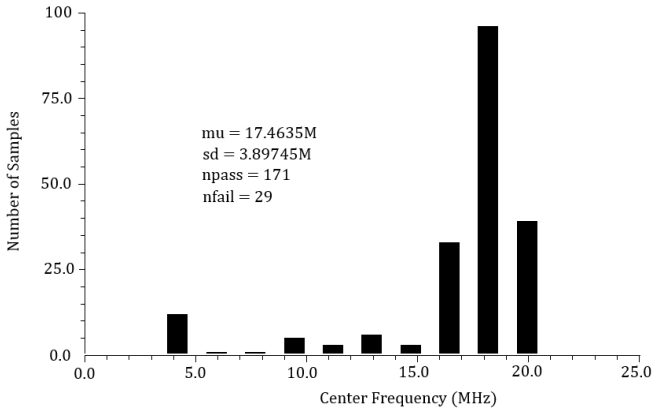

Fig. 9. Monte Carlo analysis histogram of designed band-pass class 1 FAF.

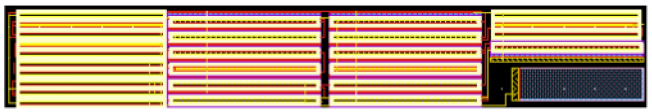

Fig. 10. The layout of ECCII+ circuit structure.

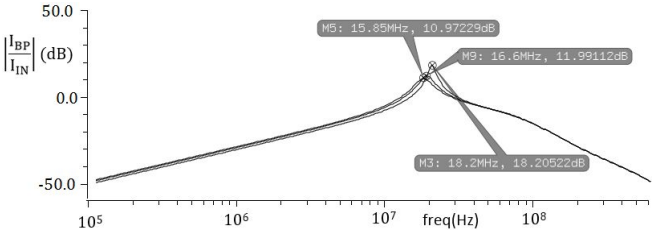

Fig. 11. Post-layout magnitude simulations of band-pass class 1 FAF.

In post-layout simulations of the 2nd-order band-pass class 1 FAF the centre frequency is varied for $f_{0A} \cong \{18.2; 16.6; 15.85\}$ MHz for bias current $I_A = \{65; 85; 95\}$ µA, respectively, and simulated magnitude responses are shown Fig. 11. It can be pointed out that due to layout parasitics there is no significant difference between regular and post-layout simulation responses.

IV. CONCLUSIONS

In order to increase the application possibilities of ECCII+, this paper presents a new CM 2nd-order band-pass class 1 FAF. Compared to basic 2nd-order band-pass filter initially designed for $f_0 = 450$ kHz [16], the f_{0A} of the new FAF is hoping over more than one decade higher – up to 19.05 MHz or 18.2 MHz in regular or post-layout simulations, respectively. In post-layout simulations with setting maximum biasing current I_A the total power dissipation of FAF was determined as 8.17 mW.

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