Design and Applications of Electronically Tunable Floating Resistor Using Differential Amplifier

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***Abstract*—In this paper, a new electronically tunable active resistance was introduced. The proposed circuit design consists of only two differential amplifiers. The main advantages of this circuit are higher bandwidth, simpler design and tunable resistance range. Also, the design of the circuit allows negative resistance structure and besides it can be used in IC realizations. Effective range of the floating resistor is controlled within a wide range of resistance in between ± 43 Ω – ± 516 kΩ.**

***Index Terms*—Active resistor, current amplifier, current mode circuits, differential amplifier.**

I. INTRODUCTION

The floating and grounded resistors in technology of silicon can be realized by using diffusion areas or polysilicon in an integrated circuit. Nevertheless, large areas of silicon chip are required to obtain these resistors. This technique is inconvenient to attain certain values. Also, it is not possible to tune the targeted values of resistance. So MOS and bipolar based active resistors have been introduced in previous studies to overcome these limitations [1].

The diverse analogue circuits, for example, filters, oscillators and amplifiers, are necessary for high performance electronically controllable active resistors. [2]–[5]. Several CMOS circuits simulating controlled resistors have been proposed in the literature [6]–[8]. Electronically tunable resistors which process in MOS technologies have been introduced. However, these resistors are not able to operate at high frequencies [9], [10]. In addition, the only voltage signal is used to drive these circuits. Thus, the ability of these circuits is limited and these circuits exhibit severe frequency limitations, essentially when low values of the simulated resistances are needed. This is due to the gate-drain and gate-source parasitic capacitances of the MOS transistors [11]. Also, the tuning ranges of the resistor which designed in MOS transistors are narrow [6], [12].

Some circuit applications used in general impedance converters (GICs) have the significant advantages of the achieving resistors by easily changing the feedback connections in the circuits. Passive components are usually used for designing GIC circuits. However, using passive device is not proper and impractical for integrated circuit implementations [13], [14].

A bipolar based floating controlled resistance has also been described in the literature [15], [16]. Also, it is introduced voltage controlled floating resistor using OTA in previous study [17]. But these studies suffer from narrow bandwidth and circuit complexity. Bipolar based current-controlled resistance is proposed in this paper as a way to avoid these problems.

Recently, some differential amplifier based circuits have been proposed in the literature [18]–[20]. It is introduced a floating resistance based on a pair of differential amplifier has the ability to operate at high frequencies in this paper. This resistor, which merely contains bipolar transistors, is very convenient for IC implementation. More components are not utilized in the circuit with the aim of keeping the low circuit complexity and the simpler design.

In this article, first, theoretical analysis for a differential amplifier is explained. Thereafter, circuit analysis and simulation results of the tunable floating resistor design are demonstrated. Finally, the suitability of this floating resistor is indicated using oscillator and current amplifier.

II. CIRCUIT DESCRIPTION

In this section, in order to carry out a simple circuit definition of the tunable active resistance as shown in Fig. 1, a basic differential amplifier is employed.

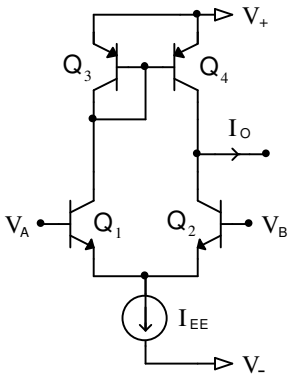

Fig. 1. Transconductance amplifier.

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Transistors Q_1 and Q_2 convert input voltages to an output current as a transconductance amplifier. Q_3 and Q_4 act as a current mirror where I_{EE} is an input biasing current. Assuming that V_A and V_B are applied from base of transistors Q_1 and Q_2, respectively, the difference between input voltages V_A and V_B of the transconductance amplifier is given by

$$V_A - V_B = V_{BE1} - V_{BE2} = V_T\left(\ln\frac{I_{C1}}{I_S} - \ln\frac{I_{C2}}{I_S}\right), \quad (1)$$

where V_{BE} is the junction voltage of the transistors. As shown in Fig. 1, I_{C1} and I_{C2} are the collector currents of the Q_1 and Q_2 transistors, respectively. Also, V_T is the thermal voltage and I_S is the reverse saturation current of the transistors.

In this case, collector currents can be written as following equations

$$\begin{cases} I_{EE} \cong I_{C1} + I_{C2}, \\ I_{C1} = \dfrac{I_{EE}}{1 + e^{\frac{-(V_A - V_B)}{V_T}}}, \\ I_{C2} = \dfrac{I_{EE}}{1 + e^{\frac{V_A - V_B}{V_T}}}. \end{cases} \quad (2)$$

The relation of I_0 and input voltages of the transconductance amplifier can be expressed as

$$I_0 = I_{C1} - I_{C2} = I_{EE}\, tanh\left(\frac{V_A - V_B}{2V_T}\right). \quad (3)$$

From (3), if $V_A - V_B << 2V_T$ is assumed, then the function $tanh[(V_A - V_B)/2V_T]$ is approximately equal to $(V_A - V_B)/2V_T$. The expression of this output current is

$$I_0 = I_{EE}\frac{V_A - V_B}{2V_T} \quad (4)$$

or

$$I_0 = G_m(V_A - V_B), \quad (5)$$

where transconductance $G_m = I_{EE}/2V_T$. Considering the small signal analysis of transconductance amplifier, the output current can be given by

$$i_o = v_A \cdot \left(\frac{g_{m4} \cdot g_{m1}}{g_{m3}}\right) - v_B \cdot g_{m2}. \quad (6)$$

Since all transistors are operating at the same bias current, $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m$, where

$$i_o = g_m(v_A - v_B). \quad (7)$$

Thus, from (5) and (7) it can be seen that

$$G_m = g_m, \quad (8)$$

which is identical to the result found for the amplifier pair.

Fig. 2 shows schematic diagram for the proposed floating positive resistor. The proposed circuit consists of two matched amplifier pairs composed of $Q_{1A} - Q_{2A}$ and $Q_{1B} - Q_{2B}$, respectively. The residual transistors are used as current mirrors. In order to inject copies of the biasing current into the transistors ($Q_{3A} - Q_{4A}$) and ($Q_{3B} - Q_{4B}$), these current mirrors are essential. The circuit is obtained by a parallel connection of the two transconductance amplifiers.

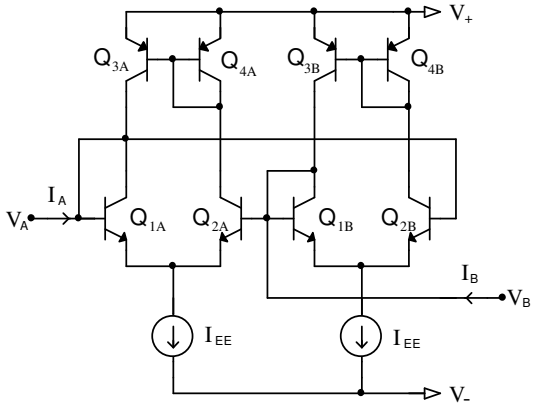


Fig. 2. Floating positive resistor.

Assuming that all the transistors are matched, an analysis of the circuit indicates that the currents I_A and I_B are written as

$$I_A = -I_B = G_m(V_A - V_B), \quad (9)$$

The resistance can now be found as

$$R_{AB} = \frac{V_A - V_B}{I_A} = \frac{2V_T}{I_{EE}}, \quad (10)$$

This means that the resistance value of the positive resistor will be tuned easily by bias current.

Fig. 3 shows the schematic diagram for the proposed floating negative resistor.

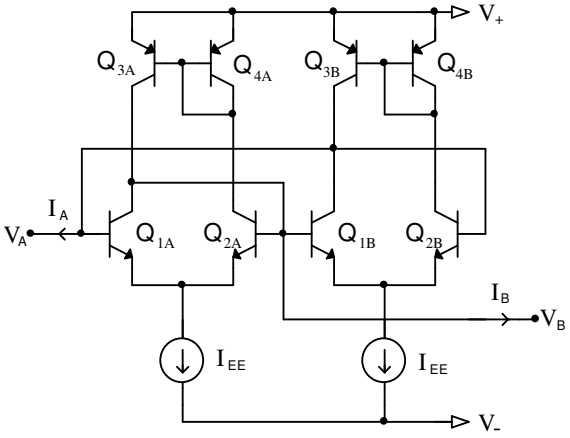


Fig. 3. Floating negative resistor.

The negative resistor structure is the same as positive resistor in terms of having components, but it is used

different connections between components in the circuit as shown in Fig. 3.

Provided that all the transistors are matched, an analysis of the circuit which operates as a negative resistor indicates that the currents I_A and I_B are given by

$$I_B = -I_A = G_m\left(V_A - V_B\right). \tag{11}$$

The resistance can now be found as

$$R_{AB} = \frac{V_A - V_B}{-I_A} = -\frac{2V_T}{I_{EE}}. \tag{12}$$

This means that the negative resistance of the negative resistor will be tuned easily by bias current.

III. Performance Analysis of the Resistor

A. Mismatch of the areas

The mismatch effect of the transconductance amplifier shown in Fig. 1 is defined as an inequality in the base-emitter areas of the transistors Q_1 and Q_2. Such a mismatch between transistors can be given as:

$$\begin{cases} I_{S1} = I_S + \dfrac{\Delta I_S}{2}, \\ I_{S2} = I_S - \dfrac{\Delta I_S}{2}. \end{cases} \tag{13}$$

Eq. (13) is defined as a proportional mismatch in the collector transport saturation current I_S. Thus, the bias current I_{EE} will be splitted between Q_1 and Q_2 transistors in proportion to their I_S values. When voltage V_A and V_B are grounded, collector currents of the transistors can be found as

$$\begin{cases} I_{C1} = \dfrac{I_0}{2}\left(1 + \dfrac{\Delta I_S}{2I_S}\right), \\ I_{C2} = \dfrac{I_0}{2}\left(1 - \dfrac{\Delta I_S}{2I_S}\right). \end{cases} \tag{14}$$

If the condition is V_A - V_B > 0, output current I_0 will be as following equation

$$I_0 = g_m\left(V_A - V_B\right) + \left(\frac{I_{EE}\Delta I_S}{2I_S}\right). \tag{15}$$

For resistor, input current I_{AB} (I_A) can be written as

$$I_{AB} = g_m\left(\mathrm{V_A} - \mathrm{V_B}\right) + \left(\frac{I_{EE}\Delta I_{SA}}{2I_{SA}}\right) - \left(\frac{I_{EE}\Delta I_{SB}}{2I_{SB}}\right), \tag{16}$$

where I_{SA} is the collector transport saturation current of the Q_{1A} and Q_{2A}. Also I_{SB} is the collector transport saturation current of the Q_{1B} and Q_{2B}. From (16), R_{AB} is written as follows

$$R_{AB} = \frac{\left(\mathrm{V_A} - \mathrm{V_B}\right)}{I_{AB}} = \frac{2V_T}{I_{EE}} + \frac{V_T\left(I_{SA}\Delta I_{SB} - I_{SB}\Delta I_{SA}\right)}{I_{SA}I_{SB}I_{AB}}, \tag{17}$$

B. Systematic output offset current

If V_A and V_B are grounded, the current-transfer ratio of a current mirror formed by transistors Q_3 and Q_4 in Fig. 1 can be found as

$$\frac{I_{C4}}{I_{C3}} = \frac{1}{1 + 2/\beta_p}, \tag{18}$$

where I_{C3} and I_{C4} are the collector currents of the transistors Q_3 and Q_4, respectively. Also, β_p is the current gain of the PNP transistors in Fig. 1. Thus, the collector current of Q_4 is given by

$$I_{C4} = \frac{I_{EE}}{2\left(1 + 2/\beta_p\right)}. \tag{19}$$

Eq. (19) defines that output terminal has a current difference. The current difference Δi_o can be expressed as follows

$$\Delta i_0 = I_{C3} - I_{C4} = \frac{I_{EE}}{1 + \beta_p/2}. \tag{20}$$

If the condition is V_A - V_B > 0, output current I_0 can be written

$$I_0 = g_m\left(V_A - V_B\right) - \frac{I_{EE}}{2\left(1 + 2/\beta_p\right)}. \tag{21}$$

Improved current mirror such as MOS current mirror should be used to reduce offset current. Assuming perfect matching of the transistors in MOS current mirror, difference current Δi_o will always be zero. Thus, proposed resistor circuit can be used for BiCMOS applications.

IV. Simulation Results

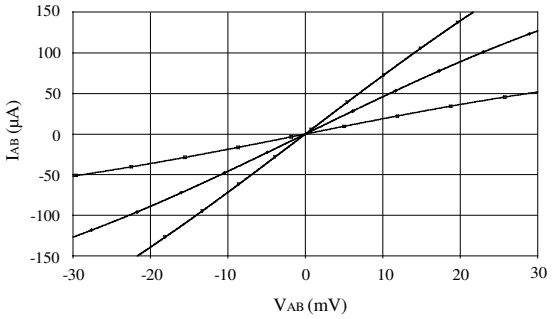
The circuits in Fig. 2 and Fig. 3 were simulated using models for the transistors of the type NR100N and PR100N whose parameters are detailed in [21], in order to demonstrate the availability of the theory. The power supply is ± 1.5 V. The biasing current I_{EE} is changed between 0.1 µA and 10 mA.

I-V characteristics of the positive resistor for different biasing current are shown in Fig. 4.

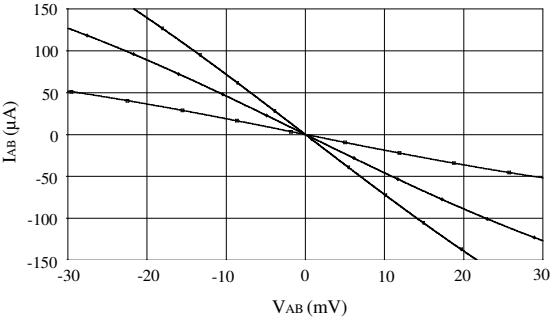
Fig. 4(a) depicts the I-V characteristics of the positive resistor for the diverse values of the I_{EE}. It is openly from the simulation results that the positive resistor can be exhibited reasonable good characteristics.

The I-V characteristics of the negative resistor for different biasing current are shown in Fig. 4(b). This figure displays, for the various values of the I_{EE}, the I-V

characteristics of the negative resistor. Although Fig. 2 and Fig. 3 have different connections, because of having similar structure, it is obvious that the negative resistor can be adjusted within reasonable values.



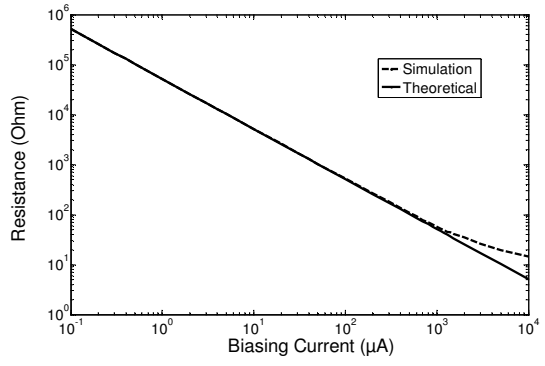
(a)



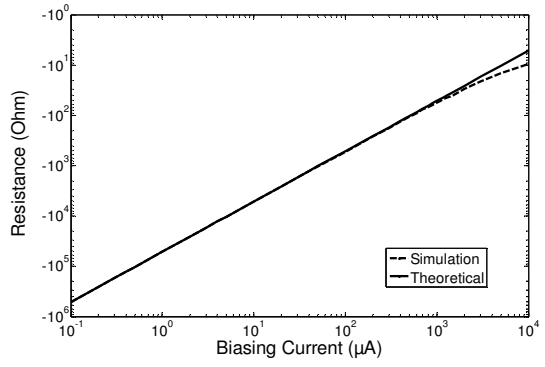
(b)

Fig. 4. I-V characteristics for: (a) positive resistor; (b) negative resistor.

Fig. 5 depicts the resistance R_{AB} at the resistor when I_{EE} is varied.



(a)



(b)

Fig. 5. Variation of the resistance with dc bias current for: (a) positive resistor; (b) negative resistor.

It is shown that the resistance value of the proposed resistor can be varied from ±5.16 Ω to ±516 kΩ with affinity between the theoretical and simulation results in Fig. 5 if bias current is tuned from 0.1 μA to 10 mA. It is seen to be excellent linear behaviour when 0.1 μA ≤ I_{EE} ≤ 1.2 mA. The linear range of the resistor is ± 43 Ω – ± 516 kΩ.

Fig. 6 depicts the changing percent total harmonic distortion (THD) versus peak to peak input current, for both the negative and positive resistor. THD %, which is a function of peak to peak magnitude of the input current, is calculated for R_{AB} = 258 Ω and frequency = 1 MHz. It is shown that the THD % in the voltage across R_{AB} when the peak-to-peak magnitude of the input current I_{AB} is varied from 100 to 500 μA, is found to change from 0.04 % to 0.747 %. It is clear that the THD is within reasonable values.

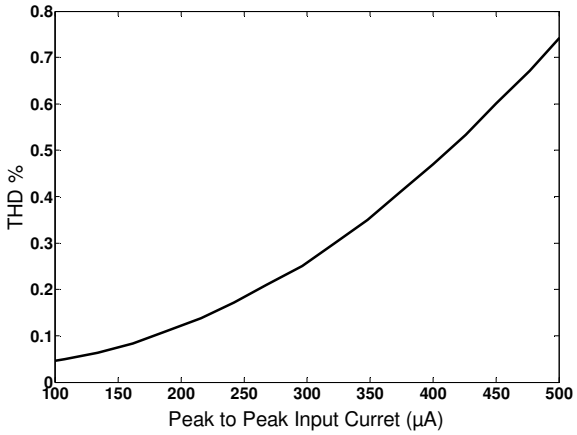


Fig. 6. THD % as a function of input current.

It is displayed the conclusions of the proposed floating resistor parameters in Table I.

TABLE I. PERFORMANCE PARAMETERS OF THE PROPOSED RESISTOR.

Parameters	**Values**
Power supply voltages	*±1.5V*
Power consumption	*0.9 mW*
−3dB Bandwidth positive resistor (V_{AB}/I_{AB}) negative resistor (V_{AB}/I_{AB})	 *66.4 MHz* *70.2 MHz*
R_{AB} ranges	*43Ω–516kΩ*
The bias current range for controlling resistor	*0.1μA–1.2 mA*
THD (for R_{AB}=258Ω and 1Mhz)	*0.747 %*
References	*±1.5V*

The −3dB bandwidths of positive resistor and negative resistor, respectively, are located at the 66.4 and 70.2MHz.

V. APPLICATIONS OF THE PROPOSED RESISTOR

A. Oscillator application

The application of the floating negative resistor is an oscillator, shown in Fig. 7 [1].

It consists of a floating negative resistor, a grounded capacitor and one inductor with loss. The negative resistor is necessary to set the oscillation condition of the circuit. Oscillator output waveform will still exist if the condition

$$|R_{AB}| \le \frac{(\omega_o L)^2}{R} \tag{22}$$

is met. This is known as the Barkhausen criterion for the oscillation.

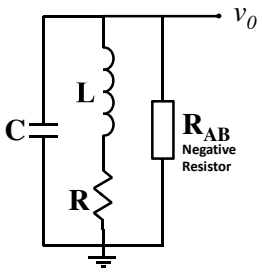


Fig. 7. An oscillator used negative resistor.

The oscillation frequency of this oscillator can be expressed as

$$\omega_o = \frac{1}{\sqrt{LC}}. \tag{23}$$

Fig. 8 shows the verified performance of the oscillator. In order to obtain the frequency responses of the oscillator, *R, L* and *C* are respectively, set to 250 Ω, 0.1 mH and 0.1 nF. Biasing current for negative resistor is 150 µA.

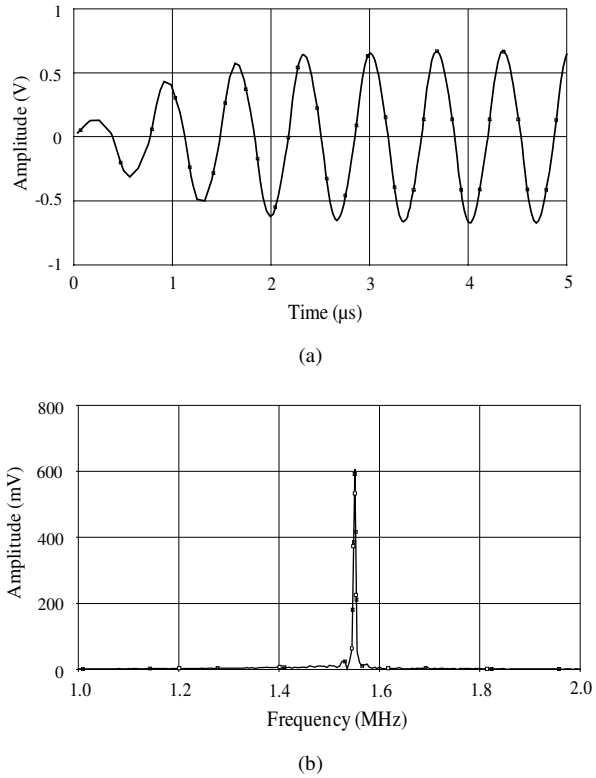


Fig. 8. The simulation results of the voltage waveforms of the oscillator a) in time domain b) in frequency domain .

As shown in Fig. 8, the oscillation frequency of the circuit is 1.5503 MHz which well agrees with the calculated result.

B. Temperature compensated current amplifier

In literature, a temperature compensated scheme for a translinear current conveyor-based circuit was investigated [22]. This scheme has a disadvantage because it has complex circuit structure. Tunable current amplifier which has a simple structure for temperature compensation as an application of the positive resistor is shown in Fig 10. Current amplifier consists of the positive resistor and controlled current conveyor (CCCII).

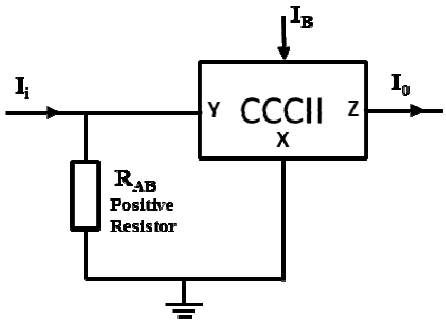


Fig. 9. Temperature compensated current amplifier.

The current I_0 of the port Z is output current for CCCII. Additionally, port *X* of the CCCII is grounded and port *Y* constitutes the input of the circuit (Fig. 9). I_0 is written as follow [23]

$$I_0 = 2I_B \frac{V_Y}{V_T}, \tag{24}$$

where I_B is bias current of the CCCII. Also V_Y is the voltage of the port Y. V_Y can be written as

$$V_Y = R_{AB}.I_i = \frac{2V_T}{I_{EE}} I_i. \tag{25}$$

From (24) and (25), we can see that the current gain of the amplifier will be expressed as

$$A_I = \frac{I_0}{I_i} = 4\frac{I_B}{I_{EE}}. \tag{26}$$

In this instance, the current gain A_I of the circuit can be independent from thermal voltage (V_T).

Fig. 10 depicts the changing current gain versus temperature for the temperature compensated current amplifier.

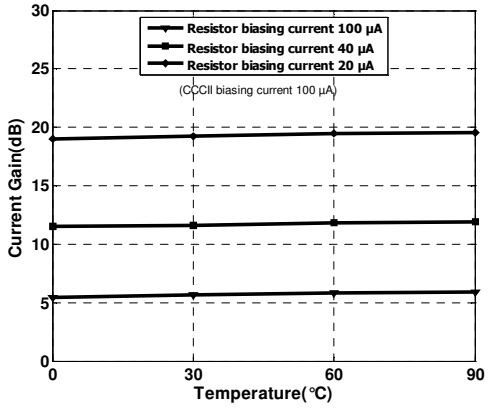


Fig. 10. The current gain of the amplifier for different biasing current of the positive resistor versus temperature.

It is clear that stable current gain is obtained at the different temperature values for the current amplifier. Also, the gain can be easily tuned by bias currents I_{EE} and I_B.

VI. CONCLUSIONS

In this study, electronically tunable active resistor using

differential amplifier circuit was designed, and its applications to an oscillator and a current amplifier were tested. A basic differential pair is used to achieve a simple circuit implementation of the floating active resistor in this design. This circuit is used as either positive resistor or negative resistor by using different connection structures. The proposed resistors were simulated using a PSpice simulation program, and its simulation results were compared with the theoretical approaches. Theoretical analyses of these circuits were achieved, and the performance of the proposed resistors was verified by PSpice simulation results.

For proposed floating resistor, the resistance value can be tuned from ± 43 Ω to ± 516 kΩ, with perfect affinity between the theoretical and simulation results. From the frequency performance in Table 1, it can be seen that the -3 dB bandwidth is enhanced to 66.4 MHz and 70.2 MHz, respectively, for positive resistor and negative resistor. Finally, the adjustment capability of the introduced resistor is useful in electronic circuit designs and the circuit is rather convenient for bipolar and BiCMOS IC realizations.

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