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Direct AC-AC Step-Down Single-Phase Converter with Improved Performances

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***Abstract*—The paper presents two high-performance single-phase AC chopper circuits which perform AC-AC bidirectional direct conversion; one of them contains resistive loads and the other one is for inductive loads. It includes useful equations for chopper design. The correct functioning is tested by simulation.**

***Index Terms*—Choppers, power conversion, circuit simulation.**

I. Introduction

The direct AC-AC converters have applications in various fields, such as AC motor drives, electronic transformers, switching AC adjustable sources, output voltage waveform restorers, etc. The AC-AC step-down converters of high frequency can replace the AC phase control made up of SCR or triacs. For frequencies of more than 20 kHz, these converters eliminate disturbing noise, have smaller filters, the output voltage is less distorted, irrespective of the load nature, the output voltage variation field is large, the efficiency is adequate and the main current can be practically sinusoidal.

In [1] and [2], the authors propose an AC chopper, with improved commutation, which leads to increased efficiency. However, this requires many switching devices and complex control circuits. The possibility of using sliding-mode control for AC-AC resonant converters is analysed in [3]. [4] and [5] present AC choppers with three level converters and [6] suggests several topology versions using commercial power modules for circuit design. In [7] an evaluation methodology for AC choppers is described.

This paper presents a simple circuit of direct AC-AC single-phase buck converter, which allows eliminating downtime in control by an adequate disposition of power switching devices. Moreover, snubber circuits are no longer necessary, the work frequency can be substantially increased (over 20 kHz), the control is simple, the power flux can be bidirectional, the functioning is adequate, irrespective of the load nature, and the efficiency is high. The equivalent circuits are studied in various functioning modes and, thus, we can establish equations which are useful for the design stage. The correct functioning of the proposed circuit was checked by simulation.

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II. The topology of the AC-AC step-down converter

The inductance L and the capacitor C represent the input high-frequency power supply filter, which eliminates the harmonics of the current absorbed from the power supply i_m.

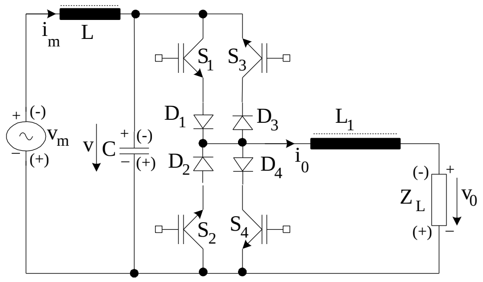

Fig. 1. AC-AC buck converter with one inductance.

In the positive alternations of the current i_o, considering a uniform PWM technique, in the time intervals $[0, DT_S]$, S_1 is in conduction, and in the intervals $[DT_S, T_S]$ S_2 is in conduction, while S_3 and S_4 are blocked through the entire alternation. The frequency $f_S=1/T_S$ is the switching frequency used for chopping the voltage from the power supply. In the negative alternations, S_3 and S_4 are in conduction in the same time intervals, while S_1 and S_2 are blocked throughout these alternations.

The load output voltage is

$$v_o \approx D\cdot v \approx D\cdot v_m ,\ D\in\left(0,1\right). \qquad (1)$$

The circuit is simple and can be used for purely resistive loads; the shift in control between the switch pairs occurs when the voltage V, and therefore the current i_o, passes through zero. There is no need for downtime when the switch pairs shift, since this occurs when voltage and currents are zero. For inductive loads, which change during functioning, it is necessary to introduce a current transducer, which detects when i_o is zero. At that time, it is necessary to shift the switch pairs under control, by using downtime. When the current fundamental i_o passes through zero, in a specific variation range of the duty factor D, the buck converter can function in the discontinuous conduction mode (DCM) and there is an inadequate timing of i_o=0, which determines an inadequate functioning of the AC-AC converter.

In order to eliminate the drawbacks mentioned above, Fig. 2 shows the proposed circuit for the direct AC-AC converter. As compared to Fig. 1, another inductance is added, which allows a new disposition of the switching devices. Thus it is possible to control simultaneously the switch pairs S_1-S_3 and S_2-S_4 and downtime is no longer necessary, as shown in the waveforms in Fig. 3.

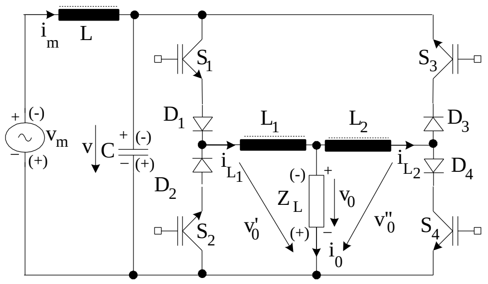

Fig. 2. AC-AC buck converter with two inductances.

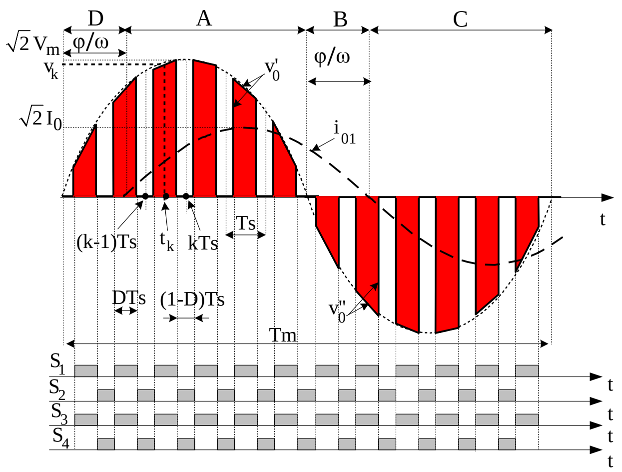

Fig. 3. Voltage and load current waveforms; the generation of the switching devices conduction intervals.

In the positive alternations of the load current, in the time intervals DT_S, i_o will flow through S_1, D_1, L_1, Z_L, and in the intervals $(1\text{-}D)T_S$, it will flow through S_2, D_2, L_1, Z_L. In the negative alternations, in the time intervals DT_S, i_o will flow through Z_L, L_2, D_3, S_3, and in the time intervals $(1\text{-}D)T_S$, it will flow through Z_L, L_2, D_4 and S_4.

The waveform of the current i_o in Fig. 3 corresponds to an inductive load

$$\begin{cases} Z_L = \sqrt{R_L^2 + \left(\omega L_L\right)^2}, \\ tg\,\varphi = \dfrac{\omega L_L}{R_L}, \\ \omega = 2\pi f_m = \dfrac{2\pi}{T_m}, \end{cases} \tag{2}$$

where R_L and L_L are the load resistance and the load inductance, respectively, f_m is the main frequency of the power supply of the AC-AC converter.

Depending on the time intervals, the circuit in Fig. 2 can be in four states (also marked in Fig. 3): a) the main voltage V_m is positive (has the polarity without brakes) and the current i_o is positive (its direction is shown in Fig. 2); b) V_m is negative (it has the polarity between brakes) and the current i_o is positive; c: V_m is negative and i_o is negative; d: V_m is positive and i_o is negative.

III. THE EQUIVALENT CIRCUITS OF THE AC-AC CONVERTER

The equivalent circuits correspond to the following simplified hypotheses: the passive components are ideal, the power devices are ideal switches, the voltage V and the load current i_o are sinusoidal.

Fig. 4 presents the equivalent circuits and waveforms corresponding to A and B states of the converter.

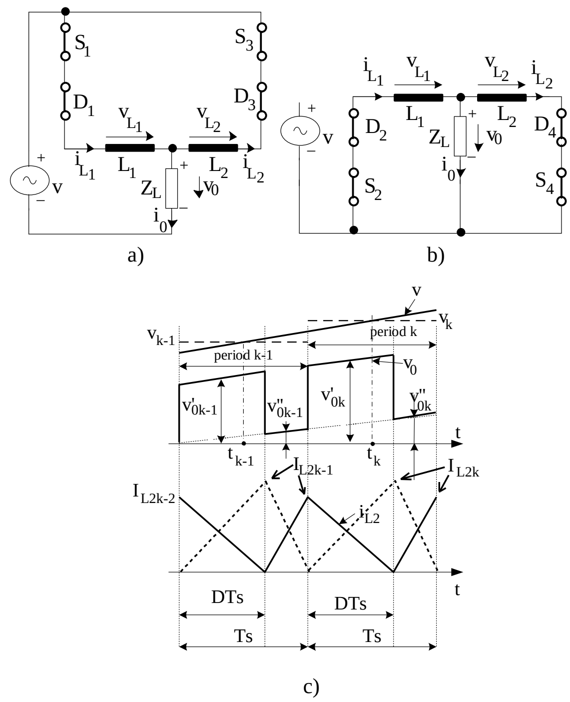

Fig. 4. The equivalent circuits and i_{L2} current corresponding to A and B states: a) the equivalent circuits in the interval DT_S b) the equivalent circuits in the interval $(1\text{-}D)T_S$. c) the waveform of the current through the inductance L_2 corresponding to the A, B states.

The equations related to the circuits are calculated based on the assumption that, in a switching period T_S, the voltage V is constant at the value

$$v_k = \sqrt{2}\cdot V \cdot \sin \omega t_k\,, \tag{3}$$

where $t_k = (k-1)T_s + \dfrac{T_s}{2}$.

For the inductive load, the voltage Vo is chopped (Fig. 4c). In the intervals DT_S and $(1\text{-}D)T_S$, we consider that the output voltages remain constant respectively at the values:

$$v_o = v_{ok}^{'}\,,\ v_o = v_{ok}^{''}\,. \tag{4}$$

If the circuit is in the A state, in the intervals DT_S and $(1\text{-}D)T_S$, the voltage V_{L1} are:

$$v_{L1k}^{'} = v_k - v_{ok}^{'}\,,\ v_{L1k}^{''} = -v_{ok}^{'}\,. \tag{5}$$

Since the average voltage on the inductance L1 is zero:

$$v_{L1k}^{'}\cdot DT_s=-v_{L1k}^{"}\left(1-D\right)T_s\ ,\ v_{L1k}^{"}=-\frac{D}{1-D}v_{L1k}^{'}\ . \tag{6}$$

In order to calculate the i_{L2} current, we first consider Fig. 4(b) in the switching period k-1, corresponding to the intervals (1-D)T_S:

$$v_{L2}=L_2\frac{di_{L2}}{dt}=-v_{L1k-1}^{"}=\frac{D}{1-D}v_{L1k-1}^{'}\ , \tag{7}$$

$$i_{L2}=\frac{D}{1-D}\frac{v_{L1\,k-1}}{L_2}t\ ,\ \ i_{L2}\left(0\right)=0\ . \tag{8}$$

In the final part of the interval (1-D)T_S (Fig. 6), we have

$$t=\left(1-D\right)T_s\ ,\quad i_{L2}=I_{L2k-1}=\frac{Dv_{L1k-1}^{'}}{L_2\ f_s}\ . \tag{9}$$

In the DT_S interval within the switching period K, according to Fig. 4(a):

$$v_{L2}=L_2\frac{di_{L2}}{dt^{'}}=v_{L1k}^{'}\ , \tag{10}$$

$$i_{L2}=I_{L2k-1}-\frac{v_{L1k}^{'}}{L_2}t^{'}=\frac{Dv_{L1k-1}^{'}}{L_2\ f_s}-\frac{v_{L1k}^{'}}{L_2}t^{'} \tag{11}$$

and in the final part of the interval (t’ =DT_S)

$$i_{L2}=\frac{D}{L_2\ f_s}\left(v_{L1k-1}^{'}-v_{L1k}^{'}\right)\approx 0\ . \tag{12}$$

The waveform of the i_{L2} current is shown in Fig. 4(c) in continuous line. Under real functioning conditions, the i_{L2} current becomes 0 before the end of the DT_S interval, even if $v_{L1k}^{'}<v_{L1k-1}^{'}$, because of the losses on the real components of the converter.

If the circuit is in the B state, we have to consider initially Fig. 4a for the calculation of the i_{L2} current. In the DT_S intervals within the K switching period, v and v_o voltages have the polarities indicated between brakes:

$$v_{L2}=L_2\frac{di_{L2}}{dt}=-\left(v_k-v_{ok}^{'}\right)=-v_{L1k}^{'}>0\ , \tag{13}$$

$$i_{L2}=-\frac{v_{L1k}^{'}}{L_2}t\ ,\ \ I_{L2k}=-\frac{Dv_{L1k}^{'}}{L_2\ f_s}\ . \tag{14}$$

In the following interval (1-D)T_S:

$$v_{L2}=L_2\frac{di_{L2}}{dt}=v_{L1k}^{"}=\frac{D}{1-D}v_{L1k}^{'}<0\ , \tag{15}$$

$$i_{L2}=I_{L2k}+\frac{D}{1-D}\frac{v_{L1k}^{'}}{L_2}t^{'}=-\frac{Dv_{L1k}^{'}}{L_2\ f_s}+\frac{D}{1-D}\frac{v_{L1k}^{'}}{L_2}t^{'}\ . \tag{16}$$

In the final part of this interval, t’ = (1-D)T_S, the i_{L2} current is

$$i_{L2}=-\frac{Dv_{L1k}^{'}}{L_2\ f_s}+\frac{Dv_{L1k}^{'}}{L_2\ f_s}=0\ . \tag{17}$$

The waveform of the i_{L2} current in B state is shown in Fig. 4(c) in dotted line.

For converter states C and D, when the load current becomes reverse, these equivalent circuits and equations remain valid, except for the role of inductances L_1 and L_2, which is reversed.

For the resistive load, the voltage V_o is no longer chopped and has the value:

$$\begin{cases} v_o=R_L\,i_o=\sqrt{2}DV\sin\omega t, \\ i_o=\dfrac{D\sqrt{2}V}{R_L}\sin\omega t. \end{cases} \tag{18}$$

The converter will be only in states A and C. In the A state, (5) becomes

$$v_{L1k}^{'}=\sqrt{2}\left(1-D\right)V\sin\omega t_k\ ,\ v_{L1k}^{"}=-\sqrt{2}DV\sin\omega t_k\ . \tag{19}$$

Eq. (9) leads to the following equation for the peak current in the switching period K

$$I_{L2k}=\frac{D\left(1-D\right)\sqrt{2}V}{L_2\ f_s}\sin\omega t_k\ . \tag{20}$$

The load current and the ratio of these currents in the switching period K are

$$i_{ok}=\frac{D\sqrt{2}V}{R_L}\sin\omega t_k\ ,\ \ \frac{I_{L2k}}{i_{ok}}=\frac{\left(1-D\right)R_L}{L_2\ f_s}\ . \tag{21}$$

The final equation can be used for the design of inductances L_1 and L_2, with a view to imposing a specific value of the ratio (less than 1%), calculated for the lowest value of the duty factor D.

IV. SIMULATION RESULTS

The correct functioning of the proposed circuits was tested by simulation. In all circuits, the converter was powered by a voltage V_m = 24 V, f_m = 50 Hz, the components of the power supply filter are: L=0.4 mH, C=5μF and the switching frequency is f_S=20 KHz. For the chopper in Fig. 1, used for a purely resistive load R_L=5Ω, the converter inductance was L_1=4 mH. Fig. 5 shows the waveforms of the V_o voltage and of the i_o current for a duty factor D=0.3, leading to an efficiency η=0.78. Fig. 6 shows the waveforms for D=0.9 and the resulting efficiency is η=0.89. The controlled switch pair was selected according to the V_m voltage polarity.

For the chopper in Fig. 2, destined to inductive loads, the simulations were made for L_1=L_2=4mH, L_L=6 mH, R_L=5 Ω. Fig. 7 shows the waveforms of V_o voltage and of the currents i_m and i_o for D=0.3 and Fig. 8 shows the same waveforms for D=0.9. In the first case, the efficiency was η=0.86 and in the second case, η=0.78.

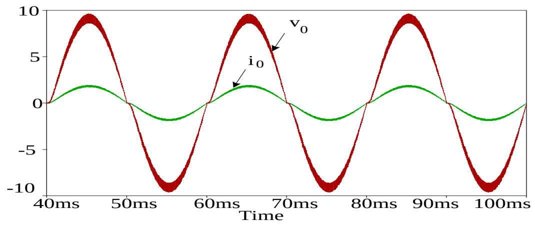

Fig. 5. Waveforms of the v_o voltage and i_o current for D=0.3.

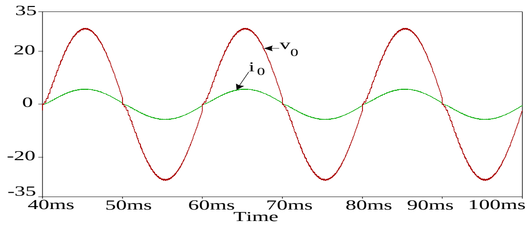

Fig. 6. Waveforms of the v_o voltage and i_o current for D=0.9.

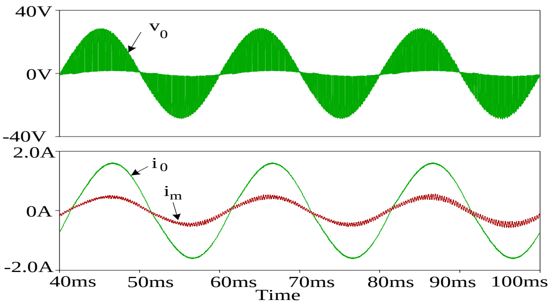

Fig. 7. Waveforms of the v_o voltage, i_m and i_o currents for D=0.3.

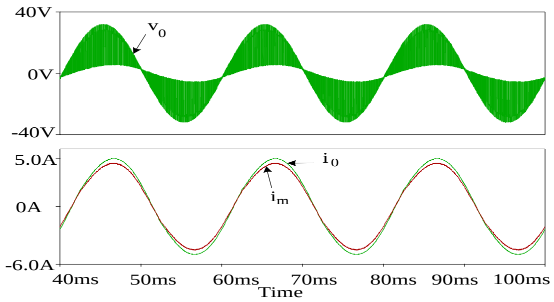

Fig. 8. Waveforms of the v_o voltage, i_m and i_o currents for D=0.9.

V. CONCLUSIONS

The paper presents two simple circuits of direct AC-AC buck converter; the first contains resistive loads and a single inductance (besides the input filter); the second is for inductive loads and contains two inductances.

The switches can be controlled without downtime and there is no need for snubber circuits. Circuit simulation showed that they function correctly within a high range of values of the duty factor D, and efficiency values obtained are η=0.89 for D=0.9 and η=0.78 D=0.3 in the case of resistive loads, and η=0.89 for D=0.9 and η=0.76 for D=0.3 in the case of inductive loads.

The power source voltage was evenly sampled, the control circuits are very simple and the component voltage and currents requirements are normal. The network filter, which eliminates the input current harmonics, is also very simple.

The circuits analysed are single-phase circuits, but a three-phase converter can be easily obtained by joining three single-phase converters. A terminal of the load impedance is connected to the network null.

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